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# Indirect Compensation Techniques for Three-Stage CMOS Op-Amps

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# Indirect Compensation Techniques for Three-Stage CMOS Op-amps

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**Abstract**— As CMOS technology continues to evolve, the supply voltages are decreasing while at the same time the transistor threshold voltages are remaining relatively constant. Making matters worse, the inherent gain available from the nano-CMOS transistors is dropping. Traditional techniques for achieving high-gain by vertically stacking (i.e. cascoding) transistors becomes less useful in nano-scale CMOS processes. Horizontal cascading (multi-stage) must be used in order to realize high-gain op-amps in low supply voltage processes. This paper discusses new design techniques for the realization of three-stage op-amps. The proposed and experimentally verified op-amps, fabricated in 500 nm CMOS, typically exhibit 30 MHz unity-gain frequency, near 100ns transient settling and 72° phase-margin for 500pF load. This results in significantly higher op-amp performance metrics over the traditional op-amp designs while at the same time having smaller layout area.

**Index Terms**—CMOS Amplifiers, low-voltage amplifier, nano-CMOS, Op-amp compensation, three-stage op-amps.

## I. INTRODUCTION

OPERATIONAL Amplifiers are an indispensable building block in the modern integrated systems. They are used in wide variety of circuit topologies including data-converters, filters, buffers and voltage references. However, continued scaling in CMOS processes has continuously challenged the established paradigms for operational amplifier (op-amp) design. As the feature size of CMOS devices keeps shrinking, enabling yet faster speeds, the supply voltage ( $V_{DD}$ ) is scaled down to enhance device reliability and to reduce power consumption. The downward scaling in gate length results in higher transition frequency,  $f_T$ , and hence faster transistors. But the higher speed comes at the cost of a reduction in transistor's inherent open-loop gain ( $g_m \cdot r_o$ ). Also with device scaling, the threshold voltage of transistors doesn't scale well with the supply voltage resulting in shrinking the voltage headroom for the amplifier [1].

The open-loop gain of the MOSFET has dropped to 10's in the sub-100nm CMOS processes and will continue to decrease with further scaling [2]. Also with scaling, the process variations become more pronounced leading to significant random offsets in op-amps due to the device mismatches.

Due to the shrinking voltage headroom with continued CMOS scaling, the paradigm of vertical stacking of devices (i.e. cascoding) needs to be replaced by horizontal cascading. Thus, in order to meet the gain requirements of op-amp in nanoscale CMOS processes, three or more stage op-amp topologies have become important.

In this paper we review the indirect-feedback compensation method for designing low-voltage, high-speed op-amps and apply it to the design of three-stage CMOS op-amps. Novel low-power cascaded three-stage op-amp topologies are proposed, with experimental results, which provide substantial improvement in performance and are tolerant to device mismatches.

## II. LOW VOLTAGE INDIRECT FEEDBACK COMPENSATION

The class of compensation in which the compensation current is fed back indirectly from the output to the internal high impedance node is defined as *Indirect Feedback Frequency Compensation* [1], [3], [4]. In this method, the compensation capacitor is connected to an internal low impedance node in the first gain stage, which allows indirect feedback of the compensation current from the output node to the internal high-impedance node i.e. the output of the first stage. In nano-CMOS processes high-speed, two-stage op-amps can be designed by employing a split-length composite transistor for indirect compensation instead of using a common-gate device in the cascode stack [5].

Figure 1 depicts splitting of an n-channel MOSFET (NMOS) or a p-channel MOSFET (PMOS) to create a low impedance internal node-A. For an NMOS, the lower device, M1B, will be in cut-off or triode region but never in saturation rendering the node-A a low impedance node [1].

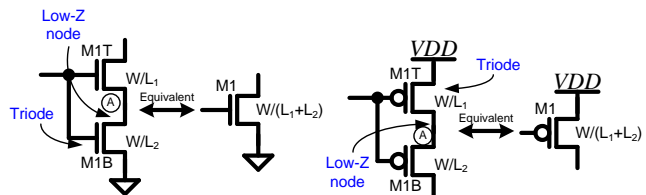


Fig. 1. Illustration of the split-length NMOS and PMOS devices and the low-impedance nodes amenable for indirect compensation [1].

The low-impedance node-A is used to feedback the compensation current to the output of the first stage. Figure 2 exhibits two-stage op-amps with a split-length current mirror load (SLCL) and split-length diff-pair (SLDP) topologies. Here,  $v_p$  and  $v_m$  are the positive and negative inputs respectively and  $v_{out}$  is the output of the op-amp [5].

When using indirect compensation, we obtain a left half plane (LHP) zero located at  $z_1 = g_{mC}/C_C$ , instead of an RHP zero, which enhances the phase margin. Also, the second pole,  $p_2$ , gets moved further away from the dominant pole by a factor of roughly  $C_C/C_1$ . Hence, pole splitting can be achieved with a

lower value of the compensation capacitor  $C_C$  and with a lower value of  $g_{m2}$ . This results in a significantly larger unity gain frequency ( $f_{un}$ ) attainable by the op-amp, with lower power consumption and more compact layout, when compared to the Miller compensated op-amps [3], [5].

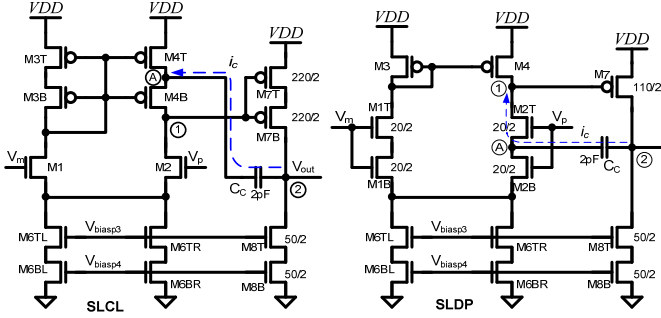


Fig. 2. Two-stage, Split-length Current mirror Load (SLCL) and Split-length Diff-pair (SLDP) op-amp topologies employing indirect compensation [3].

### III. INDIRECT COMPENSATION OF THREE-STAGE OP-AMPS

Continued interest in the three-stage op-amp design has seen numerous three-stage op-amp design techniques [6]-[11]. However, they have not been widely used in system design due to the either complex implementation or large power consumption. This section introduces design techniques which provide high-speed, device offset tolerant, stable and relatively low power three-stage op-amps.

#### A. Three-Stage Op-amp Topology

The indirect compensation technique, described in Sec. II, can be applied to three-stage op-amp design. A reversed nested compensation topology is employed as the output is not loaded by both of the compensation capacitors which results in larger unity gain frequency ( $f_{un}$ ). Figure 3 shows a reverse-nested indirect-compensated (RNIC) class-A three-stage op-amp. A stack of maximum three transistors is used to realize the low- $V_{DD}$  gain stages.

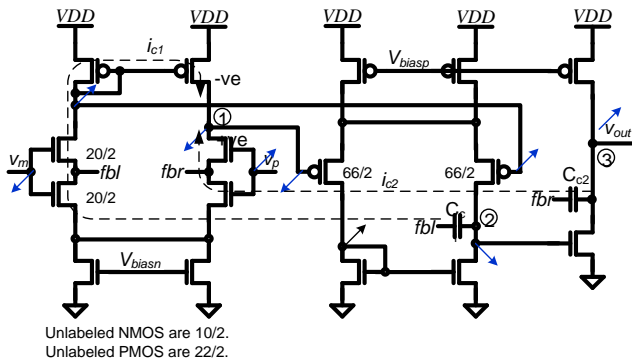


Fig. 3. A low- $V_{DD}$ , three-stage, class-A op-amp topology employing reversed nested indirect compensation (RNIC).  
Unlabeled NMOS are 10/2.  
Unlabeled PMOS are 22/2.

In this topology an NMOS diff-amp is cascaded with a PMOS diff-amp which is followed by an NMOS common-source gain stage. The PMOS diff-pair in second stage employs wider devices to increase the input common-mode

range of the second stage. SLDP topology is used for indirect compensation in order to achieve higher PSRR. The voltage levels of the nodes 1 and 2 are set to be approximately equal to  $V_{biasp}$  and  $V_{biasn}$  respectively, due to symmetry in each of the diff-amps. Thus the bias currents in all the three gain stage branches are well defined, and their  $g_m$ 's and gains are precisely fixed.

The compensation capacitor  $C_{C1}$  is used to indirectly feedback the compensation current  $i_{C1}$  from the output of the second stage (node-2) to the output of the first stage (node-1). Similarly, capacitor  $C_{C2}$  is used to indirectly feedback current  $i_{C2}$  from node-3 to node-1. The feedback currents,  $i_{C1}$  and  $i_{C2}$ , are fed back in such a way that the respective loops have an overall *negative feedback*. For example, the voltages of nodes 1 and 2 decrease together. Now if the feedback current  $i_{C1}$  is fed from node-2 to node *fbr*, it will lead to positive feedback resulting in instability. Instead the compensation current  $i_{C1}$  is fed back to node *fbl*. This inverts the sign of the current indirectly fed back to node-1 and creates an overall negative feedback loop. Similarly, the compensation current  $i_{C2}$  from node-3 is indirectly fed back to node-1 through the low impedance node *fbr*. The compensation capacitance must be connected across two nodes which are moving in opposite direction.

An obvious advantage of employing indirect feedback compensation is that, unlike in the reverse nested Miller compensation, the third stage need not always be non-inverting and also the second stage need not be always inverting. Indirect compensation can be easily achieved with a non-inverting second stage and an inverting third (output) stage by choosing appropriate signs of the feedback compensation currents. In fact, indirect compensation allows any permutation of the signs of the gains of the op-amp stages. Also the forward path delay is minimized, as we do not have to use a current mirror for non-inverting stages [9]-[11].

#### B. Small Signal Analysis

The small signal model for the RNIC three-stage op-amp (see Fig. 4) is derived using the two-stage indirect compensation model [5]. Here,  $g_{m1}$  and  $g_{m2}$  are the transconductances of transistor M2T and M1T respectively.  $R_{C1}$  and  $R_{C2}$  are the impedance attached to the nodes *fbr* and *fbl* respectively, which are both roughly equal to  $1/\sqrt{2}g_{m1}$ . Here,  $g_{mk}$  is the transconductance of the  $k^{\text{th}}$  gain stage while  $R_k$  and  $C_k$  are the resistance and capacitance respectively, attached to the node- $k$  in the op-amps ( $k = 1, 2, 3$ ). Also, it is assumed that  $C_3, C_{C1}, C_{C2} \gg C_1, C_2$  and  $g_{mk}R_k \gg 1$ .

After applying nodal analysis to the small signal model shown in Fig. 6, the resulting transfer function can be written as

$$H(s) \approx \frac{A_{ol} (1 + b_1 s + b_2 s^2)}{\left(1 + \frac{a_0}{a_1} s\right) \left(1 + \frac{a_2}{a_1} s + \frac{a_3}{a_1} s^2\right) \left(1 + \frac{a_4}{a_3} s + \frac{a_5}{a_3} s^2\right)} \quad (1)$$

The dc gain  $A_{OL}$  is equal to  $-g_{m1}R_1g_{m2}R_2g_{m3}R_3$  and the unity gain frequency is given as

$$f_{un} = g_{m1}/(2\pi C_{c2}) \quad (2)$$

The zeros (LHP) are located at

$$z_1 \approx -1/(R_{c1}C_{c1}), z_2 \approx -1/(R_{c2}C_{c2}) \quad (3)$$

and the dominant pole is given as

$$p_1 \approx -1/(g_{m3}R_3g_{m2}R_2R_1C_{c2}) \quad (4)$$

Two low-frequency non-dominant conjugate poles  $p_{2,3}$  are from the loading on nodes 1 and 2, while high-frequency parasitic poles  $p_{4,5}$  originate from the low-impedance nodes  $fb1$  and  $fb2$ .

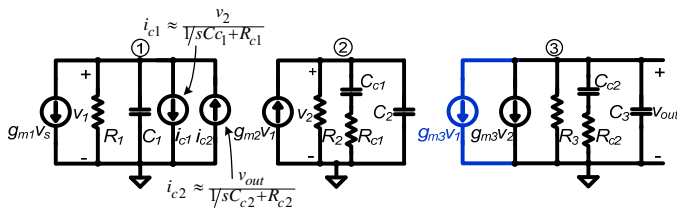


Fig. 4. Small signal analytical model for the RNIC three-stage op-amp. The highlighted  $g_{m3}v_1$  path is added for the class-AB topology.

### C. Pole-Zero Cancellation

From the small-signal transfer function seen in Eq. 1, we can cancel the LHP zeros with the non-dominant poles  $p_{2,3}$ . This can be achieved by equating the respective quadratic terms:

$$1 + b_1s + b_2s^2 = 1 + (a_2/a_1)s + (a_2/a_1)s^2 \quad (5)$$

The pole-zero cancellation leads to the following design criterions:

$$R_{c1} \approx \frac{C_L}{g_{m3}C_{c2}}, R_{c2} \approx \frac{C_{c1}}{g_{m3}C_{c2}}(C_L + C_{c2}) \approx \frac{C_{c1}}{C_{c2}}R_{c1} \quad (6)$$

Note that the design criterions are independent of the parasitic nodal resistance and capacitance values. The values of impedances  $R_{c1}$  and  $R_{c2}$  are estimated using Eq. 6. These resistance values are realized by using additional resistors, in series with the compensation capacitors  $C_{ck}$ . Thus we also have the limitation that  $R_{ck} > 1/\sqrt{2}g_{mk}$ , as the value of  $R_{ck}$  can not be less than the impedance offered by the internal nodes  $fb1$  and  $fb2$ . The pole-zero cancellation leads to real pole-zero doublets located at

$$p_2 = z_1 \approx \frac{-1}{R_{c1}C_{c1}} = \frac{-g_{m3}C_{c2}}{C_{c1}C_3} \quad (7)$$

$$p_3 = z_2 \approx \frac{-1}{R_{c2}C_{c2}} = \frac{-g_{m3}C_{c2}}{C_{c1}(C_3 + C_{c2})} = \frac{p_2}{1 + C_{c2}/C_3} \quad (8)$$

From Eq. 7 and 8, we can see that the non-dominant pole-zero doublets appear close together in the frequency domain. This arrangement of the non-dominant poles and LHP is the optimal pole-zero constellation for a low-power three-stage op-amp.

Perfect pole-zero cancellation is difficult to achieve with

process and temperature variations and the locations of poles and zeros are likely to vary. But even with these variations the pole-zero pairs remain *collocated* and form pole-zero doublets. The pole-zero doublets have been reported to degrade time domain settling of the op-amp, if the doublet is located at a frequency less than  $f_{un}$  [10]. Thus, the pole-zero doublets should be placed at a frequency higher than the  $f_{un}$  of the op-amp. This leads to another constraint for unconditional time-domain stability given as  $p_{2,3}, z_{1,2} > g_{m1}/C_{c2}$ , which results in the upper bound on  $f_{un}$

$$f_{un} \leq \frac{1}{2\pi} \sqrt{\frac{g_{m1}g_{m3}}{C_{c1}C_3}} \quad (9)$$

Since the parasitic poles  $p_{4,5}$  are located at a high frequency, the resulting small-signal transfer function of the RNIC op-amp has a single dominant pole response with almost 90° phase margin, and a near first order transient settling.

Figure 5 shows an RNIC class-AB op-amp derived from the topology seen in Fig. 3. Here, the output of the first stage is be used to drive the gate of the PMOS M10. Now, the gate of M10 is biased at  $V_{biasp}$  and the gate of M11 is biased at  $V_{biasn}$ , and they move almost together emulating a bias battery for the class-AB output stage. A low power (LP) implementation of the three-stage RNIC op-amp is shown in Fig. 6.

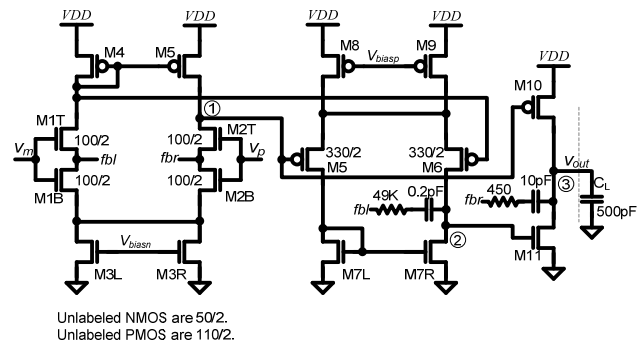


Fig. 5. A pole-zero cancelled, class-AB, RNIC, three-stage op-amp driving 500pF load.

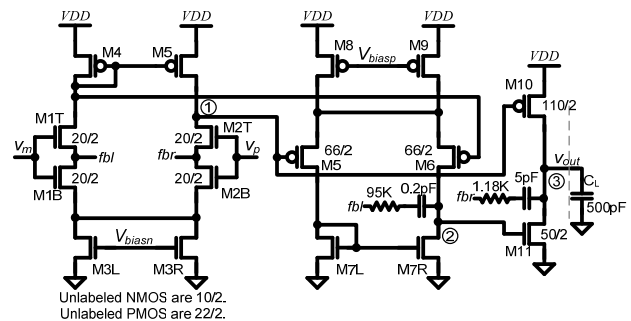


Fig. 6. A low-power implementation of the class-AB, RNIC, three-stage op-amp driving 500pF load (RNIC-LP).

The RNIC op-amp exhibits a simulated unity-gain frequency ( $f_{un}$ ) of 30 MHz and a phase margin ( $PM$ ) of 72° (as illustrated in Fig. 7). On the other hand the RNIC-LP design exhibits a  $f_{un}$  equal to 12 MHz and a  $PM$  close to 89°.



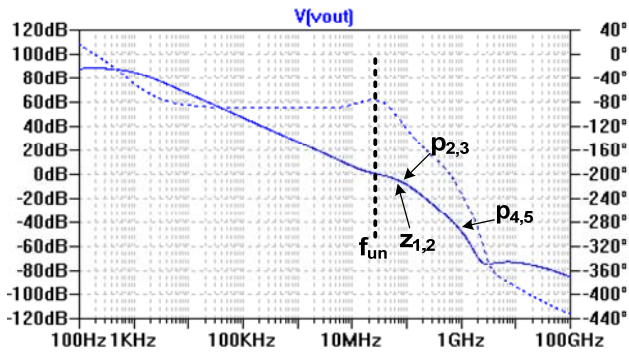


Fig. 7. Spice simulated frequency response of the pole zero cancelled RNIC three-stage op-amp. Here  $A_{OL}=87\text{dB}$ ,  $f_{un}=30\text{MHz}$  and  $PM=72^\circ$ .

#### IV. CHIP TEST RESULTS AND PERFORMANCE COMPARISON

The test chip designed in 500 nm CMOS process include single-ended op-amps driving 500 pF off-chip load (see Fig. 8). The step input response measured with the op-amps in unity gain configuration is shown in Fig. 9. The 99% transient settling time ( $t_s$ ) for a 100 mV step is found to be roughly 100ns and 250ns for the RNIC and RNIC-LP op-amp topologies. A performance comparison of the op-amp topologies designed on the test chip with the recently reported designs is presented in Table 1. The figure of merit metrics,  $FoM_S = f_{un}C_L/V_{DD}I_{DD}$  and  $FoM_L = SR.C_L/V_{DD}I_{DD}$ , are used to compare the performance of the op-amps as in [10], [11]. The proposed RNIC op-amps display higher  $FoM_s$ , faster transient settling and near ideal phase margins. The proposed three-stage RNIC topologies are elegant, low-voltage, offset tolerant and hence manufacturable in nano-CMOS processes.

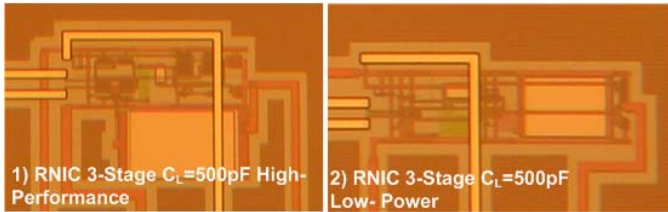


Fig. 8. Micrographs of the three-stage op-amps fabricated on the test chips.

#### V. CONCLUSION

The proposed RNIC three-stage op-amps exhibit large dc

gain, and settling as fast as a corresponding two-stage amplifier, with minimal excess power consumption and layout area. The proposed three-stage RNIC topologies are elegant, low-voltage, offset tolerant and hence manufacturable in nano-CMOS processes.

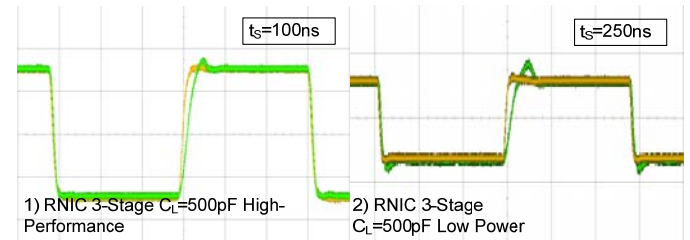


Fig. 9. Scope capture of the input step response (100mV) for the three-stage op-amps in unity gain configuration.

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TABLE I  
THREE-STAGE OP-AMP PERFORMANCE COMPARISON

	$C_L$ (pF)	$V_{DD}$ (V)	$I_{DD}$ (mA)	Power (mW)	$f_{un}$ (MHz)	$\langle SR \rangle$ (V/ $\mu$ s)	$C_{C1}, C_{C2}$ (pF)	$A_{OL}$ (dB)	$\langle t_s \rangle$ (ns)	$PM$	$FoM_S$	$FoM_L$	$IFoM_S$	$IFoM_L$
AFFC [6]	100	1.5	0.17	0.25	5.5	0.36	5.4, 4	100	510	61°	2157	1413	3235	212
TCFC [7]	150	1.5	0.03	0.045	2.85	1.04	1.1, 0.9	100	2000	59°	9500	3450	14250	51575
RNMC VB NR [8]	15	3	0.48	1.44	19.5	13.8	3, 0.7	83	75	56°	209	149	608	431
SMFCC [9]	120	2	0.21	0.42	9	3.4	4, 0	100	510	57°	2571	971	5143	1943
RNMCFNRR [10]	500	3	0.085	0.255	2.4	1.8	11, 0.35	109	780	58°	4706	3529	14118	10588
RAFFC [10]	500	3	0.105	0.315	2.4	1.95	11, 0.35	112	530	58°	3810	3095	11429	9286
RAFFC LP [10]	500	3	0.03	0.105	1.1	1.29	11, 0.35	113	1000	56°	5238	6143	15714	18429
SMCNR [11]	150	1.5	0.014	0.021	1.6	0.65	2.2, 0	113	1300	57°	11429	4643	17143	6964
<b>RNIC-LP (this work)</b>	<b>500</b>	<b>3</b>	<b>0.18</b>	<b>0.54</b>	<b>12</b>	<b>8</b>	<b>5, 0.2</b>	<b>89</b>	<b>250</b>	<b>88°</b>	<b>11111</b>	<b>7407</b>	<b>33333</b>	<b>22222</b>
<b>RNIC (this work)</b>	<b>500</b>	<b>3</b>	<b>0.5</b>	<b>1.5</b>	<b>35</b>	<b>20</b>	<b>10, 0.2</b>	<b>89</b>	<b>100</b>	<b>72°</b>	<b>11667</b>	<b>6667</b>	<b>35000</b>	<b>20000</b>
<b>RNIC-LP (this work)</b>	<b>500</b>	<b>2</b>	<b>0.18</b>	<b>0.36</b>	<b>7</b>	<b>20</b>	<b>5, 0.2</b>	<b>87</b>	<b>350</b>	<b>88°</b>	<b>9722</b>	<b>27778</b>	<b>19444</b>	<b>55556</b>
<b>RNIC (this work)</b>	<b>500</b>	<b>2</b>	<b>0.5</b>	<b>1</b>	<b>18</b>	<b>20</b>	<b>10, 0.2</b>	<b>87</b>	<b>150</b>	<b>72°</b>	<b>9000</b>	<b>10000</b>	<b>18000</b>	<b>20000</b>