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Silver Chalcogenide Based Memristor Devices

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***Abstract*—We have fabricated two-terminal chalcogenide-based devices containing Ge_2Se_3 and Ag that function as memristors. These devices have been electrically characterized at room temperature using quasi-static DC methods, AC sinusoidal methods, and AC pulse testing methods. In all cases, the devices exhibit memristive behavior.**

***Index Terms*—Memristor, Memory Device, Thin Film Devices**

I. Introduction

THE MEMRISTOR device postulated in 1971 by Leon Chua [1] as the fourth basic circuit element has received much attention in the research community since the publication of Strukov's 2008 paper titled "The missing memristor found." [2] The memristor name is a contraction for memory resistor [1] because that is exactly its function: to remember its resistance state [3]. The memristor is a two terminal passive device whose resistance state depends on its previous state and present electrical biasing conditions, and when combined with transistors in a hybrid chip, memristors could radically improve the performance of digital circuits without the need for further reduction of transistor dimensions [3]. Given their two terminal structural simplicity and electronic passivity, the applications for memristor technology range from non-volatile memory, instant on computers, reconfigurable electronics and neuromorphic computing [3, 4].

In this work, we present Ag-chalcogenide devices that exhibit memristor electrical characteristics. DC and AC electrical characterization is presented and observations discussed.

II. Experimental Details

Memristor devices were fabricated on 200 mm p-type Si wafers. Isolated W bottom electrodes were patterned on the wafers and a planarized nitride layer was used for device isolation. Vias were etched through the nitride layer to provide contact to the bottom electrode and to define the device active region. Prior to deposition of the memristor materials, the wafers received an Ar^+ sputter clean to remove residual material and potentially remove any oxides that might have formed over the W electrode. The memristor device structure consists of the layers (from bottom electrode contact side to top electrode contact): 300 Å Ge_2Se_3/500 Å Ag_2Se/100 Å Ge_2Se_3/500 Å Ag/100 Å Ge_2Se_3, see Fig. 1. The 100 Å Ge_2Se_3 layers are needed for device processing only since Ag cannot be deposited directly on Ag_2Se and since W (for the top electrode) does not adhere well to Ag in this material stack. The layers were deposited by thermal evaporation using a CHA Industries SE-600-RAP thermal evaporator equipped with three 200 mm wafer planetary rotation. The rate of material deposition was monitored using an Infincon IC 6000 with a single crystal sensor head. The base system pressure was $1x10^{-7}$ Torr prior to evaporation. A W top electrode was created by sputtering W (350 Å) and etching to define the device top contact and bond pad. Etching was performed with a Veeco ion-mill by etching through the W and the memristor device materials and stopping on nitride. The top and bottom electrode bond pad contacts were 80 µm x 80 µm.

Electrical measurements were performed with either an HP4145B or an Agilent B1500A semiconductor parameter analyzer. A Micromanipulator 6200 microprobe station equipped with a temperature controllable wafer chuck was used for the wafer-level device measurements. Probe tips were either Micromanipulator W size 7B or American Probe and Technologies 73CT-APTA probe tips. The tested devices were 180 nm in diameter as defined by the via etched through the nitride layer to the bottom electrode, Fig. 1.

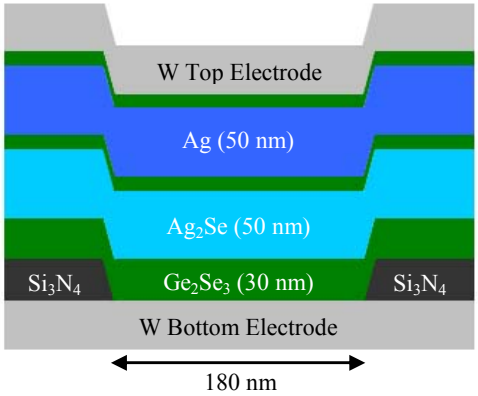

Fig. 1. Schematic representation of the fabricated device illustrating the material layers and dimensions. The unmarked layers are Ge_2Se_3 (10 nm).

III. Memristor Theory

A basic mathematical definition of a memristor is that of a voltage-controlled, one-port device in the generalized class of nonlinear dynamical systems called memristive systems

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described by (1) and (2). Here, x can be a set of state variables, G is a device conductance, and f is a generalized function [4]. Time, device current, and device voltage are represented by t, i, and v.

$$i = G(x,v,t)v \tag{1}$$

$$\frac{dx}{dt} = f(x,v,t) \tag{2}$$

In [2], Strukov et al. expounded on the mathematical memristor model and identified a state variable as the width, w, of a doped semiconductor region, illstrated in Fig. 2. This doped region represents a region of low resistance, R_{ON}, while the undoped region supplies a high resistance, R_{OFF}, and the total device resistance is the series combination of the two for a device of thickness D. Through appropriate biasing, w can expand or contract and the resistance (and thus conductance) of the device can be modulated, as predicted in (1). The modulated resistance in [2] is attributed to the migration of oxygen vacancies from the doped region into the undoped region due to the field applied across the device. It is worth noting that modulated device resistance due to ion migration had been observed and identified for decades [5, 6], however, Strukov et al. identified this behavior as that of a memristor and helped explain the unique electrical characteristics exhibited by the device.

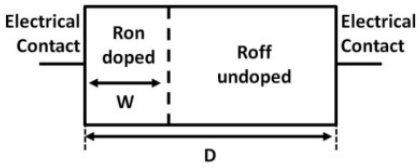

Fig. 2. Memristor device schematic illustrating the separation between the doped and undoped region. The width of the doped region, w, was identified as a state variable, x, from (1).

IV. Electrical Characterization Results

Figure 3 displays the typical electrical Lissajous I-V curve behavior of our memristor device under a sinusoidal input of 0.45 V and changing frequency. At 100 Hz, we can clearly observe that the memristor toggles between two states of low and high conductivity. The transition from low to high conductivity occurs near a threshold voltage of 0.24 V. In this case, Ag^+ ions have migrated into the active chalcogenide, Ge_2Se_3, layer and created a low-resistance path through the insulator. When the voltage decreases to an erase threshold of -0.32 V, Ag^+ ions are removed from the active chalcogenide layer and the device returns to a high-resistance state. At higher frequencies, for example 100 kHz, the device behavior approaches that of a linear resistor. This frequency-dependent behavior was predicted in [4].

Calculating the charge and flux through the device by the time integration of the current and voltage at 100 Hz produces the curves shown in Fig. 4. It is clear the charge-flux behavior is not a proper function given the multiple charge values for a single flux value. This fact contradicts the original definition of an ideal memristor as originally postulated in [1]. Instead, Fig. 4 shows two distinct nonlinear charge-flux functions – the first relating charge and flux for a device initially in a high-resistance state and the second function describing a change from low resistance to high resistance. The combination of the two functions in the complete charge-flux relation suggests the device is best described as a memristive device, i.e. a device exhibiting memristance, as opposed to an ideal memristor [4, 7].

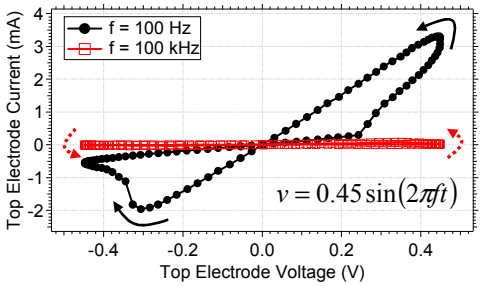

Fig. 3. Typical Lissajous I-V curve as a function of frequency for our memristor device. At low frequencies, a pinched hysteresis curve is clear. At higher frequencies, the device behavior approaches that of a linear resistor.

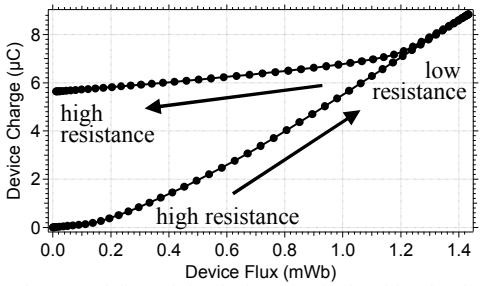

Fig. 4. Charge and flux of the device as calculated by the time integral of the 100 Hz I-V in Fig. 3. Since charge and flux are not related by a single function, the device is not an ideal memristor, strictly speaking, but is best described as a memristive device.

Another interesting characteristic of our device is the ability to continuously modulate the resistance through the application of sequential biasing. Fig. 5 shows five quasi-static DC sweeps in which the resistance of the device changes when a large enough bias is applied. For example, examining the first sweep shows a large resistance change once the voltage reaches a threshold of 0.24 V. On the second sweep only 0.17 V is needed to change the resistance, where sweep

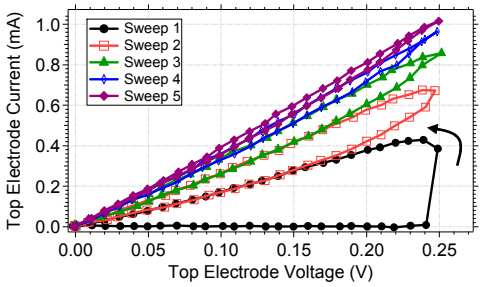

Fig. 5. Applying sequential DC sweeps to the device results in successive reduction of the device resistance. This behavior is equivalent to neurological synapses and thus a memristor can be considered an electrical synapse.

two no longer overlaps sweep one. Since a minimum threshold voltage is needed to change the resistance state of the device, relatively small voltages can be used to read the device without altering the resistance state. Furthermore, the multiple lower resistance states of the device based on the number of times biased is analogous to the behavior found in a neurological synapse. Consequently, the memristor can be considered the electrical equivalent of a synapse [8].

Conditioning the device through application of several negative pulses produces a typical DC I-V curve for the Ag-containing chalcogenide device as shown in Fig. 6. The memristor behavior is exhibited in the negative voltage region. Note the negative differential resistance (NDR) region between -0.2 and -0.4 V, characteristic of memristive devices.

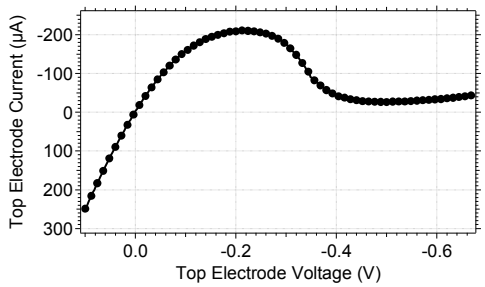

Fig. 6. Typical Ag-chalcogenide memristor DC I-V curve illustrating a negative differential resistance (NDR) region.

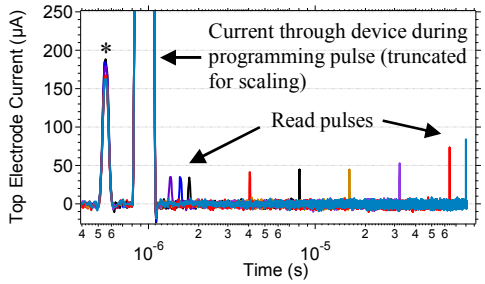

Fig. 7. After programming, a device resistance will decay. The * denotes the current through the device at steady state, prior to programming. The large truncated pulse is the current through the device during programming. The read pulses following the programming show how the device resistance changes as a function of time for the given programming conditions. Each read pulse corresponds to a different pulse test on the same device.

In addition to showing a dependence on their past state, the Ag-chalcogenide devices show initial time dependence after programming wherein the device state will relax toward its initial state. After conditioning the device with negative pulses, a steady-state current (marked with *) was reached, Fig. 7. A time dependent relaxation is observed by reading current through a device after programming with a -1.1 V, 250 ns pulse. As the read pulse time delay is increased, the current through the device increases. With this given programming pulse (-1.1 V, 250 ns), the device reaches a higher resistance initially, but over a period of hundreds of microseconds, decays back to a lower resistance state. A time-dependent resistance (or conductance) is accounted for in (1) and complies with memristive behavior. However, this data suggests that shorter programming pulses may be insufficient to program the device into a time-stable resistance state.

V. Conclusion

We have fabricated and tested Ag-containing chalcogenide devices that exhibit memristor electrical characteristics. The AC characteristics presented illustrate the pinched I-V curve that approaches a linear resistor as frequency increases. DC characteristics show distinct resistance states dependent on previous states and applied voltage. Further DC data shows NDR curves characteristic of memristive devices. Pulse tests illuminate a time-dependence on the resistance state of the device. Further device characterization will explore pulse width effects and temperature effects of the device state.

Acknowledgment

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