

8-1-2005

Low-Voltage Bandgap Reference Design Utilizing Schottky Diodes

David L. Butler
IEEE

R. Jacob Baker
Boise State University

Low-Voltage Bandgap Reference Design Utilizing Schottky Diodes

David L. Butler and R. Jacob Baker

Department of Electrical and Computer Engineering
Boise State University, Boise, Idaho USA
e-mail: dlbutler@ieee.org or jbaker@boisestate.edu

Abstract - As semiconductor device geometries continue to shrink, the corresponding voltage applied across the processed devices must also be reduced. Therefore reference voltages used in integrated circuits will need to be reduced as well. A typical bandgap reference (BGR) voltage generator uses PN junction diodes or PNP BJT's to bias the reference. The forward bias voltage of these devices is typically 0.7 volts, and has a limiting effect on how low a reference voltage can be generated, as well as how low a system voltage can be applied. Schottky, or metal-semiconductor (MS), diodes have a lower forward bias voltage, typically of about 0.3 volts. The implementation of Schottky metal-semiconductor diodes in place of PN diodes in the design of the BGR, should allow for lower reference voltage generation. This project consists of the design and simulation of a BGR utilizing MS diodes, followed by fabrication and validation of the design.

I. INTRODUCTION

The bandgap reference voltage generator is designed to provide a stable reference voltage across the device operating temperature and voltage. The BGR should also be functionally stable regardless of typical process variations. This circuit is a low voltage reference design for short channel processes. The design uses a known BGR circuit, but replaces the PN junction diodes with MS diodes [1].

The BGR design validation process will involve several steps. First is to simulate the design operability of the BGR after replacement of the PN diodes in the circuit with the MS diodes. An approximated Schottky diode model will be used to estimate the actual operation. The modeled circuit will then be laid out and fabricated in a short channel CMOS process. The actual diodes and resistors will not be connected, but bonded in after fabrication to allow for post fabrication circuit adjustments. Once the actual MS diodes have been fabricated, the operational characteristics will be recorded and the simulation SPICE model will be updated accordingly. With this more accurate diode model, the BGR circuit design will then be further simulated to achieve an optimized reference. Then the final circuit will be built and characterized. Design validation will involve showing acceptable BGR operation, measured across nominal voltage, temperature and process variations.

II. CIRCUIT DESIGN

The bandgap reference generates a stable voltage over temperature ranges utilizing devices with properties that are proportional to absolute temperature (PTAT) and complementary to absolute temperature (CTAT). The circuits are used to complement each other thus providing for a more stable temperature performance than is possible with each alone [1]. The overall temperature behavior of the BGR is modeled by the following equation:

$$\frac{\partial V_{REF}}{\partial T} = nN \ln K \cdot \frac{\partial V_T}{\partial T} + \frac{N}{L} \cdot \frac{\partial V_{D1}}{\partial T} \quad (1)$$

Since the diodes in the circuit would have to be fabricated and characterized before the circuit resistor values could be determined, the resistors would not be fabricated in the layout, but would be applied externally after fabrication. The rest of the circuit (the MOSFET portion) was designed based on SPICE simulation models, based on estimates of the MS diodes anticipated operation [2]. The circuit was then ready for layout. The general BGR circuit design is shown here in Figure 1.

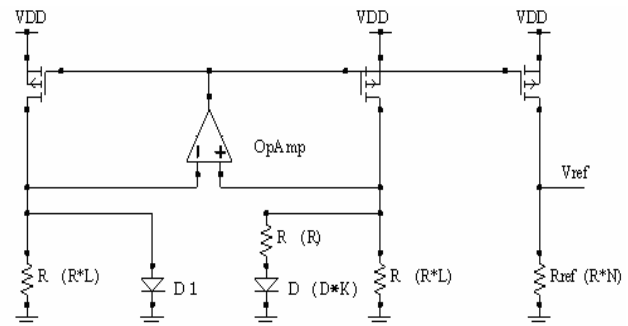
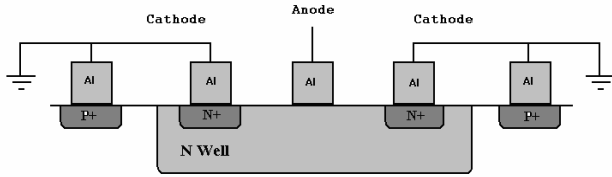


Figure 1. Bandgap Reference Circuit Design

III. FABRICATION

The actual physical implementation of the design was laid out using the LASI layout program [3]. The microchip was fabricated through a MOSIS fabrication organization [4]. The specific fabrication facility was American Microsystems Inc. (AMI) [5]. The AMI foundry produced the chip using their 0.5µm process designated AMI_C5F by MOSIS. The Technology code is SCN3ME_SUBM.

The AMI C5N process allows for the fabrication of the MS diode. The MS diode is (in this process) formed by first creating an N-well in the P-type substrate. Then an opening to the silicon (through the glass) of the N-well is created by the selection of the active layer. Unlike the more common use of the active layer as an ohmic contact, no N+ implant is selected, but rather a contact is selected and the metal (TiN/AlCu/TiN) is deposited on the N-well. This metal to low implant N-well semiconductor forms a metal semiconductor rectifying diode. The cathode of the diode is connected using a common ohmic contact. It is formed in the same N-well by means of a contact. But in this case the N+ layer is selected facilitating a high N+ type implant to the active opening, which allows for a reduced contact resistance. For this project, the ohmic contact is grounded. Contacts are also applied around the N-well in the substrate. These contacts are applied through an active and P+ layer to ensure the substrate is also tied to ground. The cross section is shown in Figure 2.



P Type Substrate

Figure 2. Schottky Diode Cross Section

In addition to the single diodes, multiple diode structures were also fabricated. These were laid out as single diodes of the same design. But to allow for larger multiple diodes for DK, (larger K) single diodes were also grouped in parallel clusters of 2, 4 and 8. These are referred to as x1, x2, x4, and x8 respectively. The full chip and diode detail are shown in Figure 3.

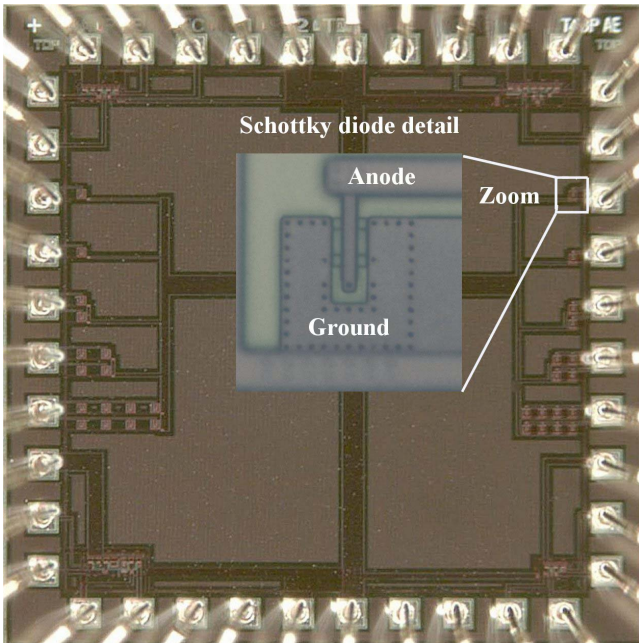


Figure 3. Full Chip Image

IV. MEASURED RESULTS

The Schottky diodes in the circuit were characterized to determine their actual operational characteristics, in order to form a more precise diode model in SPICE. This model would then be used in simulating the BGR circuit operation. Therefore a close approximation of the MS diode model, and not an exact fit, was needed to get the BGR to function. The diode current equation (ignoring series and shunt resistances) is given below in equation 2 [6]. Since the operation of this circuit does not involve reverse bias components, these were not characterized.

$$I_D = I_s \left(\exp \left\{ \frac{qV_D}{nkT} \right\} - 1 \right) \quad (2)$$

Most tests run were voltage sweeps. These were run across operating voltage and temperature, in order to determine current-voltage (I-V) curves over input voltage range and temperature.

This first test was run from 0V to 1.0V, and at 0°C and 70°C. Since the area of operation that is of interest for the BGR is below 0.6V, all future measurements were taken from 0V to 0.6V. Figure 4 shows the resulting measured I-V characteristics of a single diode.

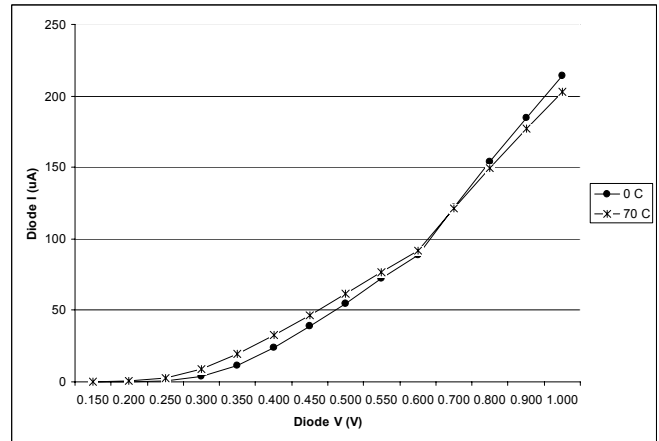


Figure 4. Schottky Diode I-V vs. Temperature

This measured data was used to determine a temperature coefficient. It is evident that the diode change in voltage with temperature is CTAT, as determined by equation 3.

$$\frac{\partial V_D}{\partial T} = \frac{V @ T_{max} - V @ T_{min}}{T_{max} - T_{min}} \quad (3)$$

The measured averaged results on two diodes indicated that the value is $-0.56 \text{ mV}/^\circ\text{C}$. This was determined by using a set current and measuring the voltage at 0°C and 70°C. In this case three currents were used (3μA, 5μA and 10μA) and the results were averaged. This brings up the point that although most devices functioned similarly, there was significant current and thermal variation between diodes.

Based on measured results of all functional single diodes, the MS diode final average resistance was determined to be approximately 2.2kΩ. This was determined by the slope of I-V curve from 0.4V to 0.6V, since the series resistance is one divided by the slope of the I-V curve. The ideality factor (n) and saturation current (Is) were estimated by applying values to the SPICE simulation, and modeling it to the actual measured curve. Using this method, n was determined to be approx 0.43 and Is was set to $7 * 10^{-18} \text{ A}$.

With this close approximation of the diode behavior modeled in SPICE, the BGR circuit was then designed. The values of the resistor R, and ratios N and L, were calculated as follows and used in the model, with the R*N (Rref) value being trimmed as needed for the best performance. A value of 8 was used for K, as the largest diode structure fabricated had eight individual diodes.

With the diode measurements taken relative to temperature (as previously noted), the diode thermal derivatives was determined to be:

$$\frac{\partial V_{D1}}{\partial T} = -0.56 \text{ mV}/^\circ\text{C}$$

Since the design involved unknown resistor values, external 1/8W carbon film resistors were implemented. The thermal effect was

minimal because of the ratios used in the design, and is expected to be similar on actual fabricated resistors.

$$\frac{\partial V_T}{\partial T} = 0.085\text{mV}/^\circ\text{C}$$

With this information, and setting the temperature coefficient (TC) to zero (desired), the following were solved for. First L is determined through the following equation:

$$L = \frac{-\frac{\partial V_{D1}}{\partial T}}{n * \ln K * \frac{\partial V_T}{\partial T}} \quad (4)$$

Next N was solved as is indicated in the following equation:

$$N = \frac{V_{REF}}{nV_T * \ln K + \frac{V_{D1}}{L}} \quad (5)$$

With the diode current estimated at 1μA, R was solved for from the following equation:

$$R = \frac{n * V_T * \ln K}{I} \quad (6)$$

The resulting L was 7.7 and N was 6.6. With R solved as 22kΩ. With these values, resistors were set as follows:

$$R * L = 22\text{k}\Omega * 7.7 = 172\text{k}\Omega$$

$$R * N = 22\text{k}\Omega * 6.6 = 145\text{k}\Omega$$

Since the goal was to develop a low voltage reference, a voltage of 0.4 volts was selected as a target. This is an arbitrary point, but it is within the low voltage arena that is the desirable area of operation. The target operating voltage (VDD) range was from 2.0V to 3.0V. It should be noted that the 0.5μm AMI process used in the fabrication of the chip is a 3.3V-5.0V process. A process temperature range of 0°C to 70° was used as the temperature range of evaluation.

Based on these criteria, and through simulation trial and error, Rref was initially set to 35kΩ instead of the calculated 145kΩ. Simulation indicated that at Rref of 145kΩ, the output voltage was closer to 0.7V. Thus a value of 35kΩ was used, with Rref being refined later once the actual results could be evaluated. The final circuit was then built using the values for R, N and L based on the calculated and simulation results, as shown in Figure 5.

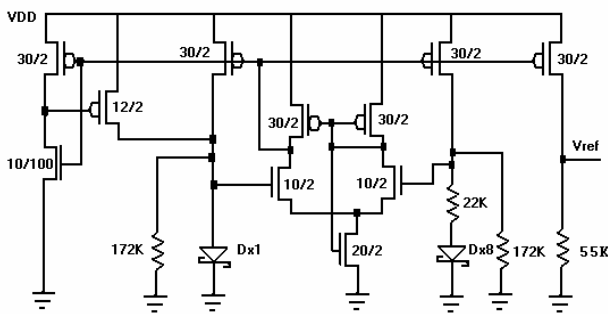


Figure 5. Final BGR Design

Note that Rref value differs from the original 35kΩ and this 55kΩ is the final trim value that brought Vref to 400mV at 2.5V VDD and 25°C. Pre-trim, the first parts reference voltage was measured as 0.251V at a VDD of 2.5V, lower than desired. It was expected to be necessary to “trim” the output resistor (Rref) to tune the

circuit. Once Rref was trimmed, the reference output shown in Figure 6 was produced.

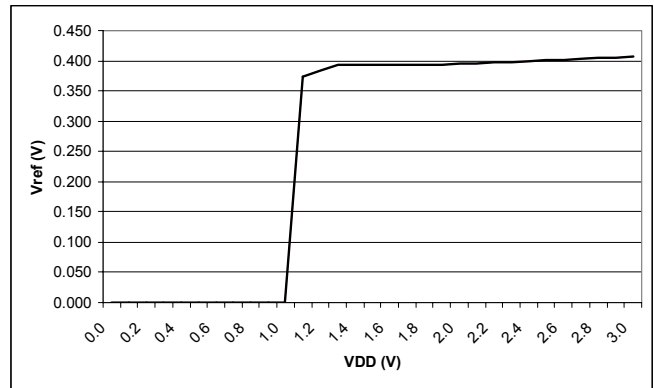


Figure 6. Measured Reference Voltage

The resulting output was relatively stable over the operating range of 2.0V to 3.0V. The startup circuit was toggled in until the circuit started (at approx 1.1V) and was then disconnected. (Because the startup circuit was considered a potential problem during the preliminary design phase, it was bonded out in the actual layout so the BGR could be evaluated independently of the startup circuit.) The circuit proved stably functional at a low of 1.2V VDD. Over the operating voltage range (from 2.0V to 3.0V VDD), the reference voltage shift was 14mV. Three other parts measured were 7mV, 8mV, and 24mV. The circuit current was approximately 23.75μA at 2.5V VDD and 25°C.

The temperature effects were also evaluated. Figure 7 shows the operation of the circuit as measured at 0°C and at 70°C.

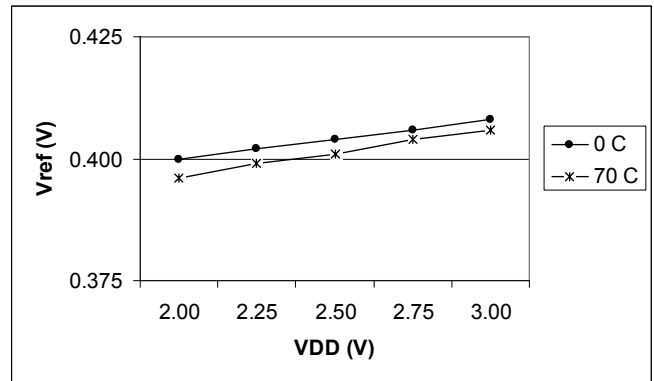


Figure 7. BGR Temperature Behavior

As is evident in Figure 7, there is little temperature variation between the minimum and maximum operating ranges. The TC of this part was calculated at 2.5V VDD using equation 7 [5].

$$TC = \frac{1}{V_{REF}} \left(\frac{\partial V}{\partial T} \right) = \frac{1}{V_{REF}} \left(\frac{V_{REF\ max} - V_{REF\ min}}{T_{\max} - T_{\min}} \right) * 10^6 \quad (7)$$

The TC was calculated as -107ppm/°C, and indicates a voltage variation of only -43μV/°C. Other parts tested were 214, 286, and 500ppm/°C.

As a further evaluation, the external resistor Rref on one part was trimmed to achieve a 100mV Vref at 2.5V VDD. Although the circuit resistor values were not optimized for this reference voltage,

the BGR was evaluated simply at 25°C to determine if functionality was possible at this voltage by trimming alone. Resistor Rref was trimmed at 2.5V to 23.14kΩ, where Vref was at 0.10V. Over the 2.0V to 3.0V VDD range, the circuit operated well, with Vref varied only 2.2mV over the 1.0V range.

Note that there are process variation effects in the reference voltages and thermal characteristics. To determine the cause of these effects, one BGR circuit was tested at 25°C and 2.5V VDD. It was set to a reference voltage of 400mV, then while all other factors remained the same (even the same diode set was used for DK) the single diode D1 was replaced one at a time with the other single functional diodes. Figure 8 shows the resulting reference voltages.

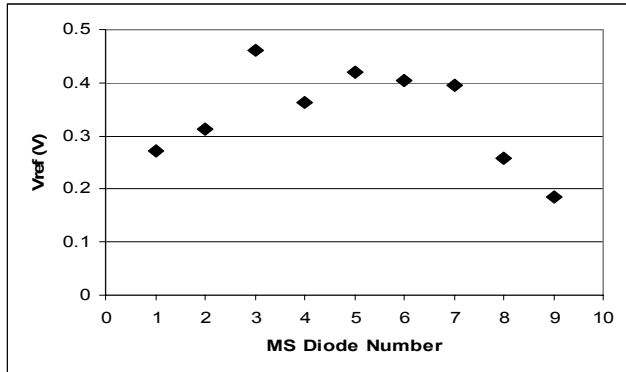


Figure 8. Vref Distribution Relative to D1

The Vref changed considerably as the BGR was operated with the different diodes indicating that the diodes did contribute significantly to variations in the reference voltage. Reference voltages ranged from 0.185V to 0.462V with D1 as the only variable.

The modeling of all diodes using a HP 4156 parameter analyzer indicated significant variation of the single diode (x1) I-V distribution, and the reducing distribution on the x2, x4 and then minimal distribution of the x8 diode structures. Further, the diodes threshold voltages (Vt) were compared. The results can be seen in Figure 9.

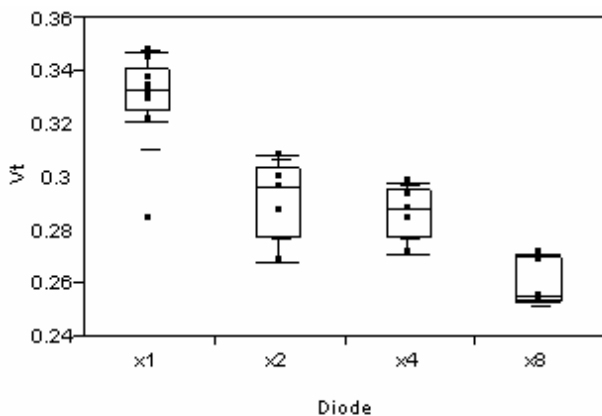


Figure 9. MS Diode Vt Distribution

Note the large distribution of the single diodes vs. the smaller distribution of the x8 diode structures. It should be noted that one single diode was excluded from this distribution as 5μA of current was never achieved, even at 0.6V external voltage.

The Vt point itself is lower for the multiple diode structures as is expected, since multiple diodes are connected in parallel. In addition to allowing for a tighter distribution, this attribute may also benefit the design as a lower diode Vt allows for lower reference voltage generation. Simulations were run on the BGR design using the x8 diode structure model that indicated the circuit would function if x8 diode structures were employed in its design.

V. CONCLUSION

The results indicate that the BGR design utilizing Schottky diodes was functional over the intended operating voltage and temperature ranges. Although there was evidence of significant initial condition variation induced by process variation, the post trim results indicated this variation could be minimized.

Measured results indicate a MS diode threshold voltage thermal characteristic of -0.56mV/°C. With several parts evaluated, the BGR circuits produced a reference voltage with a voltage gradient of a low of 7mV/V, to a high of 24mV/V, across a one volt VDD sweep. Temperature coefficients ranging from -107ppm/°C to 500ppm/°C were measured.

Further, results indicate there would be process variation mitigation benefits by use of the same BGR circuit, but utilizing multiple MS diode structures for D1 instead of a single diode. Multiples of DK would also be utilized. Given the variations in the single diode, and the lack of variation of the multiple diode structures, it appears that using multiple structures could help minimize process variation effects and thus make the circuit operation more predictable. It would also seem likely to have the effect of reducing the probability of a single diode defect causing the circuit to fail, as an open (or high resistance) in one diode would be mitigated by the operation of the other diodes.

REFERENCES

- [1] R. Jacob Baker, "CMOS Circuit Design, Layout and Simulation" 2nd edition Wiley Interscience, 2005 pp745-770
- [2] Ouse Tech, WinSpice Version 1.05.07 <<http://www.winspice.co.uk/>>
- [3] Dr. D. E. Boyce, LASI [Layout System for Individuals] Version 7.0.2.7 <<http://members.aol.com/lasicad/>>
- [4] MOSIS "Low-Cost Prototyping and Small-Volume Production Service" <<http://www.mosis.org/>>
- [5] AMIS [C5N Process] <<http://www.mosis.org/products/fab/vendors/amis/c5/>>
- [6] Dieter K. Schroder, "Semiconductor Material and Device Characterization" 2nd edition, Wiley Interscience, 1998 pp169-208