HIGH-SPEED DELTA-SIGMA DATA CONVERTERS FOR NEXT-GENERATION WIRELESS COMMUNICATION

by

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Dedicated to My Amma

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ABSTRACT

In recent years, Continuous-time Delta-Sigma (CT-$\triangle\Sigma$) analog-to-digital converters (ADCs) have been extensively investigated for their use in wireless receivers to achieve conversion bandwidths greater than 15 MHz and higher resolution of 10 to 14 bits. This dissertation investigates the current state-of-the-art high-speed single-bit and multi-bit Continuous-time Delta-Sigma modulator (CT-$\triangle\Sigma$M) designs and their limitations due to circuit non-idealities in achieving the performance required for next-generation wireless standards. Also, we presented complete architectural and circuit details of a high-speed single-bit and multi-bit CT-$\triangle\Sigma$M operating at a sampling rate of 1.25 GSps and 640 MSps, respectively (the highest reported sampling rate in a 0.13 μm CMOS technology node) with measurement results. Further, we propose a novel hybrid $\triangle\Sigma$ architecture with two-step quantizer to alleviate the bandwidth and resolution bottlenecks associated with the contemporary CT-$\triangle\Sigma$M topologies. To facilitate the design with the proposed architecture, a robust systematic design method is introduced to determine the loop-filter coefficients by taking into account the non-ideal integrator response, such as the finite opamp gain and the presence of multiple parasitic poles and zeros. Further, comprehensive system-level simulation is presented to analyze the effect of two-step quantizer non-idealities such as the offset and gain error in the sub-ADCs, and the current mismatch between the MSB and LSB elements in the feedback DAC. The proposed novel architecture is demonstrated by designing a high-speed wideband 4^{th} order CT-$\triangle\Sigma$ modulator prototype, employing a two-step quantizer with 5-bits resolution. The proposed modulator takes advan-

tage of the combination of a high-resolution two-step quantization technique and an excess-loop delay (ELD) compensation of more than one clock cycle to achieve lower-power consumption (28 mW), higher dynamic range (>69 dB) with a wide conversion bandwidth (20 MHz), even at a lower sampling rate of 400 MHz. The proposed modulator achieves a Figure of Merit (FoM) of 340 fJ/level.

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LIST OF ABBREVIATIONS

– ADC Analog-to-Digital Converter

– RF Radio-Frequency

– LNA Low-Noise Amplifier

– VGA Variable Gain Amplifier

– AAF Anti-Aliasing Filter

– DR Dynamic Range

– DSP Digital Signal Processing

– ASIC Application-Specific Integrated Circuit

– CT Continuous-Time

– SNDR Signal-to-Noise and Distortion ratio

– BW Bandwidth

– $\triangle\Sigma$ Delta-Sigma

– OSR Oversampling Ratio

– SC Switched Capacitor

– MDAC Multiplying Digital-to-Analog Converter

– SHA Sample-and-Hold

– FoM Figure of Merit

– GSM Global System for Mobile

– GPRS General Packet Radio Service

– EDGE Enhanced Data Rates for GSM

– W-CDMA Wideband Code Division Multiple Access

– CDMA2000 Code Division Multiple Access 2000

– TD-SCDMA Time Division Synchronous Code Division Multiple Access

– DT Discrete-Time

– CT-$\triangle\Sigma$ Continuous-Time Delta-Sigma

– IIT Impulse-Invariant Transformation

– T_s Sampling Period

– LSB Least-Significant Bit

– FS Full-Scale

– PDF Probability Density Function

– PSD Power Spectral Density

– SQNR Signal-to-Quantization Noise Ratio

– ENOB Effective Number of Bits

– STF Signal Transfer Function

– NTF Noise Transfer Function

– IBN In-band Quantization Noise

– OBG Out-of-Band Gain

– MSA Maximum Stable Amplitude

– ELD Excess-Loop Delay

– PVT Process, Voltage and Temperature

– CIFF Distributed Feed-Fordward Summation

– CIFB Distributed Feedback Summation

– NRZ Non Return-to-Zero

– RZ Return-to-Zero

– SCR Switched-Capacitor Resistor

– DRS Dynamic Range Scaling

– B Quantizer Resolution

– N Order of the Filter

– DEM Dynamic Element Matching

– SNR Signal-to-Noise Ratio

– TDC Time-to-Digital Converter

– VCO Voltage-Controlled Oscillator

– Opamps Operational Amplifiers

– ITF Integrator Transfer Function

– GBW Gain Bandwidth Product

– SJNR Signal-to-Jitter Noise Ratio

– PLL Phase-Locked Loops

– ABCD State-Space Matrices

– CM Common-Mode

– SF -3σ Variation on NMOS and PMOS and $+3\sigma$ variation on Resistor

– A_{dc} Open-Loop DC Gain

– SAFF Sense-Amplifier Based Flip-Flop

– SR Slave Set-Reset

– PCB Printed Circuit Board

– LDO Low Dropout

– EMI Electromagnetic Interference

– DUT Design Under Test

– FA Full-Adder

– DDA Differential Difference Amplifier

– DNL Differential Non-Linearity

– ECF Error Correction Factor

– LVDS Low-Voltage Differential Signaling

– MSB Most Significant Bit

– DWA Data-Weighted Averaging

– S/H Sample-and-Hold

– T/H Track-and-Hold

CHAPTER 1

INTRODUCTION

An analog-to-digital converter (ADC) is an essential block in many of today's wireless communications systems. A simplified block diagram of a typical receiver chain, used in a wireless communication system, is shown in Figure 1.1 [1]. The antenna receives an incoming radio-frequency (RF) signal and processes it through an RF filter to remove the out of band signal content [2, 3, 4]. Then, the filtered RF signal is amplified using a low-noise amplifier (LNA), which is designed to amplify the signal while adding as low noise and distortion as possible [2]. The output of the LNA is then down-converted to baseband using a mixer and amplified through a variable gain amplifier (VGA) [2, 3, 4]. Then, the amplified signal from VGA is further bandlimited using an anti-aliasing filter (AAF) and then digitized by an ADC [5, 6]. The ADC provides sufficient dynamic range (DR) for the subsequent digital-signal processing (DSP) algorithms to demodulate the digital data while meeting the performance metrics mandated by the wireless communication standard [1, 7]. The DSP tasks such as channel equalization and clock recovery, demodulation, and error-control coding are performed on a dedicated digital platform, such as a DSP processor or a customized application-specific integrated circuit (ASIC) [3, 8].

As the ADC plays a vital role in interfacing the real-world analog signals with the programmable abstraction of a DSP platform, the correct choice of ADC is critical

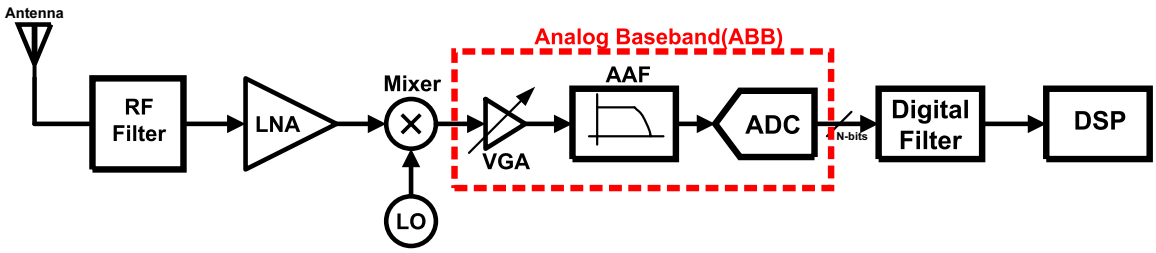

Figure 1.1: Typical digital communication receiver path.

for overall system performance and energy efficiency. In general, the conversion of a continuous-time (CT) analog signal into its digital representation involves unavoidable errors due to limited resolution of the quantizer, device thermal and flicker noise, sampling clock jitter, and circuit non-idealities that degrade the ADC performance. It is important to understand the effect of noise and non-idealities introduced by the ADC in order to meet the desired specifications dictated by the system-level architecture. Overall, the dynamic performance of the ADC is critical in a wireless receiver and plays a direct role in determining the overall sensitivity and accuracy of the receiver [1, 5, 9].

1.1 Motivation

In recent years, continuous CMOS technology scaling has sustained rapid improvements in the processing speed of radio-frequency front-end circuits, ADC interfaces, and DSP platforms [10]. This has paved the way for innovative system architectures facilitating new wireless communication standards that provide higher data rates with improved energy-efficiency, such as the 5G networks and IEEE 802.11 a/b/g/n/ac wireless LANs [10]. These have been enabled by the ability to infuse smarter algorithms, more efficient DSPs, highly-optimized hardware accelerators, and smarter

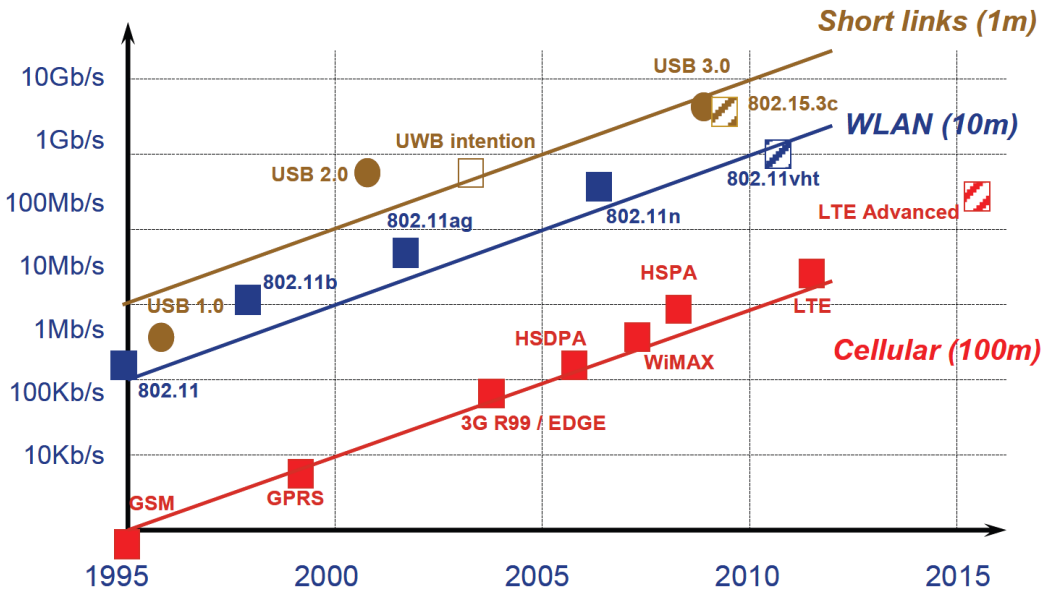

Figure 1.2: Data rates for Wired and Wireless applications over time [10] .

hardware-software partitioning systems, all on the same chip [10].

Figure 1.2 shows the evolution of data rates for wired and wireless applications over past few decades. The trend in Figure 1.2 clearly reveals that cellular links, wireless LANs, as well as short links consistently show a $10\times$ increase in data rates every five years without any degradation in throughput [4, 10]. Sustaining this trend of improvement in next-generation wireless communication standards calls for even higher conversion bandwidth ($> 150\,MHz$) while providing higher signal-to-noise and distortion ratio ($SNDR > 74\,dB$), while maintaining energy-efficiency from the ADC architectures intended for battery powered hand-held wireless devices [4].

Figure 1.3 depicts the classification of ADC architectures based upon their SNDR and conversion bandwidth (BW) specifications [11]. Further, Figure 1.4 shows the energy consumption (in pJ per sampling rate) vs SNDR, for Nyquist rate as well as oversampling ADCs compiled from the IEEE ISSCC and VLSI conferences [11]. As

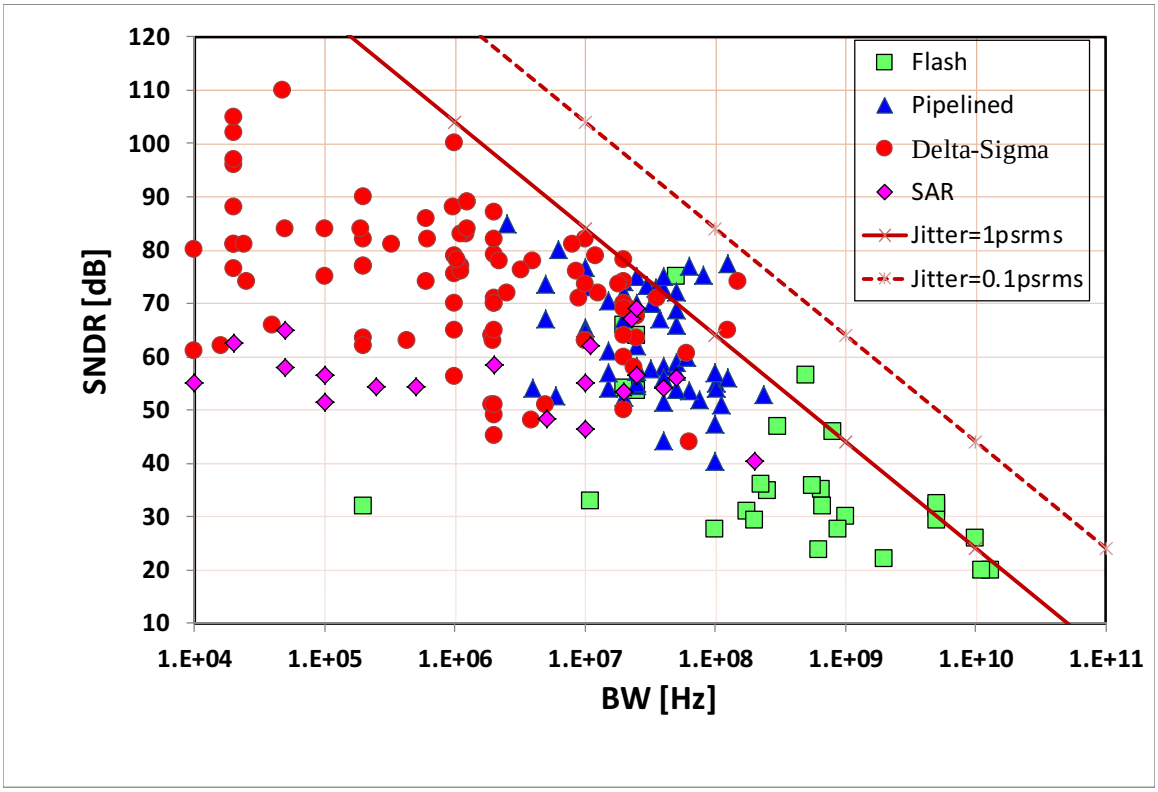

Figure 1.3: SNDR vs conversion bandwidth of different classification of ADCs [11].

illustrated in Figure 1.3, the fundamental limitation on the achievable ADC SNDR is set by the sampling clock jitter and thermal noise contributed by the circuits [5, 6].

In general, for the scaled CMOS technologies in the nanometer regime, Flash ADCs have been used for lower resolution (4-6 bits) and higher-speed data conversion with Nyquist sampling rates ranging from 100's of MHz to several GHz's [12, 13]. Continuous CMOS scaling directly benefits Flash ADCs to easily realize higher sampling rates up to a few GHz. However, the nano-CMOS technologies are more prone to process variations and poor component matching on-chip [14, 15]. Also, the circuit complexity and power consumption of Flash ADC increases exponentially for every $1-$bit increase in resolution [12, 13]. Thus, the available resolution of a Flash ADC is limited to $5-6$ bits, which is clearly shown in Figure 1.3.

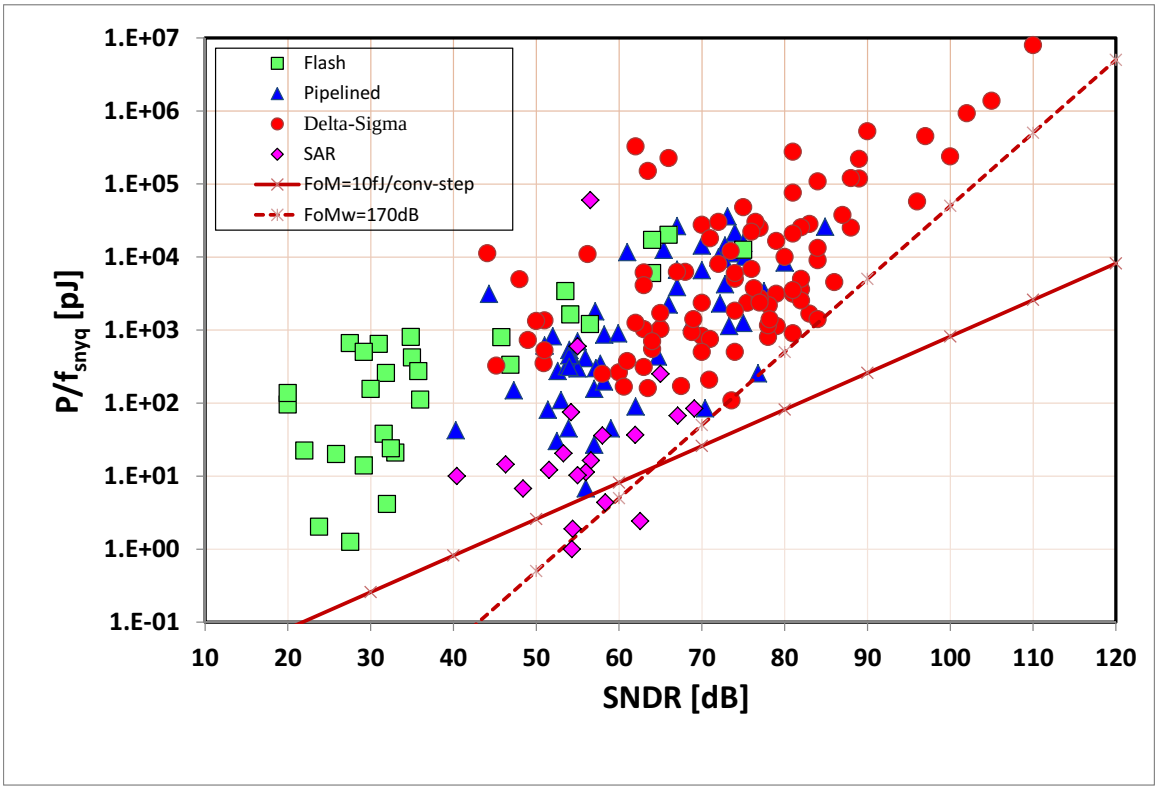

Figure 1.4: Energy consumption (in pJ per sampling rate) vs SNDR of different classification of ADCs [11].

The commonly preferred ADC architectures in a wireless receiver chain are the pipeline ADCs [4, 5, 16] and the Oversampling or Delta-Sigma ($\Delta\Sigma$) ADCs [17, 18, 19]. In general, each of these architectures has its own distinct advantages and targeted applications. In wireless systems with high bandwidth requirements, pipeline ADCs have been traditionally employed in the past, due to their relatively wide conversion bandwidth (up to 100 MHz) with moderate resolution (8-12 bits) while employing a low oversampling ratio (OSR) (e.g., 2 or 4) [5]. This can be observed in the ADC architecture trends from Figure 1.3 [11]. However, a pipeline ADC is implemented using switched capacitor (SC) multiplying digital-to-analog converter (MDAC) stages that require a precise closed-loop gain. Therefore, it necessitates a high open-loop

gain requirement for the opamps while achieving desired settling accuracy from the MDAC stages and tight matching from the capacitors [5, 6]. Thus, it poses challenges in scaled nano-CMOS technologies where the maximum open-loop gain available from the transistors is constantly deteriorating along with the shrinking voltage headroom and pronounced device variations. In order to compensate for the resulting circuit non-idealities, pipelined ADCs designed in nano-CMOS technologies require complex digital calibration circuitry [20, 21]. This digitally assisted analog paradigm results in significant increase in digital design complexity, calibration latency and convergence delays, power consumption, and silicon real estate. Also, the pipelined ADCs typically present a large input capacitance, determined by the thermal noise budget in the sample-and-hold (SHA) stage, to achieve the specified dynamic range [5, 6, 20, 21]. This increased input capacitance increases the power and design complexity of the AAF and an input buffer capable of driving the large input capacitance, which can be further explained by comparing Figure 1.3 with Figure 1.4.

Though the pipelined ADC can, in principle, achieve better resolution than some oversampling ADCs in Figure 1.3, their figure of merit (FoM) is highly limited due to their higher power consumption, as illustrated in Figure 1.4 [11]. On the other hand, $\Delta\Sigma$ ADC's architecture is becoming an attractive candidate compared to the pipelined ADC architecture, as they trade higher DSP for relaxed performance requirements from the analog components [11, 17, 18, 22, 23]. This is a favorable trade-off in nano-CMOS technologies where digital is inexpensive to implement and employs well-established digital decimation filters architectures [24].

Figures 1.3 and 1.4 clearly illustrate that the $\Delta\Sigma$ ADCs are also suitable for high-resolution and low-to-medium bandwidth applications by employing quantization noise-shaping along with oversampling [11]. Further, $\Delta\Sigma$ ADCs are gaining

wider acceptance in wireless applications due to several desirable features including relaxed AAF requirements due to oversampling, higher achievable DR (>70 dB), and low-power digital friendly implementation [19, 25, 26]. Both the 2^{nd} generation (e.g., GSM, GPRS, and EDGE) and the 3rd-generation (e.g., WCDMA, CDMA2000, and TD-SCDMA) cellular systems widely started using $\Delta\Sigma$ ADCs in their cell phone receivers [27, 28]. Also, the $\Delta\Sigma$ ADCs are a good match for other wireless applications including Bluetooth, digital FM, Zigbee, and IEEE 802.11 wireless LANs [23, 27, 28, 29].

Most of the contemporary commercial $\Delta\Sigma$ ADCs, intended for wireless applications, have been implemented using switched-capacitor (SC) circuit techniques, also known as discrete-time (DT)-$\Delta\Sigma$ ADCs. This was primarily due to the confluence of mature methodologies for SC design and robustness in the presence of process variations [30, 31]. Even though the design methodologies for SC or DT-$\Delta\Sigma$ ADCs are well-established and easy to scale with technology, the maximum achievable sampling rate is restricted to a few 100 MHz's. These restrictions arise from the settling speed and accuracy requirements from the opamps employed in the SC integrators, which are difficult to design with a reasonable power budget with a sampling rate greater than $300 - 400$ MHz, even in scaled CMOS technologies. Compared to their DT counterparts, continuous-time delta-sigma (CT-$\Delta\Sigma$) ADCs have the distinct advantage of higher speed and/or lower power consumption [17, 18, 32, 33]. The absence of stringent settling requirements on the opamps enables CT-$\Delta\Sigma$ ADCs to achieve sampling rates up to several GHz's with steadily improving conversion bandwidths [17, 18].

Continuous-time $\Delta\Sigma$ modulators further offer several unique features that greatly reduce the challenges in design of ADCs for systems that simultaneously require

wider conversion bandwidths ($>$ 25 MHz) and higher dynamic range performance ($>$ 70 dB):

- The inherent power-efficient architecture eliminates the need for high settling speed opamp stages essential for sampled-input ADCs, such as the pipeline or traditional DT-$\Delta\Sigma$ ADCs [19, 26].

- A built-in AAF feature realized by the internal low-pass continuous-time loop-filter combined with oversampling [19, 26, 34] greatly relaxes the performance requirements from an external AAF, if one is needed at all. This is the single most important factor in the growing adoption of CT-$\Delta\Sigma$ ADCs in commercial products [18, 23].

- A purely resistive and constant input impedance, as opposed to the time-varying input impedance presented by a sampling switch, makes it easier to be driven by a preceding stage such as a VGA in the receiver chain. Further, lack of periodically switching components in the loop-filter injects significantly reduced substrate and supply noise into the overall system, resulting in quieter operation and low spurious tone (spur) power levels [32, 33].

- The relaxed bandwidth requirements for the loop-filter opamps, operating in continuous-time, results in overall lower power consumption when compared to their corresponding discrete-time counterparts [32, 33].

- Due to the continuous-time operation of the loop-filter, input-signal sampling errors such as the sampling aperture error, error due to incomplete opamp settling, charge injection, and other switched-capacitor specific degradations do not exist in continuous-time circuits [19, 26]. Further, the error induced due

to the sampling jitter in the flash quantizer is shaped and reduced by the $\Delta\Sigma$ feedback loop.

Due to the above desirable features offered by CT-$\Delta\Sigma$ ADCs, when compared to the DT-$\Delta\Sigma$ ADCs, they are gaining wider interest in upcoming wireless applications such as IEEE 802.11ac+ WLAN and IEEE 802.16e Mobile Wimax for their lower power consumption, wider conversion bandwidth ($\geq$ 10 MHz), and ease of integration in nano-CMOS technologies [11, 17, 18, 22]. Every stage of development of next-generation wireless standards, as illustrated in Figure 1.2, demand more performance requirements from these ADCs, in terms of resolution (or dynamic range), bandwidth and power consumption. For example, upcoming standards such as 802.11ac extensions demand up to 160 MHz of conversion bandwidth while maintaining dynamic range greater than 60 dB [18].

This work focuses on several aspects of designing high-speed CT-$\Sigma\Delta$ ADCs in order to achieve higher conversion BW ($>$ 15 MHz) and DR ($>$ 60 dB) for the available 130 nm CMOS technology by consuming very low power ($<$ 20 mW) for these applications. First, the complete system and circuit-level design aspects for optimized single-bit and multi-bit CT-$\Delta\Sigma$ ADCs operating at speeds and performance comparable with the state-of-the-art are presented and discussed, with techniques for addressing several design challenges as well as their solutions substantiated with measurement results. Then, a novel architecture is proposed and analyzed for realizing wideband CT-$\Delta\Sigma$ ADCs suitable for next-generation wireless applications by utilizing low OSR and higher resolution multi-step quantizers at low sampling frequency. A fourth-order CT-$\Delta\Sigma$ ADC, employing a two-step quantizer, is presented to illustrate the concept and its chip-level implementation is detailed [35, 36, 37].

1.2 Dissertation Organization

This dissertation covers a detailed theoretical analysis of the contemporary as well as the proposed CT-$\Delta\Sigma$ ADCs. The effect of circuit non-idealities and their influence on the performance of the $\Delta\Sigma$ ADC are detailed. Further, the complete system and circuit-level implementations of these modulators are explained with simulation results. Last, the complete hardware prototyping and test procedure for the high-speed prototype chips are presented.

The dissertation has been organized as follows:

Chapter 2 provides a brief background on the oversampling ADCs. Fundamental analytical results along with the synthesis procedure for the discrete-time prototype loop-filter are also presented, which help understand the rest of the dissertation.

Chapter 3 provides an introduction to CT-$\Delta\Sigma$ ADCs and describes the analytical as wells as the numerical approaches to the synthesis of the CT loop-filter, starting from the prototype DT loop-filter, using impulse-invariant transformation (IIT). Further, prominent design challenges involved in a CT-$\Delta\Sigma$ ADC are addressed along with their solutions. These include excess loop delay due to the quantizer, errors due to the clock jitter, RC time constant variation due to process shifts effects of finite gain and unity gain frequency of the opamps, and feedback digital-to-analog converter (DAC) non-linearity.

Chapter 4 describes the complete system and circuit-level implementation of a high-speed, ultra-low power energy-efficient single-bit CT-$\Delta\Sigma$ modulator. This chapter also details the noise budgeting, dynamic-range scaling, and complete circuit non-idealities of the modulator performance using system-level simulation (i.e., using *SIMULINK* models) to achieve optimized ultra-low power design. Finally, this

chapter covers the test setup of high-speed prototype ADC testing with chip results.

Chapter 5 describes the complete system and circuit-level implementation of high-speed, low-power multi-bit CT-$\Delta\Sigma$ modulator. It describes a detailed multi-bit quantizer (i.e., Flash ADC and DAC), non-idealities on modulator performance using system-level simulation. Also, it demonstrates and discusses the circuit-level implementation of each block in detail. Finally, measurement results from the prototype chip are presented.

Chapter 6 demonstrates the first hybrid novel high-speed, energy-efficient multi-step quantizing CT-$\Delta\Sigma$ modulator, using a 5-bit two-step quantizer. The complete systematic synthesis procedure of the CT loop-filter is introduced to determine the loop-filter coefficients by taking into account the non-ideal integrator response, such as finite opamp gain and the presence of multiple parasitic poles and zeros for ELD compensation greater than one clock cycle. Further, it discusses the behavior modeling and system-level simulation to analyze the effect of quantizer non-idealities such as offset and gain error in the two-step sub-ADC, and current mismatch between the MSB and LSB elements in the DAC to simulate the performance limitation of the proposed modulator. Finally, measurement results from the prototype chip are presented.

Chapter 7 concludes the dissertation and discusses future directions for this research.

1.3 Unique Contributions

- The complete design flow with system-level optimization and circuit-level innovation in single- and multi-bit CT-$\Delta\Sigma$ ADCs for large conversion bandwidth.

The modulator is demonstrated at highest speeds in 130 nm CMOS for bandwidth greater than 15 MHz with a DR greater than 60 dB.

- The first Hybrid CT-$\Delta\Sigma$ architecture is proposed with an architectural innovation for large bandwidth (low-OSR) designs and demonstrated proof of concept in 130 nm CMOS technology.

CHAPTER 2

OVERVIEW OF OVERSAMPLING ANALOG-TO-DIGITAL CONVERTERS

This chapter presents an overview of the Oversampling or $\Delta\Sigma$ ADCs to set the stage for rest of the dissertation. Further, fundamental concepts such as quantization, oversampling and noise-shaping are introduced in this chapter and illustrated with analytical results. Also, the procedure for synthesizing discrete-time $\Delta\Sigma$ modulators is detailed, which forms the basis for discussion in the remaining chapters.

2.1 Quantization

As discussed in the previous chapter, an ADC is employed to convert real-world analog signals, which are continuous in time and amplitude, into its sampled (discrete-time) and digital (discrete-amplitude) representation. Conversion of a continuous-time analog signal into digital is carried out in two steps. The analog input is first sampled-and-held for a sufficient fixed time or the sampling period (T_s). Then, the sampled and held signal is quantized, where it is represented by one of the fixed discrete or quantized levels with the separation depending upon the resolution of the ADC. The block that performs this quantization operation is called a *quantizer*.

Figure 2.1 shows the simple block diagram of a sampler operating at a clock rate f_s, followed by the quantizer. Here, $X_{in}(t)$ is a continuous-time and continuous-amplitude

input signal, which is sampled to result in a discrete-time but continuous amplitude signal, $X_{in}[nT_s]$. The uniform quantizer "bins" $X_{in}[nT_s]$ into $M-$discrete-levels that are digitally represented by B-bit wide words ($B = log_2(M)$), which set the maximum achievable resolution of the ADC [5, 6, 19].

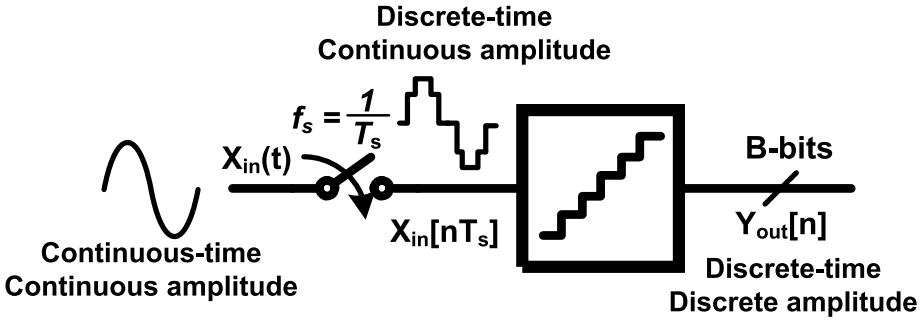

Figure 2.1: Block diagram showing the conversion of an analog input signal to its digital representation.

The quantizer can be understood as a memoryless non-linear block defined by its input/output characteristics (i.e., x-y transfer curve) [19, 38]. An example of quantizer input/output characteristics is shown in Figure 2.2(a), where the number of quantization levels is 4 and thus the quantized output signal can be represented as a 2-bit binary code [19, 38]. The step size or the difference of two adjacent quantized input levels, $\triangle_{LSB}$, is known as least-significant bit or LSB size. Also, the difference between the lowest and highest input levels is called the full-scale (FS) of the quantizer, given by $2\,V_{Ref}$ in Figure 2.2(a).

The deviation between the sampled input and the quantized output is called the quantization error or quantization noise (e_q). Figure 2.2(b) shows the relationship between the e_q and the input X_{in}. From this figure, it can be seen that as long as the input X_{in} is confined between $-\left(\frac{V_{Ref}+V_{LSB}}{2}\right)$ and $+\left(\frac{V_{Ref}+V_{LSB}}{2}\right)$, the error, e_q,

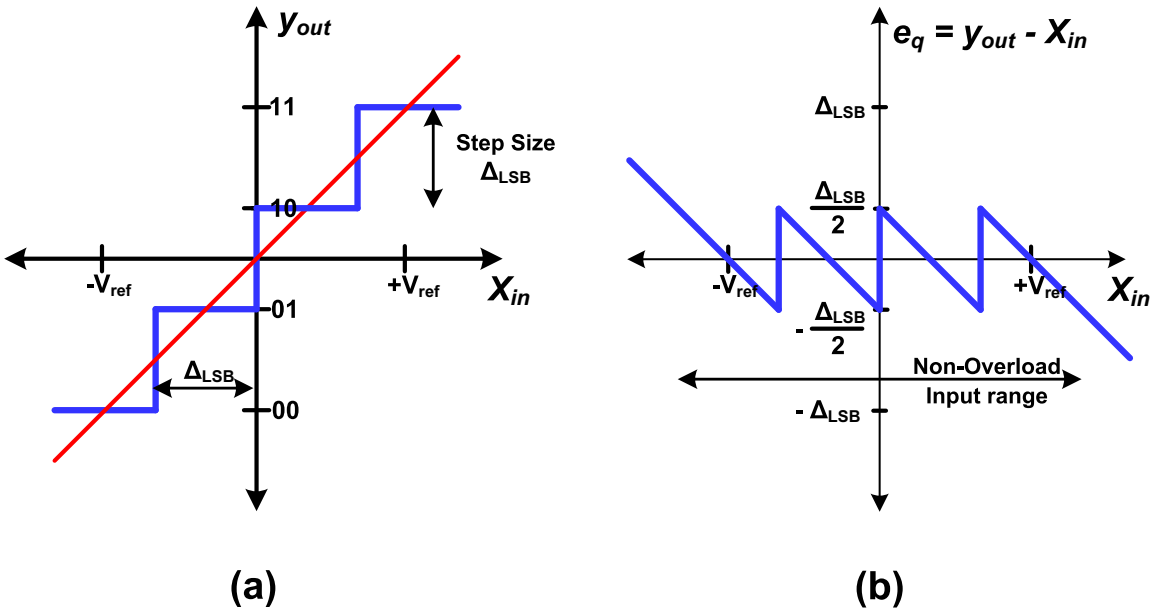

Figure 2.2: (a) Transfer curve and (b) Error Function of 2-bit Quantizer.

is bounded between $-\frac{V_{LSB}}{2}$ and $+\frac{V_{LSB}}{2}$. The range of X_{in} where this condition is satisfied is called the non-overload input range. For an N-bit ADC, the LSB size is given by Equation 2.1.

$$\triangle_{LSB} = \frac{FS}{2^N} = \frac{(V_{ref} - (-V_{ref}))}{2^N} \tag{2.1}$$

In order to define some important properties of the quantizer, it is necessary to estimate quantization noise power, or the mean square value of the quantization noise. As the quantizer is a deterministic block, the output, y, is a function of $X_{in} \pm e_q$. Thus, the value of the error is primarily determined by the input [19, 38, 39]. If we assume that the input changes randomly between the samples and the amount of change is comparable with or greater than the LSB-size, without causing quantizer overloading, then the error, e_q, is largely uncorrelated from sample to sample and has equal probability of lying anywhere in the range of $\pm\frac{\triangle_{LSB}}{2}$ [19, 38, 39].

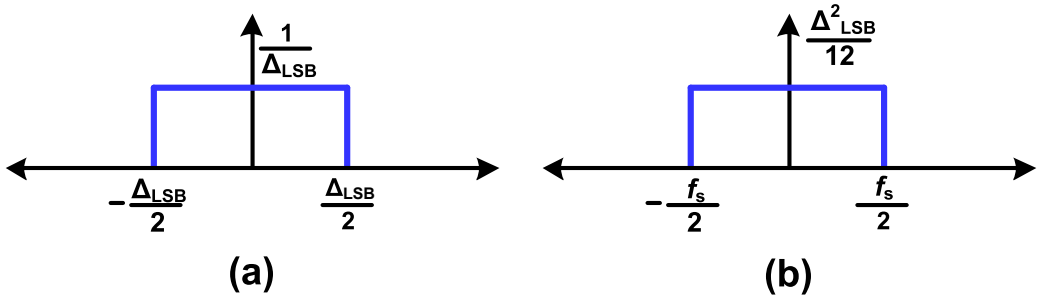

Figure 2.3: (a) Probability density function (PDF) and (b) Power spectral density (PSD) of the quantization noise.

Further, if the quantization error is modeled as a wide sense stationary random process and independent of the input signal, then it can be represented as a white noise process with samples uniformly distributed between $\pm\frac{\triangle_{LSB}}{2}$ [19, 38, 39]. Therefore, the probability density function (PDF) of the quantization noise is given as $e_q \sim U[-\frac{\triangle_{LSB}}{2}, \frac{\triangle_{LSB}}{2}]$, and is illustrated in Figure 2.3(a). Further, the power spectral density (PSD) of the quantization noise is approximated to be flat in the Nyquist frequency band $f \in [-\frac{f_s}{2}, \frac{f_s}{2}]$ as shown in Figure 2.3(b). The quantization noise power (σ_e^2) is calculated from Figure 2.3 as

$$\sigma_e^2 = \frac{1}{\triangle_{LSB}} \int_{-\frac{\triangle_{LSB}}{2}}^{\frac{\triangle_{LSB}}{2}} x^2 e_q(x) dx = \frac{\triangle_{LSB}^2}{12} \tag{2.2}$$

The impact of the quantization noise on the ADC dynamic performance is found by calculating its maximum signal-to-quantization-noise ratio (SQNR). This parameter is obtained by dividing the power of a full-scale sinusoidal input signal with quantization noise power [5, 6, 40]. The maximum amplitude without causing overloading of the ADC is $2^N \triangle_{LSB}$ and the average power of the sine wave is calculated as

$$P_{sig} = \frac{\left(2^{N-1} \triangle_{LSB}\right)^2}{2} \tag{2.3}$$

The maximum SQNR of an ideal ADC with a sinusoidal input signal is estimated as

$$SQNR_{max} = \frac{Maximum\,Signal\,Power}{Quantization\,Noise\,Power} = \frac{P_{sig}}{\frac{\triangle_{LSB}^2}{12}} = \frac{3}{2} \cdot 2^{2N} \tag{2.4}$$

Further, the above Equation 2.4 is expressed in dB as Equation 2.5, which is widely used to characterize the dynamic performance of an ADC [5, 19].

$$SQNR_{max,dB} = 6.02N + 1.76 \tag{2.5}$$

The above equation is inverted as Equation 2.6, which is used to estimate the effective number of bits (ENOB) or N_{eff} of an ADC. N_{eff} is also a measure of the effective resolution of the ADC.

$$N_{eff} = \frac{SQNR_{max,dB} - 1.76}{6.02} \tag{2.6}$$

2.2 Oversampling

From Figure 2.3, it is evident that the quantization noise power is uniformly distributed from $\left[-\frac{f_s}{2}, \frac{f_s}{2}\right]$, where $f_s\,(= 2.BW)$ is the Nyquist sampling frequency of the quantizer and BW is the conversion bandwidth of the input signal. However, by employing oversampling (i.e., $f_s = 2 \cdot OSR \cdot BW$), and filtering the output of the ADC to the desired bandwidth as shown in the Figure 2.4, the quantization noise power in the signal bandwidth (i.e., the bandwidth of interest) is reduced [19, 38, 39]. This results in a moderate improvement in the ADC resolution. In order to calculate

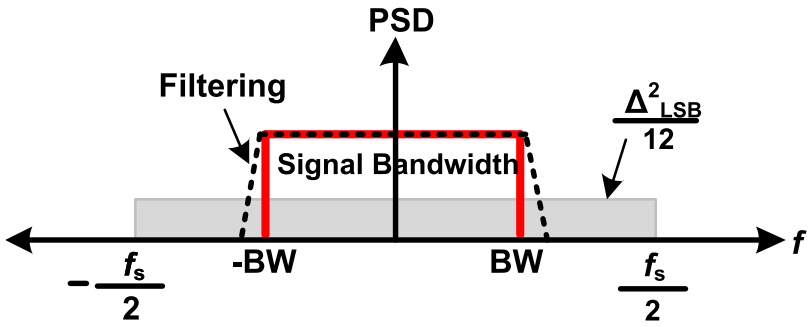

Figure 2.4: Effect of Oversampling on PSD of Quantization noise.

the effective quantization noise power in the signal band, the power spectral density of quantization noise is integrated over the bandwidth of the ADC as [19, 38, 39]

$$INB_{\sigma_e^2} = \frac{1}{f_s}\int_{-BW}^{BW} \sigma_e^2 df = \sigma_e^2 \frac{2BW}{f_s} = \frac{\sigma_e^2}{OSR} \tag{2.7}$$

The above equation clearly reveals that there is a decrease in quantization noise power in the signal band when compared to Equation 2.2. Further, the maximum SQNR can be calculated by assuming signal power as in Equation 2.3

$$SQNR_{max}\,(dB) = 6.02N + 1.76 + 10log_{10}OSR \tag{2.8}$$

From Equation 2.8, it is clear that if the sampling rate, f_s, is equal to twice the Nyquist rate (i.e., $OSR = 2$), the SQNR is improved by $3\,dB$. In other words, for every doubling of OSR, SQNR improves by $3\,dB$, or $0.5\,bits$ [19, 38, 39].

2.3 Quantization Noise Shaping

As discussed in the previous section, the oversampling trades a higher sampling frequency compared to Nyquist bandwidth to achieve higher SQNR. However, for

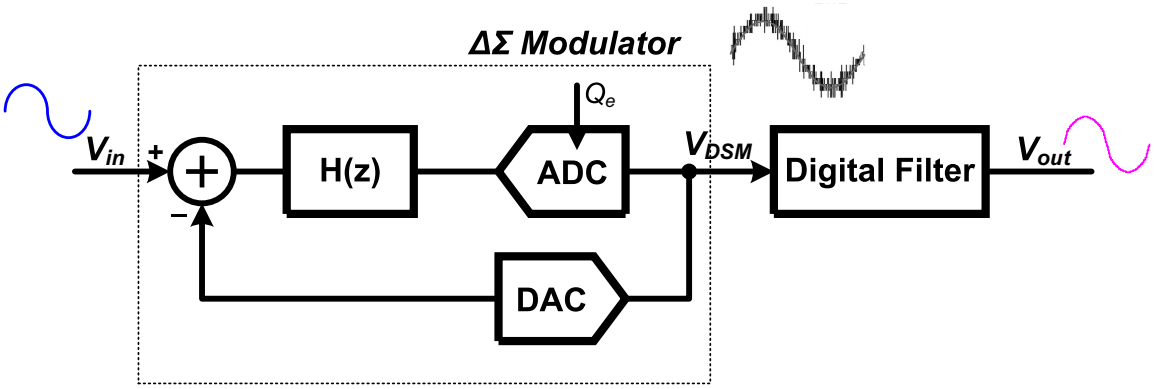

Figure 2.5: Operation of an ADC employing ΣΔM.

every doubling of OSR, an SQNR enhancement of only $3\,dB/octave$ is achieved. In order to make use of oversampling in a more efficient way, a negative feedback loop with a frequency dependent gain is employed to attenuate the in-band quantization noise, as shown in Figure 2.5 [19, 38, 39]. As a consequence, the effective quantization noise is significantly reduced in the signal band while the out-of-band quantization noise is amplified. This form of signal processing is called noise-shaping and forms the basis of ΔΣ modulation [5, 19].

Figure 2.5 shows the simplified block diagram and motivation behind a ΔΣ modulator. Here, a low-resolution ADC and DAC is employed in a feedback loop comprising of a loop filter, $H(z)$. By employing oversampling along with the feedback loop with a frequency dependent low-pass gain element, $H(z)$, the quantization noise from the low-resolution ADC, $Q_e(z)$, is high-pass filtered to yield lower quantization noise power in the signal bandwidth. Thus, the noise-shaping results in a lower quantization noise in the signal bandwidth and the modulated out-of-band, high-frequency noise can be filtered out digitally, leading to a much higher in-band SQNR. Thus, much of the analog-signal processing in the ADC is transferred to the digital domain, which is favorable in scaled CMOS technologies. A ΔΣ ADC is comprised of a ΔΣ modulator

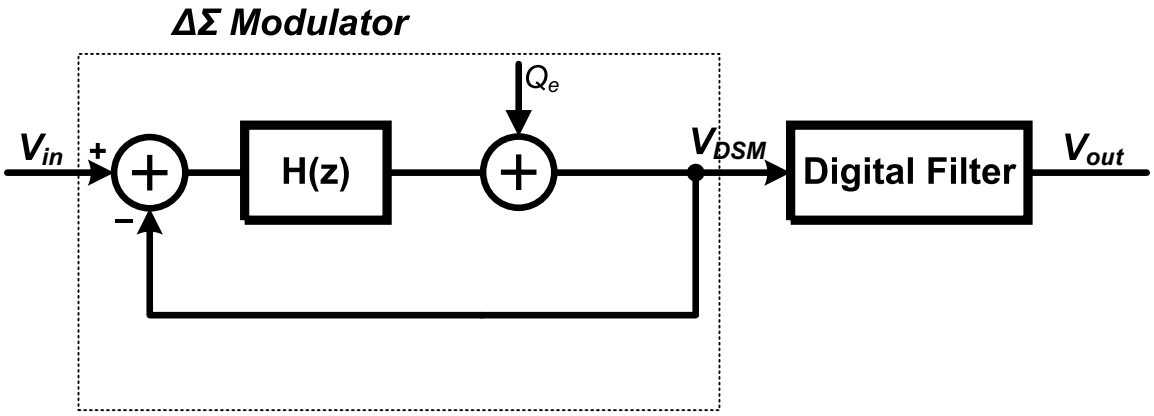

Figure 2.6: Simplified block diagram of ΣΔM shown in Figure2.5.

followed by the digital decimation filter stages [19]. Since the design methodology for the decimation filters is well-established, we are primarily concerned with the mixed-signal design challenges involved in the $\Delta\Sigma$ modulator. It must be noted that in circuits literature, $\Delta\Sigma$ ADC and $\Delta\Sigma$ modulator are used interchangeably to describe the same data-conversion system.

The fundamental advantage of the $\Delta\Sigma$ ADC is that it can independently achieve noise-shaping and resulting higher SQNR without affecting the signal content in the desired signal band. To analyze the $\Delta\Sigma$ modulator shown in Figure 2.5, the quantizer block is replaced with its linearized model, which is essentially a linear gain block with additive quantization noise, as shown in Figure 2.6 [19, 38]. The resulting system-level block diagram has two inputs, $V_{in}(z)$ and $Q_e(z)$, and one output, V_{DSM}. The transfer function from V_{in} to V_{DSM} is called the signal-transfer function (STF) and is given by

$$STF\left(z\right) = \frac{V_{DSM}\left(z\right)}{V_{in}\left(z\right)} = \frac{H\left(z\right)}{1 + H\left(z\right)} \tag{2.9}$$

Similarly, the transfer function from Q_e to V_{DSM} is called the noise-transfer

function (NTF) and is given by

$$NTF\left(z\right)=\frac{V_{DSM}\left(z\right)}{Q_e\left(z\right)}=\frac{1}{1+H\left(z\right)} \tag{2.10}$$

To achieve first-order noise-shaping, consider using a loop-filter $H\left(z\right)=\frac{z^{-1}}{1-z^{-1}}$, then $V_{DSM}\left(z\right)$ can be rewritten as

$$V_{DSM}\left(z\right)=z^{-1}V_{in}\left(z\right)+\left(1-z^{-1}\right)Q_e\left(z\right) \tag{2.11}$$

This implies that the output signal, $V_{DSM}\left(z\right)$, is the combination of the input signal $V_{in}\left(z\right)$, which is delayed and appears to be unaltered at the output V_{DSM}, in addition to the first-order noise-shaped quantization noise. The order of noise-shaping is associated with the order of the NTF. In order to exactly understand the effect of the first-order noise-shaping $\Delta\Sigma$ modulator on its SQNR, the power spectral density of the quantization noise at the output, V_{DSM}, is calculated by multiplying σ_e^2 with the squared magnitude of the NTF (i.e., $\left|NTF\left(e^{j\Omega}\right)\right|^2$). Here Ω is the normalized angular frequency defined as $2\pi f/f_s$ [19, 38]. The power of the in-band quantization noise (IBN) within the signal bandwidth is given by

$$INB_{\sigma_e^2}=\frac{1}{2\pi}\int_{-\Omega_B}^{\Omega_B}\sigma_e^2|NTF\left(z\right)|^2d\Omega=\frac{1}{\pi}\int_{0}^{\pi/OSR}\sigma_e^2\left(2sin\left(\frac{\Omega}{2}\right)\right)^2d\Omega \tag{2.12}$$

By assuming that the OSR is sufficiently large, such that $\Omega_B=\frac{\pi}{OSR}$ is much smaller than 1, then the $2sin\left(\frac{\Omega}{2}\right)$ term in the above Equation 2.12 can be simplified as Ω. Therefore, Equation 2.12 can rewritten as [19]

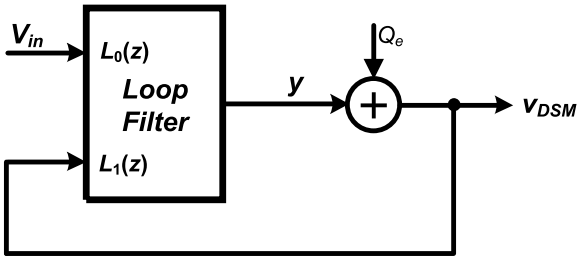

Figure 2.7: General block diagram of single-loop ΣΔM.

$$INB_{\sigma_e^2} = \frac{\sigma_e^2}{\pi} \int_0^{\pi/OSR} (\Omega)^2 \, d\Omega = \frac{\sigma_e^2 \pi^2}{3OSR^3} \tag{2.13}$$

Using the above in-band quantization noise power and the signal power from Equation 2.3, the maximum SQNR (dB) can be calculated as [19, 38]

$$SQNR_{max}\,(dB) = 6.02N + 1.76 + 30log_{10}OSR - 10log_{10}\frac{\pi^2}{3} \tag{2.14}$$

By comparing the above results with Equation 2.8, it is obvious that by combining oversampling with first-order noise-shaping, we can effectively triple the increase in resolution when compared to plain oversampling, resulting in an SQNR enhancement of $9\,dB/octave$, or equivalently, $1.5\,bit$ per doubling in OSR [19]. It must be noted that the total noise power in the output spectrum from DC to $\frac{f_s}{2}$ is higher than that of a Nyquist-rate data converter. Thus, oversampling with a sufficiently large value of OSR is a must to realize the performance gains from a ΔΣ ADC. However, there is a lower limit on OSR for a given order of a modulator, below which oversampling converters do not provide tangible performance benefits [19].

2.4 Synthesis of Discrete-Time Loop-Filter

The first-order noise-shaping concept can be extended to a higher-order $\Delta\Sigma$ modulator. A generalized block diagram of a DT-$\Delta\Sigma$ modulator is shown in Figure 2.7 [19]. In this figure, the modulator loop-filter has two inputs and its output y can be expressed as a linear combination of inputs V_{in} and V_{DSM} [19]. Using Figure 2.7, we can express this relationship as as follows

$$Y(z) = L_0(z) V_{in}(z) + L_1(z) V_{DSM}(z) \tag{2.15}$$

$$V_{DSM}(z) = Y(z) + Q_e(z) \tag{2.16}$$

Using Equations 2.15 and 2.16, the modulator output $V_{DSM}(z)$ can be expressed as

$$V_{DSM}(z) = STF(z) V_{in}(z) + NTF(z) Q_e(z) \tag{2.17}$$

where

$$STF(z) = \frac{L_0(z)}{1 + L_1(z)} \quad and \quad NTF(z) = \frac{1}{1 + L_1(z)} \tag{2.18}$$

Conversely, from the above Equations for the STF(z) and NTF(z), one can compute the required loop-filters transfer functions, $L_0(z)$ and $L_1(z)$ using

$$L_0(z) = \frac{STF(z)}{NTF(z)} \quad and \quad L_1(z) = 1 - \frac{1}{NTF(z)} \tag{2.19}$$

By appropriately selecting $L_0(z)$ and $L_1(z) = L_d(z)$, a higher-order NTF can be realized while keeping the STF equivalent to just a few delays. For an L^{th}- order

NTF (i.e., $(1-z^{-1})^L$), the in-band quantization noise power over the bandwidth can be calculated using same approach as before and it results as follows [19]

$$INB_{\sigma_e^2} = \frac{\sigma_e^2 \pi^{2L}}{(2L+1)\, OSR^{(2L+1)}} \tag{2.20}$$

The maximum SQNR in dB can be expressed as follows

$$SQNR_{max}\,(dB) = 6.02N + 1.76 + (2L+1)\, log_{10} OSR - 10 log_{10} \frac{\pi^{2L}}{(2L+1)} \tag{2.21}$$

In general, the SQNR will improve with the OSR at a rate of $6L+3\,dB/octave$, or equivalently, $L+0.5\,bit/octave$ with the L^{th}- order noise shaping [19].

2.5 Higher Order Stable NTFs with Optimized Poles/Zeros

To improve the SQNR, higher order NTF (i.e., $(1-z^{-1})^L$) can be realized by placing all the zeros at $z=1$ and the poles at $z=0$. However, it is noted that increasing the order also increases the NTF out-of-band gain (OBG) [19, 39]. In general, the maximum out-of-band gain of a higher order NTF with all zeros at DC and poles at $z=0$ grows exponentially according to $\|NTF\,(z)\|_{f_s/2} = 2^L$.

A large out-of-band gain usually limits the DR of the modulator by reducing the maximum stable input amplitude (MSA). The larger OBG causes more wiggling at the quantizer input, which saturates the quantizer even for smaller inputs and causes irrecoverable quantizer saturation and loop instability. The MSA is referred to as the overload level of the $\Delta\Sigma$M. Thus, to utilize the benefit of a higher SQNR from a higher order NTF, it is necessary to reduce OBG while maintaining high in-band noise

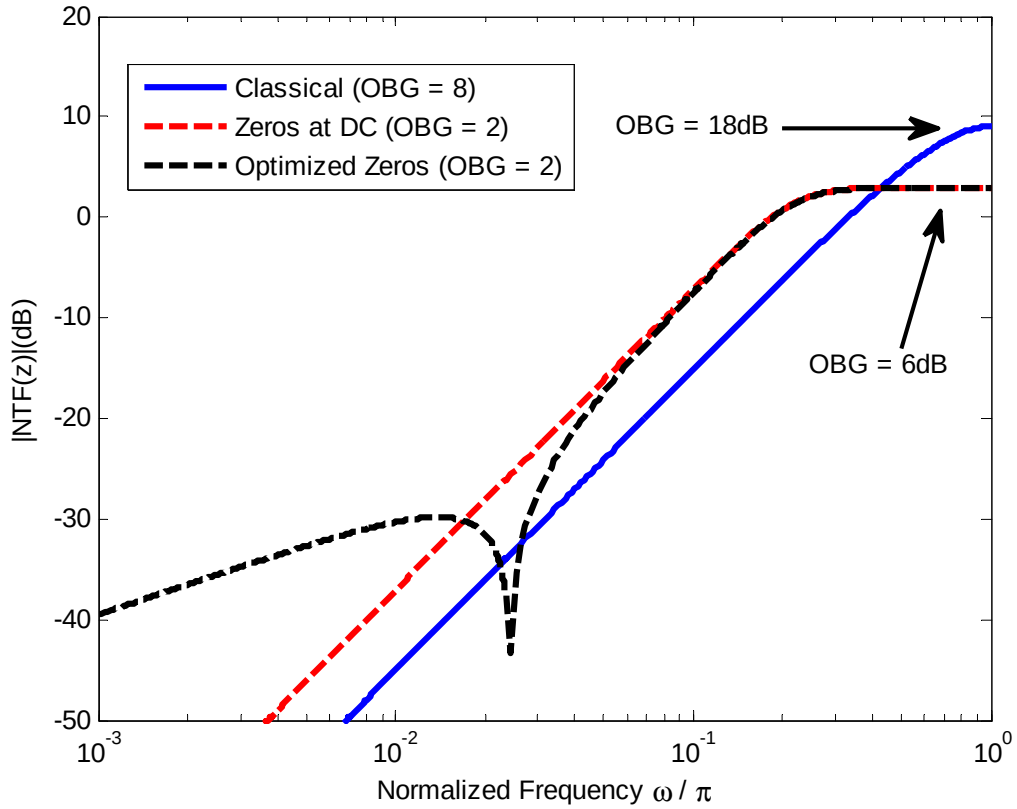

Figure 2.8: 3^{rd}- order NTF design comparison showing the effect of pole/zero placement on the out-of-band gain and in-band noise.

shaping. In order to reduce the OBG in a higher order NTF, poles are introduced into the NTF as given in Equation 2.22, with satisfying the no-delay free loops in the modulator (i.e., the 1^{st} sample of the NTF impulse response is 1 or $h[0] = 1$) [19, 39].

$$NTF\left(z\right) = \frac{\left(1 - z^{-1}\right)^{L}}{D\left(z\right)} \tag{2.22}$$

The most commonly used pole positions are realized from high-pass Butterworth or inverse Chebyshev transfer functions with a cut-off frequency outside the signal band [19, 39]. Further, the zero locations can be optimized for efficient SQNR

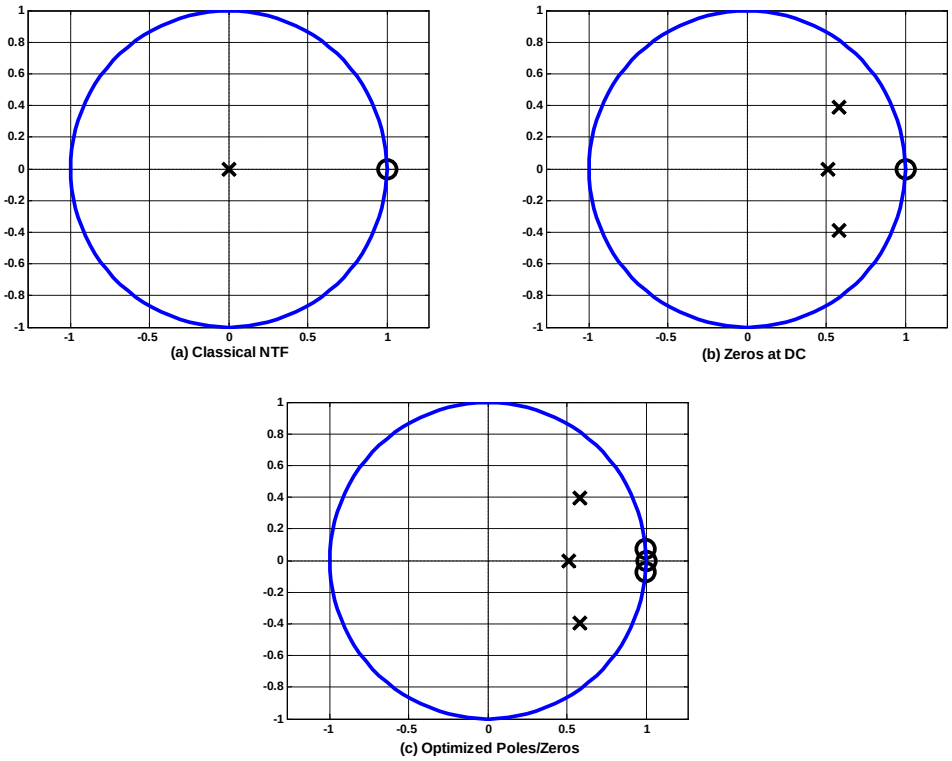

Figure 2.9: Pole/Zero locations of NTFs shown in Figure 2.8.

improvement using the following criteria [19, 24, 39]

$$min\left[\int_0^{BW}|NTF\left(z\right)|^2\,df\right]=\begin{cases} min\left[\int_0^1\prod_{i=1}^{L/2}\left(f-f_{zi}\right)^2\,df\right], L\ is\ even \\ min\left[\int_0^1 f^2\prod_{i=1}^{(L-1)/2}\left(f-f_{zi}\right)^2\,df\right], L\ is\ odd \end{cases} \tag{2.23}$$

The complete solution to the above equations are given in [19] where f_{zi} is normalized to the signal bandwidth. It is also noted that the actual zero frequencies are inversely proportional to the OSR and thus the improvement in dynamic range only depends on the NTF order and is independent of OSR.

In this work, the NTF is efficiently synthesized with optimized pole and zero using

the *delta-sigma toolbox* [41] in *Matlab* and its algorithm is detailed in [19]. Figure 2.8 shows the comparison of NTF with and without pole/zero or NTF optimization, which clearly explains that OBG is manipulated by increasing effective in-band noise. Further, Figure 2.9 shows the corresponding pole/zero plot for the NTFs in Figure 2.8.

2.6 Summary

This chapter presented an general overview of the $\Delta\Sigma$ ADCs. Further, fundamental analytical results along with the synthesis procedure for the DT prototype loop-filter are also presented.

CHAPTER 3

OVERVIEW OF CONTINUOUS-TIME DELTA-SIGMA MODULATORS

This chapter provides a step-by-step methodology for the synthesis of CT-$\Delta\Sigma$ loop-filter starting from the prototype DT loop-filter (synthesized from Section 2.4) using IIT, along with background information on CT loop-filter architectures. Also, it discusses basic limitations on selecting an appropriate parametric matrix of CT-$\triangle\Sigma$M to achieve higher conversion bandwidths and SQNR. Further, using the parametric matrix and synthesized CT loop-filter from the DT loop-filter for a given feedback DAC waveform, we can realize the modulator with real circuit blocks. However, the non-idealities of those circuit blocks as well as the clock source will influence the performance, and can even affect the stability of the overall modulator. In this chapter, critical design issues are discussed in detail from the system point of view, which include regenerative delay from the Flash ADC (i.e., excess-loop delay (ELD)), process, voltage and temperature (PVT) variation in the loop-filter coefficients, effect of clock jitter, effect of operational amplifier non-idealities on CT integrators, and finally the non-linearity of the feedback DAC.

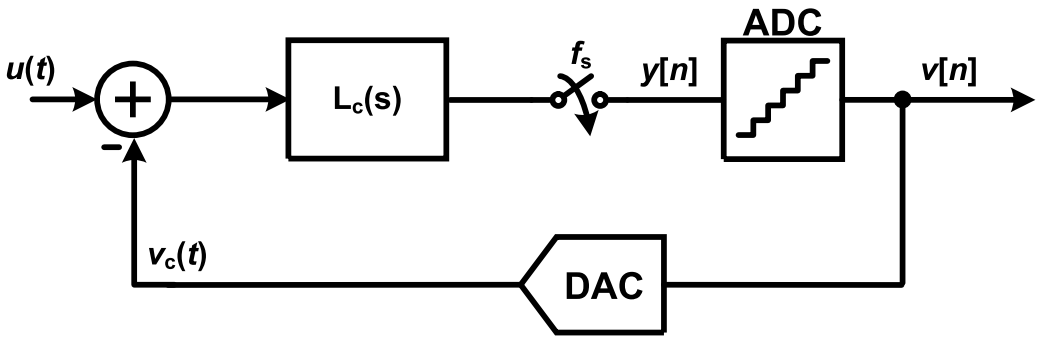

Figure 3.1: General block diagram of CT- ΣΔM.

3.1 Synthesis of the CT-Loopfilter

For a DT-ΔΣM, it is straightforward to design its loop-filter from Equation 2.19 using the desired $NTF(z)$ [19]. However, for a continuous-time ΔΣM, the CT loop-filter ($L_c(s)$) has to be designed based upon the DAC output waveform in the feedback path of the modulator. This is due to the fact that the CT loop-filter responds continuously to the input signal, unlike the switched-capacitor filters in which an analog charge is supplied to the filter at one clock phase and the output analog voltage is ready at another clock phase [19, 26, 38, 42].

In general, there are two approaches to synthesize a CT loop-filter, $L_c(s)$, (i) direct synthesis in the continuous-time domain, and (ii) transformation from a prototype discrete-time loop-filter ($L_d(z)$) [26, 42]. This dissertation uses the DT-to-CT transformation methodology to synthesize the CT loop-filter. This section helps the reader to understand the synthesis of the CT loop-filter for the traditional and proposed architectures in Chapter 4, 5, and 6, respectively.

A simple block diagram of a CT-ΔΣM is shown in Figure 3.1. In this figure, $L_c(s)$ is the CT loop-filter, implemented either using cascaded integrators with distributed feed-forward summation (CIFF), feedback (CIFB), or their hybrid architectures,

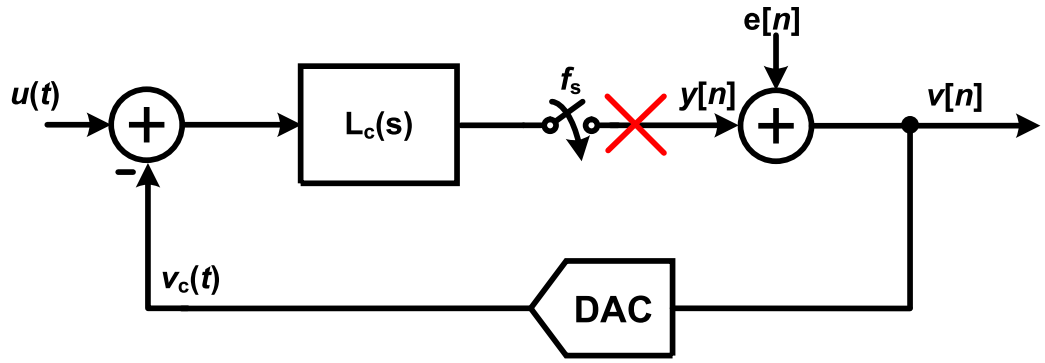

Figure 3.2: Modified general block diagram of CT- ΣΔM with incorporated quantizer model.

whose output is sampled at frequency, f_s (or equivalent time period T_s) and quantized using a quantizer. Ideally, there is no sampler inside the CT modulator. However, the quantizer inside the loop is clocked at f_s, which implies that there is an implicit sampling operation occurring inside the modulator [26, 38]. Thus, by placing the sampler immediately before the quantizer, as shown in the block diagram in Figure 3.1, it implies that the input to the quantizer is a DT, continuous-amplitude signal given by $y[n] \triangleq y_c(nT_s)$. Also, from Section 2.1, the quantizer output, $v\,[n]$, can be expressed as the summation of quantization error signal, $e\,[n]$, and an input, $y\,[n]$. Thus, Figure 3.1 can be simplified as Figure 3.2.

In order to synthesize the CT loop-filter, $L_c(s)$, corresponding to the DT prototype $L_d\,(z)$, the open-loop impulse response seen by the quantization noise with $u\,(t) = 0$, from Figure 3.2 should match with the open-loop DT-ΔΣM. As shown in Figure 3.3, this is achieved by breaking the loop around the quantizer and using an input $e[n] = \delta[n]$, which results in an open-loop impulse response, $l[n]$, which in the z-domain is represented by $L_d\,(z)$. This doesn't imply that the waveforms inside the loop are a discrete-time signal [26, 42]. However, the sampled values of the continuous-time waveform at the input of the quantizer, at sample times $t = nT_s$, define an exact DT

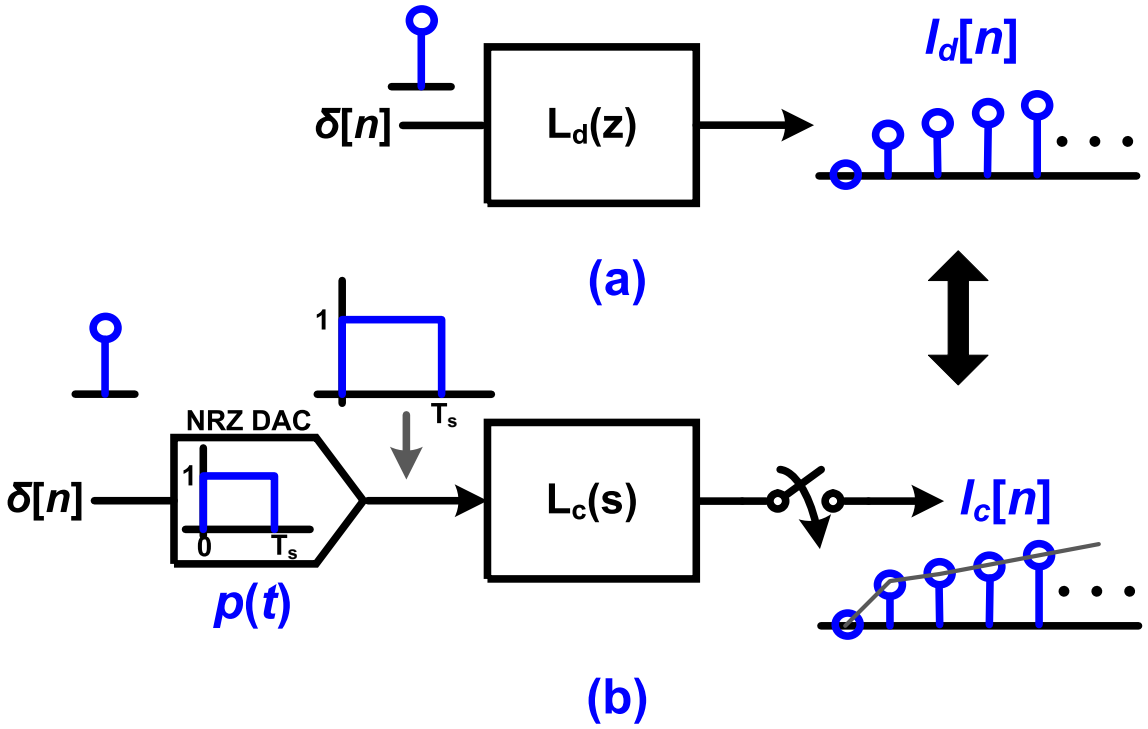

Figure 3.3: Open-loop responses of (a) DT- ΣΔM (b) CT- ΣΔM.

impulse response for the CT loop [38, 43, 44].

In the CT open-loop diagram from Figure 3.2, the DAC can be thought of as a discrete-to-continuous time-signal converter, which makes a CT pulse $v_c(t)$ from the quantizer output, $v[n]$, a discrete-time sequence [26, 42]. The following equation should be satisfied for the impulse responses to match each other

$$z^{-1}\{L_d(z)\} = L^{-1}\{P(s)\,L_c(s)\} \tag{3.1}$$

Further, the above equation can also be rewritten in time domain as

$$l(n) = \{p(t) \otimes l_c(t)\}\,|_{t=nT_s} = \int_{-\infty}^{+\infty} p(\tau)\,l_c(t-\tau)\,d\tau\,|_{t=nT_s} \tag{3.2}$$

where $P(s) = \mathcal{L}(p\,(t))$ is the impulse response of the DAC pulse shape [26, 42].

It can be seen that the DAC pulse-shape plays a significant role in the synthesis of the CT loop-filter. Different DAC pulses will result in different CT loop-filters for a given DT loop-filter prototype [26, 42]. Three commonly used feedback DAC pulse-shapes are non-return-to-zero (NRZ), return-to-zero (RZ), and switched-capacitor resistor (SCR). Each of these DAC pulse-shapes has its own distinct advantages and disadvantages. Detailed description of the DAC pulse-shapes can be found in [26, 42].

3.2 CT-Loop-Filter Architectures

Two popular architectures, feedback and feed-forward, are widely used in the CT-$\triangle\Sigma$M [26]. Each of them have their own advantages and disadvantages. In the following sections, we will review these two major classes of loop-filter architectures, which will greatly benefit the reader in understanding the system-level design of CT-$\triangle\Sigma$M in the subsequent chapters.

3.2.1 Casacade of Integrators with Feedback Vs Cascade of Integrators with Feedforward

An example of a 3^{rd}-order CT-$\triangle\Sigma$M with a CIFB and CIFF loop-filters is shown in Figures 3.4 (a) and (b), respectively [19, 26]. As can be deduced from Figure 3.4 (a), the feedback-type loop-filter requires several DACs, (k_1, k_2, k_3), feeding back to each integrator output, though it does not need a high-performance summing opamp before the quantizer. On the other hand, in the feed-forward structure, only one DAC is usually needed in the feedback path, therefore the latter is more area-efficient. However, the feedforward loop-filter requires a multi-input summing opamp to sum

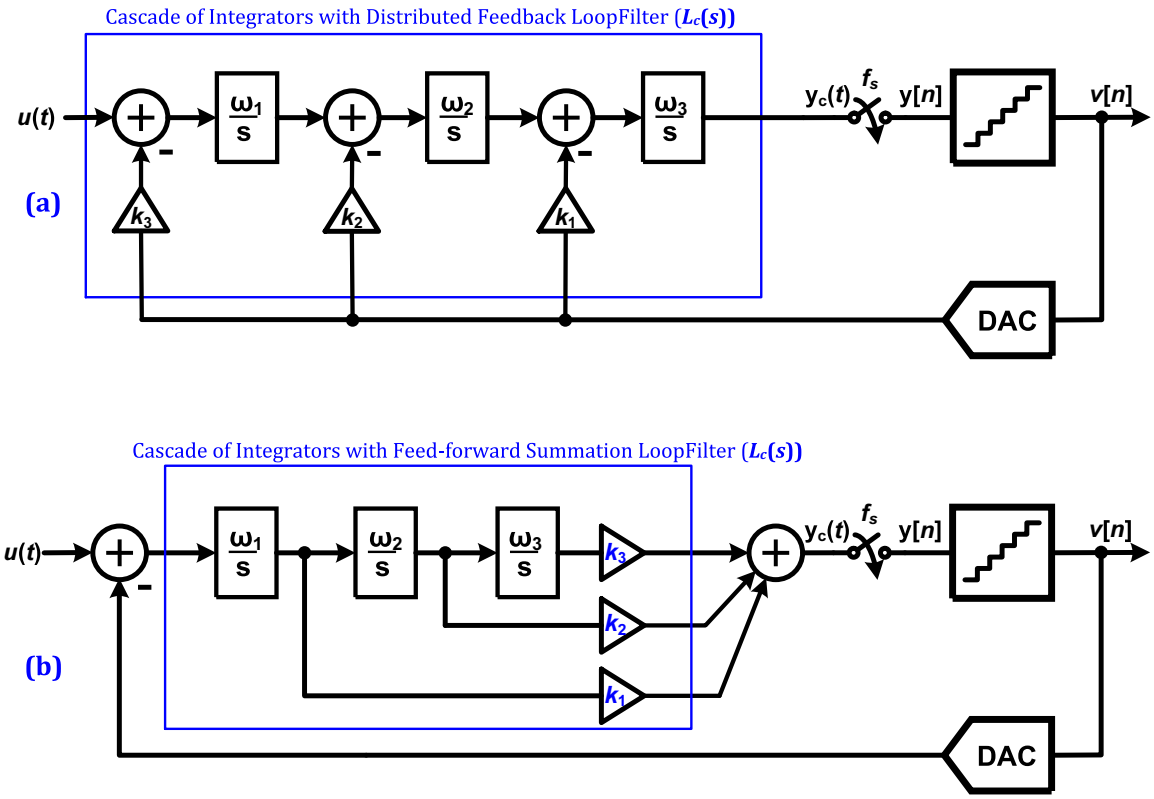

Figure 3.4: $3^{rd}-$order CT-$\triangle\Sigma$M with (a) cascade of integrators with distributed feedback and (b) cascade of integrators with feed-forward summation loop-filter architecture.

all feedforward branches, (k_1, k_2, k_3), just before the quantizer. Thus, the summer speed and linearity requirements will become one of the main bottlenecks of the overall modulator, especially in high-speed CT-$\triangle\Sigma$M designs [44].

Here, $\{\omega_1, \omega_2, \omega_3\}$ are the unity-gain frequencies of the integrators in the loop-filter, with a given sampling rate f_s. These non-trivial values for ω_i are obtained after performing dynamic range scaling (DRS) on the closed-loop to restrict the integrator state swings, as described later in Section 4.2.4. Notice that the first integrator is the "fastest" in a feedforward design due to the resultant trend $\{\omega_1 > \omega_2 > \omega_3\}$, while the first integrator is the slowest in the feedback-type modulator due to the trend

$\{\omega_1 < \omega_2 < \omega_3\}$. Thus, the integrating capacitor of the first integrator in a feed-forward loop-filter will be much smaller than that in a multiple-feedback modulator for a fixed resistor. Further, the input-referred noise and distortion considerations for the whole modulator dictate a large bias current in the first opamp. Therefore, in the first integrator, poles resulting from the finite bandwidth of the opamp can be expected to be at much higher frequencies. This can be used as an advantage in the feed-forward design, since the first integrator needs to be designed with the highest unity-gain frequency and is the most power hungry in the loop-filter. On the other hand, in a feedback-type architecture, steps must be taken to ensure that the parasitic poles in the last integrator (which is the most power hungry) are not at a lower frequency so that the loop stability is impacted. Thus, it requires larger bias currents in the last opamp due to the requirement grounded by $\{\omega_1 < \omega_2 < \omega_3\}$ and also in the first opamp due to circuit noise considerations, which in turn increases the overall power dissipation for the modulator.

Another significant advantage of the feed-forward loop-filter is the small output swing of the first integrator when compared to the feedback architecture. Also, with a smaller output swing, the first integrator allows a larger open-loop gain, and hence lower performance requirements on the following stages [26, 33]. However, one of the main disadvantages of a feed-forward architecture is the out-of-band peaking in its inherent anti-alias filtering characteristics, which implies that at the peaking frequency, the maximum stable input level is reduced by the gain of the peaking. As a result, the dynamic range of the ADC is compromised in the presence of large out-of-band interferer in the wireless receiver. On the other hand, a feedback type loop-filter does not suffer from gain-peaking and the resulting STF doesn't present any issue in the overall design [45].

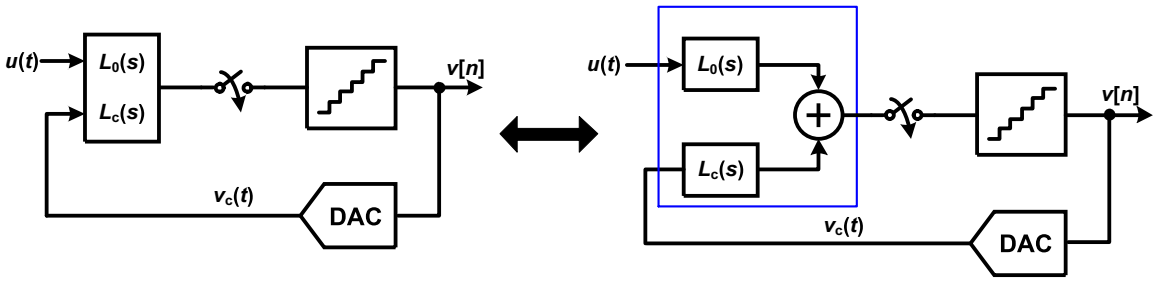

Figure 3.5: Linearized model of general CT-△ΣM.

Based on the above discussion, this dissertation uses the combination of feed-forward and feedback architecture or hybrid architecture. The complete system-level design of hybrid architecture will be explained in each of the CT-△ΣM designs in the later chapters.

3.3 STF Behavior in CT-△ΣM

The synthesis of a CT-ΔΣM from a DT modulator using IIT only considers the NTF, this transformation cannot guarantee that the STF of the CT-ΔΣM is the same as that of the corresponding DT-ΔΣM [26, 39]. Usually the resulting STF is different due to the CT pre-filtering in the former. Figure 3.5 shows the linearized model of a general CT-ΔΣM block diagram derived from Figure 2.7. This block diagram is further simplified by bringing out the sampler, as shown in Figure 3.6. The simplified block diagram clearly shows that the signal, $u(t)$, is pre-filtered by $L_0(s)$ before being sampled by the quantizer. This $L_0(j\omega)$ response provides an inherent anti-alias filtering in a CT-ΔΣM.

From Figure 3.6, there are two transfer functions that can be identified within the modulator (i) from the input $u(t)$ and (ii) from quantization noise. Applying IIT on the feedback path results in the same equation as 3.1. The transfer function from

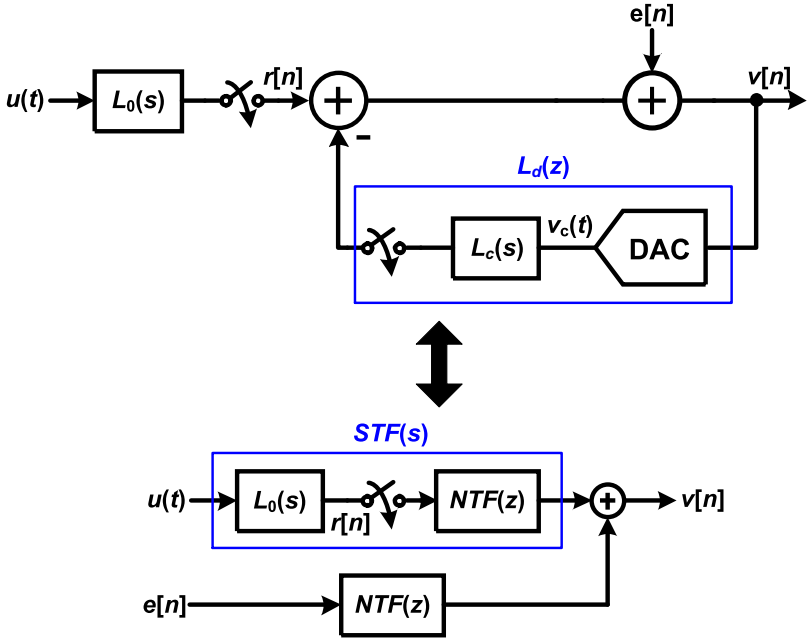

Figure 3.6: Simplified equivalent model of the CT-△ΣM shown in Figure 3.5 with separated pre-filtering transfer function $L_0(s)$ and the loop transfer function $L_c(s)$.

$r[n]$ to $v[n]$ is given as

$$\left.\frac{v[n]}{e[n]}\right|_{u(t)=0} = \frac{1}{1-L_d(z)} = NTF(z) \tag{3.3}$$

Using Figure 3.6, the STF from the CT input, $u(t)$, to the DT output, $v[n]$, can be expressed in terms of the modulator NTF and the forward path filter $L_0(s)$ as

$$STF(j\omega) = L_0(j\omega)\, NTF\left(e^{j\omega T_s}\right) \tag{3.4}$$

The characteristic of STF is purely based on the loop-filter architectures, $L_c(s)$, in Figure 3.1. In general, the pole frequency of $L_0(s)$ in the above equation always coincides with zeros of $NTF(z)$ and results in an unity-gain signal passband. Especially, in feedback CT loop-filter architecture, the resultant $L_0(s)$ is an all-pole

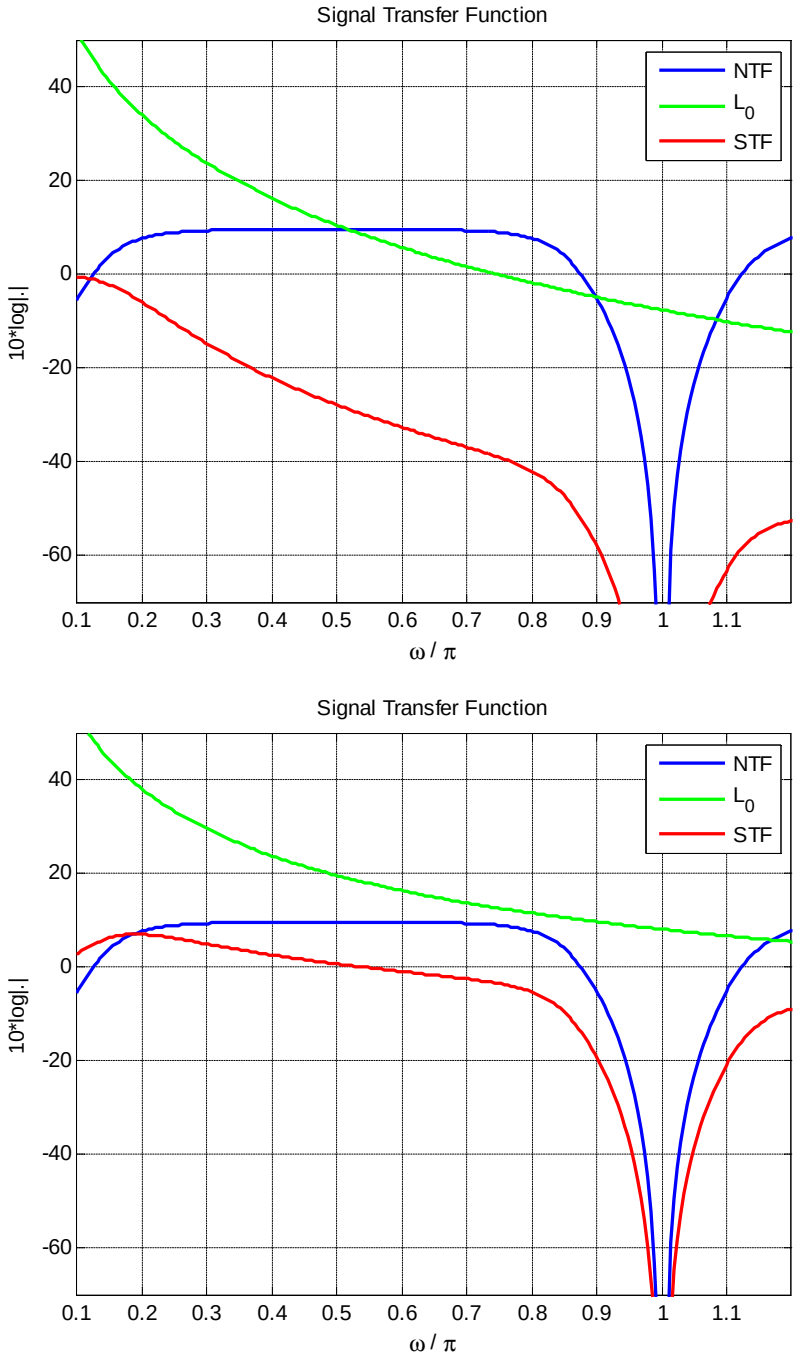

Figure 3.7: Implicit AAF of 3^{rd}-order CT-$\Delta\Sigma$M with feedback (above) and feedfordward (below) loop-filter architectures

transfer function. Thus, the poles of $L_0(s)$ cancel with zeros of $NTF(s)$ and exhibit a flat in-band frequency response [34, 45].

On the other hand, feed-forward loop filter architecture results in additional zero in $L_0(s)$ (number of zeros equal to the order of $L_c(s)$). These zero limit the high-frequency role-off of $L_0(s)$ and combine with the out-of-band gain of $NTF(z)$ and exhibit out-of-band peaking in the STF. Figure 3.7 shows the resultant STF of a 3^{rd}-order CT-$\Delta\Sigma$M with feedback and feed-forward loop-filter architectures. This figure clearly shows the resulting peaking in out-of-band of STF. In order to mitigate the peaking effect in STF, several techniques have been introduced in the literature with some power penalty for the overall modulator [34, 45].

3.4 Parameter Matrix of $\triangle\Sigma$ Modulator

The performance matrix of any $\Delta\Sigma$M is defined based on the desired DR and conversion BW of the ADC. This performance matrix mainly depends on three key design parameters of the $\Delta\Sigma$M, which are:

- sampling frequency (f_s),
- quantizer resolution (B),
- order of the loop-filter (N).

The impact of these design parameters are individually addressed below.

3.4.1 Sampling frequency

The sampling frequency, f_s, is related to the conversion BW of $\Delta\Sigma$M by the following Equation 3.5.

$$f_s = 2 \cdot OSR \cdot BW \tag{3.5}$$

An important factor that limits the sampling frequency of CT-$\Delta\Sigma$ ADC is ELD. In a given technology, the maximum achievable sampling frequency, $f_{s,max}$ is primarily constrained by the tolerable ELD in the CT-$\Delta\Sigma$ loop [19, 26, 42].

ELD is primarily contributed by the finite regeneration time of the comparator latches in the quantizer, the delay from the DAC drivers and dynamic element matching (DEM) logic in the feedback DAC. Typically, in a conventional CT- $\Delta\Sigma$M, ELD is selected to be smaller than or equal to 0.5 for reduced sensitivity of the loop-filter coefficients due to process variations [19, 26, 42]. Therefore, ELD mainly limits the f_s, which in turn restricts the maximum achievable BW and OSR. On the other hand, any limitation on OSR constrains the maximum achievable signal-to-noise ratio (SNR). To compensate for the SNR degradation due to lower OSR, a higher resolution (i.e., multi-bit quantizer) is often used [17, 18, 22, 33, 46].

3.4.2 Quantizer Resolution

In $\Delta\Sigma$ ADC, the quantizer can be implemented either using one-bit or multi-bit based on the design requirements such as BW, f_s, and SQNR. But, in general, the one-bit quantizer has dominated over the multi-bit quantizer due to its inherent linearity, which is particularly important for overall performance of the $\Delta\Sigma$M [47, 48]. Also, the circuit implementation becomes very simple as the low-resolution ADC can be implemented using a single comparator and DAC, which simply consist of the feeding back of the reference voltage depending on the quantized value [47, 48].

The main drawback of using a single-bit quantizer is high quantization noise power (due to the large LSB size), which results in a lower DR. To suppress the

in-band quantization noise power and to improve the DR, the signal has to be heavily oversampled. To further enhance the DR, the order of $L(s)$ can be increased. But, the later potentially leads to stability issues in the overall loop dynamics (which will be addressed later in the following section). Also, in many cases, increasing the OSR ratio is not preferable due to the wider conversion bandwidth requirement. On the other hand, to achieve a wider signal bandwidth, the designers are limited by the lower oversampling ratio for a given clock rate [17, 18, 22, 33]. Any limitation on OSR limits the maximum achievable SNR and DR. In order to compensate for the SNR degradation due to lower OSR, higher resolution (i.e., multi-bit quantizers) are often used [17, 18, 22, 33, 46]. Several CT-$\Delta\Sigma$ modulators targeting 10-12 bits resolution with a signal bandwidth ranging from 5-20 MHz have been recently reported [17, 22, 33, 46].

This multi-bit low-resolution quantizer is typically implemented using Flash ADC to digitize the loop-filter output. In recent years, other ADC architectures such as a time-to-digital converter (TDC) and voltage-to-frequency converter based on a voltage-controlled oscillator (VCO) have also gained wider popularity in nano-CMOS technologies. But, each of these ADC architectures have its own advantages and disadvantages when employed inside a $\Delta\Sigma$ loop [49, 50, 51]. The highly popular ADC architectures such as pipelined or successive approximation can be considered instead of a flash ADC. However, multi-step quantizers take greater or equal than one clock cycle to digitize a sampled input. This adds latency to the feedback signal and this cannot be tolerated inside the loop and leads to instability [26, 42]. In summary, there are several advantages when using a multi-bit quantizer inside the $\Delta\Sigma$M loop, which include:

- Lower quantization noise floor and higher dynamic range [19, 26]

• Relaxed slew-rate requirements in the loop filter opamps [26, 33]

• Use of a multi-bit quantizer improves SQNR without increasing clocking frequency or OSR

• The stability problems associated with higher order $\Delta\Sigma$ are alleviated by the use of multi-bit quantization (i.e., the quantizer is not overloaded during the operation) [19, 26]

• A lower LSB size allows a higher OBG, which leads to aggressive noise-shaping with higher MSA.

In general, the Flash quantizer with feedback current-steering ADCs is used as the quantizer within the CT-$\Delta\Sigma$ loop [17, 18, 22, 33, 46]. The Flash quantizer uses a straightforward but circuit-intensive approach for analog-to-digital conversion where an input signal, $V_{in}(t)$, is simultaneously compared with $2^B - 1$ reference voltages in order to decide the output quantization level [5, 12, 52]. This approach requires $2^B - 1$ comparators to perform the conversion, which clearly shows that the power consumption and the area requirement of such ADC's are not suitable for achieving higher resolution. Due to circuit complexity and power consumption, the $\Delta\Sigma$M loop employs a maximum of a 4-bit resolution Flash ADC with a current DAC as a quantizer.

3.4.3 Order of the Loop-Filter

For the given quantizer resolution, increasing the loop-filter order also relaxes the f_s. However, the higher-order loop-filter requires more co-efficients to stabilize the modulator, thus increasing its complexity. Moreover, the loop-filter coefficients will drift due to PVT variation and may cause SNR degradation. Despite the drawbacks

of the higher-order loop-filter, in general loop-filter around three is preferred in high-speed $\Delta\Sigma$M sampling at $f_{s.max}$ with 4-bit quantizer [17, 18, 22, 33, 46].

3.5 Design Issues in CT-$\triangle\Sigma$ Modulator

Once the CT loop-filter, $L_c(s)$, is synthesized from the DT prototype for a given feedback DAC pulse, as explained in Section 3.1, the system is ready to be realized with transistor-level circuit blocks for a given parametric matrix which can meet the desired specifications [19, 26]. However, the non-idealities of the real circuit blocks and the clock source have significant effect on the performance of the modulator, including the stability of the modulator [19, 26]. In this section, we will review some of the most critical design issues, which include:

- Non-idealities of the CT integrators
- PVT variation on loop-filter coefficients
- Delay from the flash ADC
- Clock jitter
- Linearity requirement from feedback DAC

For each of the above design issues, detailed analysis supported by simulations, and methods to mitigate them are discussed below.

3.5.1 Operational Amplifier Non-idealities on CT Integrators

In general, a CT loop-filter, $(L_c(s))$, can either be implemented using active-RC or $G_m - C$ integrators as shown in Figure 3.8 [26, 38]. In this dissertation, an active-RC integrator is chosen over $G_m - C$ due to the following reasons:

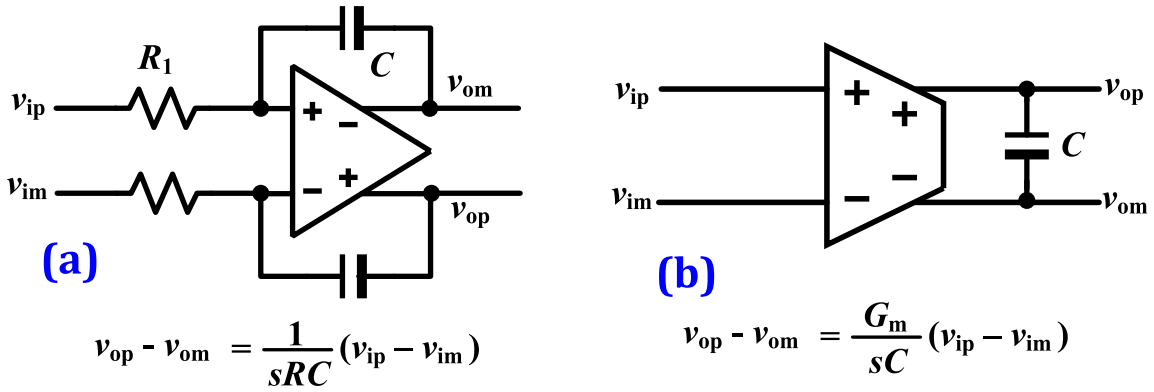

Figure 3.8: (a)Active RC Integrator (b)$G_m - C$ Integrator.

1. Active-RC integrators have overall better linearity for the same power consumption and allow higher signal swing while the $G_m - C$ integrators are significantly limited by both [26, 38].

2. Active-RC integrators provide significantly quieter virtual grounds due to the closed-loop functionality of the operational amplifiers (opamps) regardless of the integrators input. Thus, the current-mode ADCs can properly sink or supply its output current, without adding significant distortion in the integrator output [26, 38].

In spite of the above advantages, $G_m - C$ can achieve higher speed and lower power consumption when compared to their active-RC counterparts. However, due to the high MSA requirement (i.e., linearity and signal swing), opamp-based active-RC integrators are preferred in high-speed CT-$\Delta\Sigma$M. Thus, only the non-idealities of the active-RC integrators will be discussed in this section.

Active-RC Integrators consist of an opamp and passive components, resistor and capacitor, as shown in Figure 3.8(a). Ideally, an opamp has an infinite open-loop gain and bandwidth. However, a real opamp departs somewhat from ideal due to the

non-idealities (i.e., the finite DC gain and bandwidth limitation due to parasitic poles and zeros). The simplified first-order model of these non-idealities to characterize the opamp is given as [38]

$$H(s) = \frac{A_{DC}}{1 + \frac{s}{\omega_p}} \tag{3.6}$$

where A_{dc} and ω_p are the finite DC gain and pole frequency of the opamp, respectively.

Using the above first-order linear opamp model, the integrator transfer function (ITF) for a active RC integrator shown in Figure 3.8(a) can be derived as follows (for simplicity, consider the single-ended version)

$$ITF(s) = -\frac{1}{R_1} \frac{1}{\frac{C_1}{A_{DC}\omega_p} s^2 + \left(\frac{(A_{DC}+1)C_1}{A_{DC}} + \frac{1}{A_{DC}\omega_p R_1}\right) s + \frac{1}{A_{DC}R_1}} \tag{3.7}$$

The above equation can be further simplified, as $A_{DC} \ggg 1$, which is a common case in real opamps, then the above equation can be rewritten as [38]

$$ITF(s) = -\frac{1}{R_1} \frac{1}{\frac{C_1}{A_{DC}\omega_p} s^2 + \left(C_1 + \frac{1}{A_{DC}\omega_p R_1}\right) s + \frac{1}{A_{DC}R_1}} \tag{3.8}$$

$$ITF(s) = -\frac{k_1 f_s}{s} \frac{\left(1 - \frac{k_1 f_s}{GBW + k_1 f_s}\right)}{\left(1 + \frac{s}{GBW + k_1 f_s}\right)}\Bigg|_{k_1 = \frac{f_s}{R_1 C_1}} \tag{3.9}$$

Equation 3.8 can further simplified as Equation 3.9 by replacing $k_1 = \frac{f_s}{R_1 C_1}$ and $A_{dc}\omega_p = GBW$, where GBW stands for the gain bandwidth product of the opamp [38].

It can be deduced from Equation 3.9 that the required gain (k_1) is multiplied by a factor $\left(1 - \frac{k_1 f_s}{GBW + k_1 f_s}\right)$ and ideal integrator bandwidth is further limited due to the second pole (ω_{p2}) at $-GBW + k_1 f_s$. The above $ITF(s)$ model are extensively used in

system-level design of CT-$\Delta\Sigma$M's (in later chapters) to understand and mitigate the effect of opamp finite DC gain and bandwidth on modulator performance. Thus, the gain error is compensated with an additional gain (k_c) and proper opamp bandwidth specification will be obtained before the circuit-level implementation of the loop-filter [38].

3.5.2 Effect of PVT Variation on Loop-Filter Coefficients

As discussed in Section 3.5.1, active-RC integrators are chosen in high-speed CT-$\Delta\Sigma$M design. But, due to the PVT variation, there is a systematic variation in the loop-filter time constants (i.e., the absolute values of resistors and capacitors) that impact the overall accuracy of the integrator transfer function and result in performance degradation of CT-$\Delta\Sigma$M. In general, due to PVT variation, the absolute values of resistors and capacitors can vary as large as $\pm 20\%$ independently from die-to-die. Thus, it is reasonable to believe that the RC product or the integrator gain can vary $\pm 40\%$.

In order to understand the effect of the RC time constant on the overall modulator performance, the 3^{rd}-order maximally flat nominal NTF (i.e., with no variation in the RC time constant) with an out-of-band gain of three (a 4-bit quantizer is assumed, which facilitates the use of an NTF with a large out-of-band gain) is used [26].

Figure 3.9 shows the magnitude response of nominal NTF in dB with its time constant (i.e., $1/RC$ is $+30\%$ higher from nominal value), which shows a significant out-of-band peaking of the NTF. Similarly, for time constant (i.e., $1/RC$ is -30% lower from nominal value), the in-band quantization noise is higher than the nominal case, while the out-of-band gain is smaller than 3.

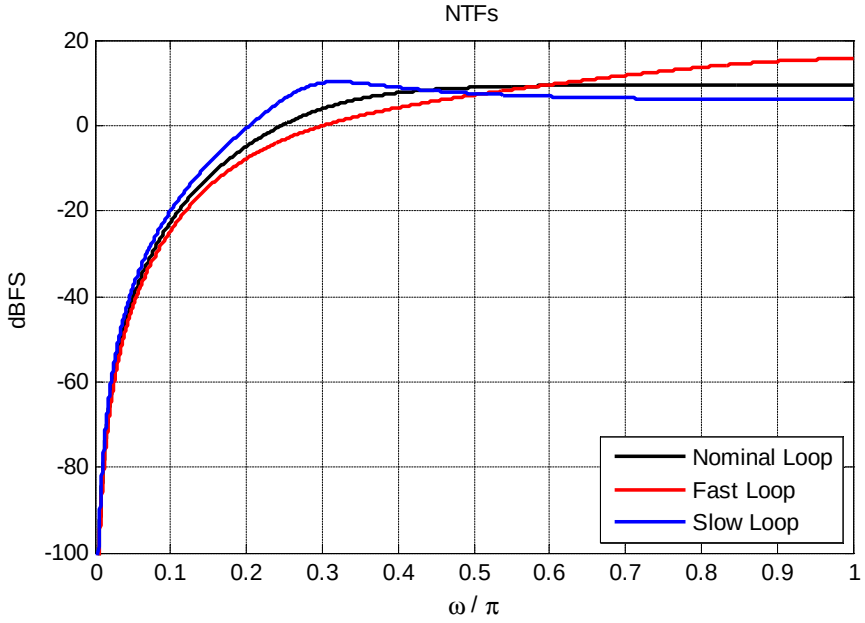

Figure 3.9: Magnitude of NTF in dB with $\pm 30\%$ time constant with respect to nominal k_i values.

The above discussion can also be interpreted in the time-domain behavior of the modulator. Figure 3.10 shows the output of a CT-$\Delta\Sigma$M for different values of a RC time constant, when the modulator is excited by a sinusoidal input. When a RC time constant varies +30% more than the nominal value, the large out-of-band gain in the NTF results in more "wiggling" of the analog–digital converter output sequence around the input signal, since the quantization noise is amplified to a larger extent, as seen in Figure 3.10 (bottom) when compared to the ideal case in in Figure 3.10 (top) [53, 54, 55]. The larger wiggling pushes the modulator into instability even for smaller input amplitude and reduces the maximum achievable MSA. For the NTFs used in practice, simulations show that a $\pm 5\%$ deviation of the time constants from their nominal values is usually acceptable.

To make the RC time-constant variation as small as $\pm 5\%$, a simple tuning

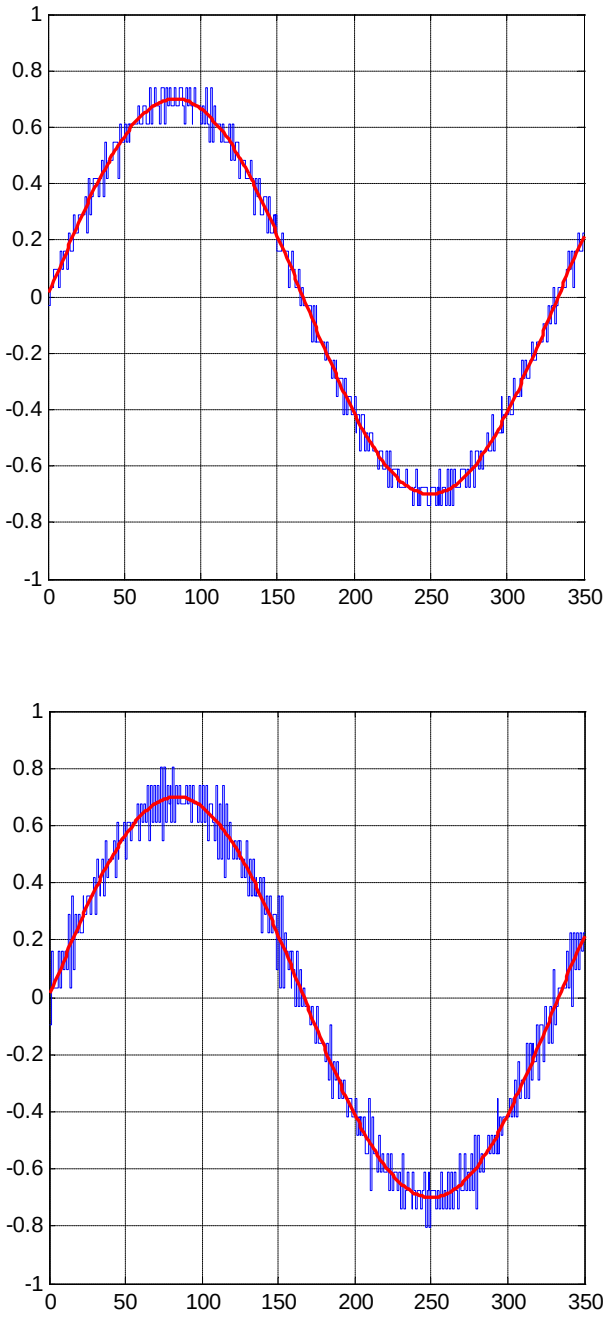

Figure 3.10: Time-domain output stream of a 4-bit CT$\Delta\Sigma$ modulator when: (top) nominal loop filter (i.e., no variation in RC time constant), thus the OBG is 3; (bottom) loop filter is fast (i.e., RC time constant varies+30% more than the nominal value).

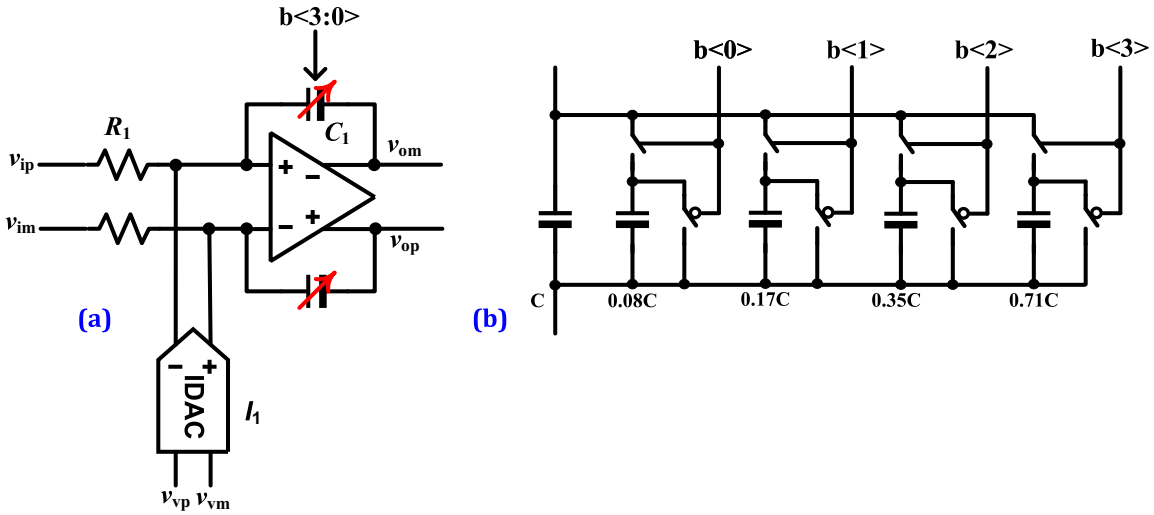

Figure 3.11: (a) First integrator; Other integrators are similar except for the absence of the DAC. (b) Switchable feedback capacitor for adjusting the time constants.

technique will be used. In the past several decades, many useful tuning techniques were published for designing CT filters [53, 54, 55]. This work uses the normal manual digital tuning. In general, it is more convenient to tune the capacitors instead of the resistors to adjust the RC product because the integration capacitor is shared by all input resistors. Figure 3.14 shows the diagram of a tunable capacitor array implemented as banks of digitally switched binary weighted capacitors. The tuning range is chosen large enough to compensate for a variation of process-dependent RC time constant up to $\pm 40\%$. A 4-bit tuning word provides the required tuning range while allowing a tuning accuracy better than $\pm 5\%$.

3.5.3 Excess Loop Delay

A simplified block diagram of a single-loop CT-$\Delta\Sigma$M is shown in Figure 3.12 to illustrate the effect of excess loop delay. In Figure 3.12, $L(s)$ is the loop filter and the quantizer is represented as a linear model. From this figure, it seen that the quantizer

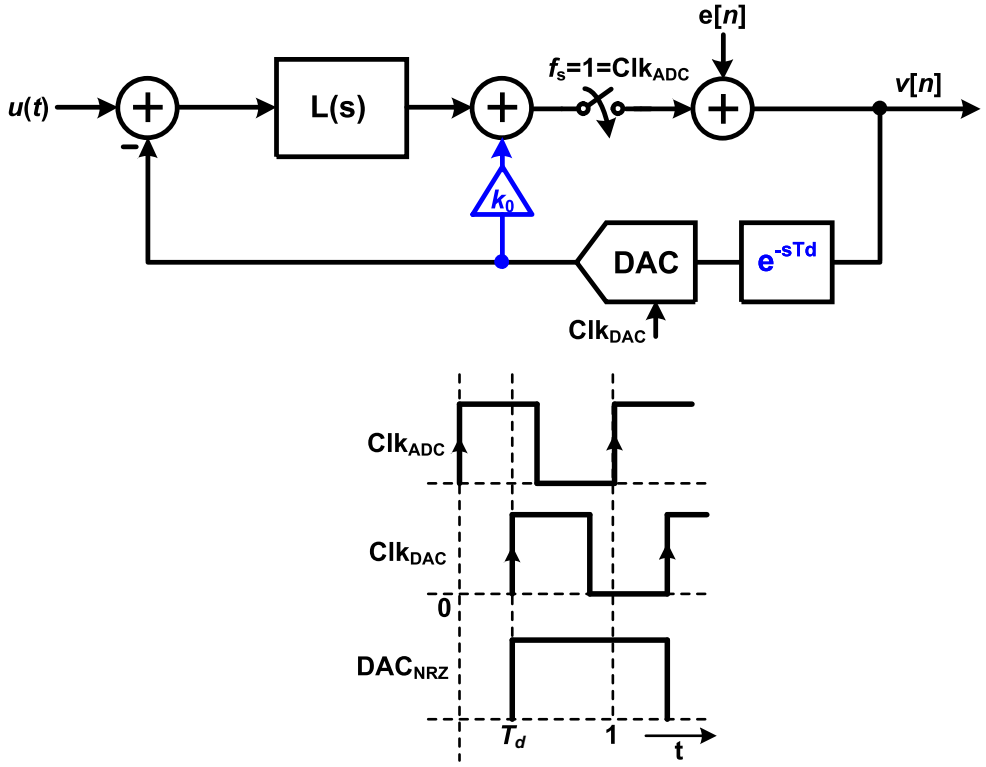

Figure 3.12: Excess delay in continuous-time $\triangle\Sigma$ modulator

is clocked at the rising edge of CLK_{ADC} and after a delay, T_d, DAC is clocked at the rising edge of CLK_{DAC}. The reason behind this is that any practical ADC takes time to make a decision due to the limited switching speed of the transistors. Thus, there exists a certain amount of delay between the quantizer sampling instance and the feedback DAC output. This delay is known as excess loop delay and it can be detrimental to the stability of the modulator loop. Because, if the DAC waveform is not contained in one sampling period and enters the adjacent cycle due to the ELD, as shown in Figure 3.12, as DAC_{NRZ}, then the effective order of the loop filter will be increased [26, 42].

This can be explained by modeling the delayed DAC waveform from Figure 3.12 as the superposition of two individual pulses as the following equation using Figure

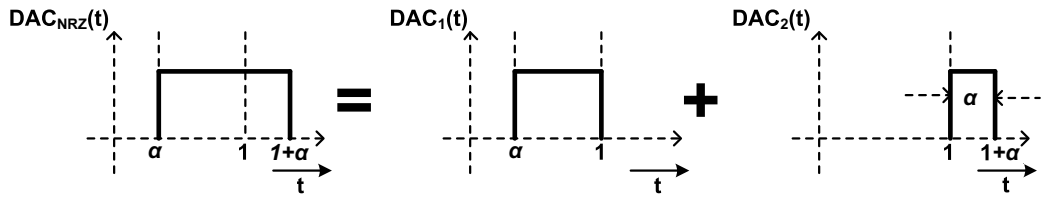

Figure 3.13: Decomposition of a delayed DAC waveform from Figure 3.12.

3.13 as

$$DAC_{NRZ}(t) = DAC_1(t)|_{T_d,T_s} + DAC_1(t)|_{0,T_d} \tag{3.10}$$

where $DAC_1(t)$ represents a pulse from $\alpha = \frac{T_d}{T_s}$ to $\beta = T_s$, and $DAC_2(t)$ represents a pulse from 0 to $\beta = \frac{T_d}{T_s}$ and $DAC_2(t)$ is delayed by one clock cycle. The resulting Z-transform is calculated as the superposition of the two terms, where the term associated with $DAC_2(t)$ includes a z^{-1} factor, which is responsible for the increased order of the loop filter.

Let's consider the 2^{nd}-order open-loop transfer function of the continuous-time loop filter required to realize a modulator NTF of $(1-z^{-1})^2$ is of the form $L(s) = \frac{k_1 s + k_2}{s^2}$. For an NRZ DAC without excess delay, $k_1$and k_2 can be shown to be 1.5 and 1, respectively, using IIT. With ELD, the integrators are converted into their z-domain equivalents using the impulse invariance transformation corresponding to a DAC pulse delayed by T_d (we assume that $T_d < 1$). Using the table from reference [26], we get

$$\frac{1}{s} \longrightarrow \frac{1-T_d}{z-1} + z^{-1}\frac{T_d}{z-1} \tag{3.11}$$

$$\frac{1}{s^2} \longrightarrow \frac{(0.5 - T_d + 0.5T_d^2)\,z + 0.5\,(1-T_d^2)}{(z-1)^2} + z^{-1}\frac{T_d\,(1-0.5T_d)\,z + 0.5T_d^2}{(z-1)^2} \tag{3.12}$$

Using $k_1 = 1$ and $k_2 = 1.5$, the discredited loop filter becomes

$$L_d(z,\alpha) = \frac{1}{2}\frac{z^2(4-\alpha)(1-\alpha) - 2z(\alpha^2 - 4\alpha + 1) + \alpha(3-\alpha)}{z(z-1)^2}\Bigg|_{k_1=1,k_2=1.5} \tag{3.13}$$

The root-locus of the NTF poles versus normalized ELD of α is plotted in Figure 3.14 [39], where the DT loop-transfer function of the modulator is given by Equation 3.13. Clearly the number of poles is increased from 2 to 3 even for an infinitesimal delay. Further increase of ELD pushes NTF poles outside of the unit circle, where the critical delay is shown with $\alpha_{crit} = 0.2$. The effect of ELD on the stability manifests itself as the reduced overload-level, which adversely affects the modulator dynamic range. It has also been shown that the ELD can elevate the quantization noise floor by degrading the NTF at low frequencies [26, 42]. Therefore, to avoid potential dynamic range losses, the excess delay in CT-$\Delta\Sigma$M needs to be controlled.

3.5.3.1 Conventional ELD Compensation

In order to stabilize the 2^{nd}-order CT-$\triangle\Sigma$M with $L_d(z,\alpha)$, an additional direct path around the quantizer with a gain k_0 (as shown in Figure 3.12) results in a loop filter transfer function, $L(s)$, given by

$$L(s) = \frac{k_1}{s^2} + \frac{k_2}{s} + k_0 \tag{3.14}$$

The value of $\{k_1, k_2, k_0\}$ can be found by solving

$$k_0 z^{-1} + k_1\,(RHS\,of\,3.11) + k_2\,(RHS\,of\,3.12) = \frac{2z-1}{(z-1)^2} \tag{3.15}$$

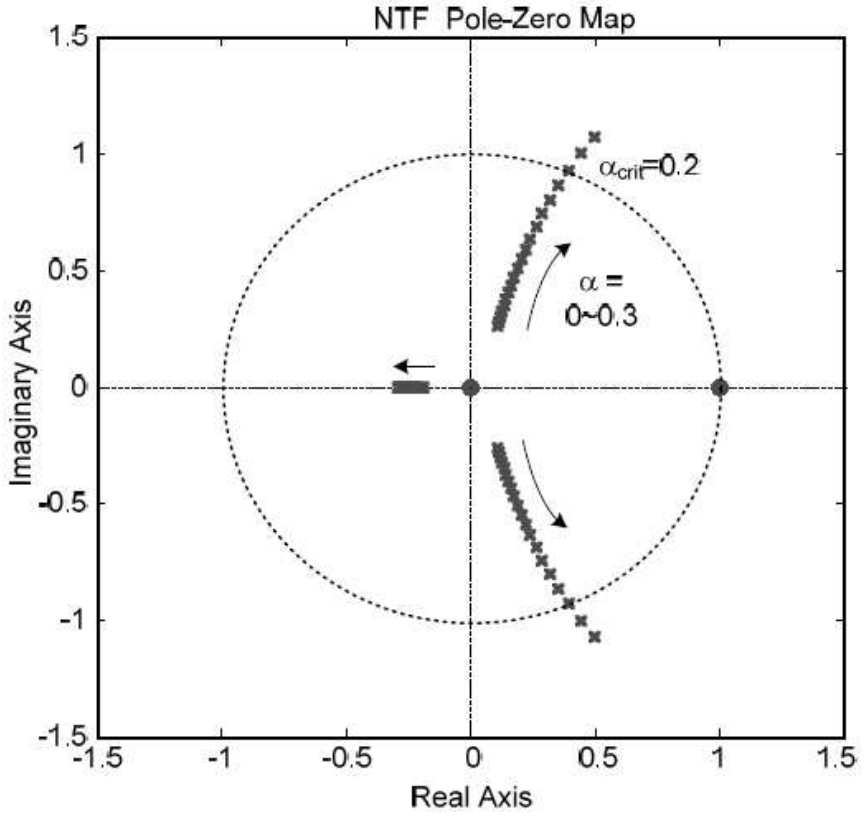

Figure 3.14: NTF Pole/Zero map subject to 0 to 30% ELD.

Simplifying the above equation results in

$$\{k_1, k_2, k_0\} = \left\{1.5T_d + 0.5T_d^2,\ 0.5T_d^2 + T_d,\ 1\right\} \tag{3.16}$$

As expected, setting $T_d = 0$ in the above solution yields $\{k_1, k_2, k_0\} = \{1.5, 1, 0\}$. For different DAC pulses like NR or triangular, the overall process remains the same, only 3.11 and 3.12 will change [26, 42].

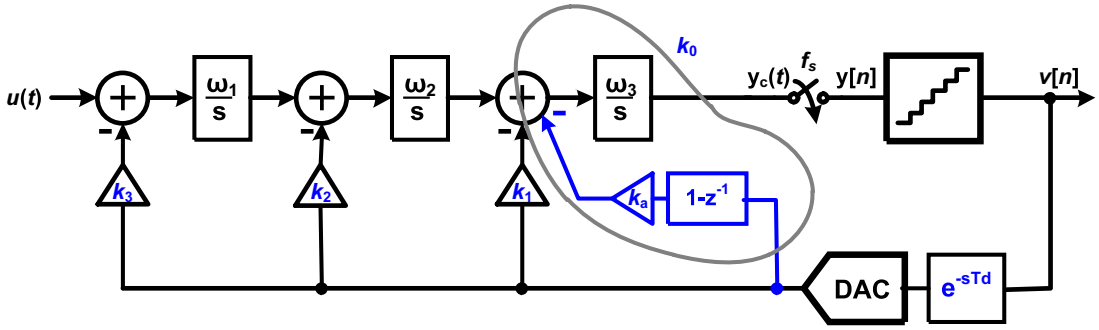

Figure 3.15: ELD compensation using a digital differentiators.

3.5.3.2 ELD Compensation Using a Digital Differentiator

Figure 3.15 shows the 3^{rd}-order CIFB CT-$\triangle\Sigma$M where the ELD compensation path is moved from the output of the last integrator to its input. In return, the DAC output signal must be differentiated before being integrated [42]. To achieve this, the digital differentiator was implemented in [17]. The direct path gain, k_0, is achieved by $k_0+\omega_3$, where the CT integrator transfer function is canceled by digital differentiation and results in a constant gain at the output. This method eliminates the requirement for a high-speed summer. Further, this ELD compensation in combination with feed-fordward and feedback architecture is used in traditional high-speed CT-$\Delta\Sigma$M in the following chapters. The detailed system-level design of this architecture will also be explained in the subsequent chapters.

3.5.4 Clock Jitter

In a DT-$\Delta\Sigma$M, the CT input signal is already sampled at the input of the modulator, thus the sampling error caused by clock jitter is directly added to the output without any attenuation [19]. While in the CT-$\Delta\Sigma$M, the sampling occurs at the input of the quantizer, though any error due to the variation of the sampling instant of

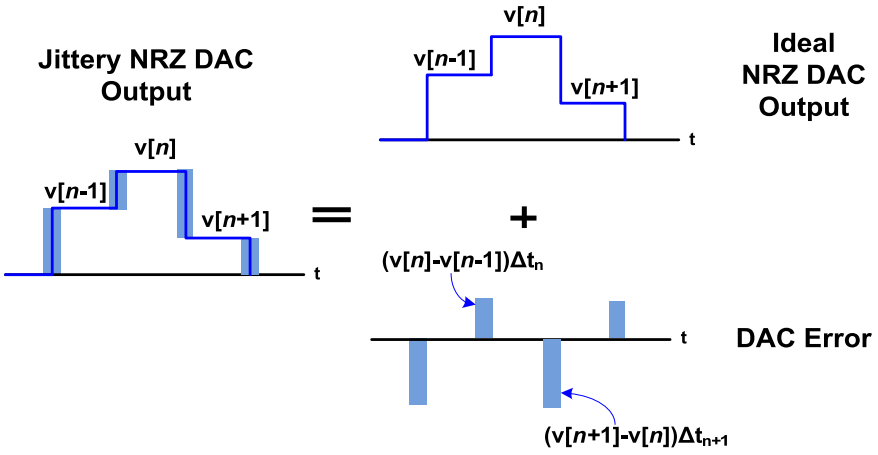

Figure 3.16: Equivalent representations of a jittered DAC stream.

the quantizer is noise-shaped by the high loop-gain. Thus, the jitter-induced error contribution towards the total in-band noise power should not be affected by this sampling jitter component.

However, the feedback DAC in CT-$\Delta\Sigma$M is continuous, which means that the feedback signal is fed to the loop filter at all times instead of just at the sampling instants in DT-$\Delta\Sigma$M. Hence, any timing error of the feedback signal transition edges caused by the DAC clock jitter is equivalent to the feedback signal error itself. The effect of clock jitter on the CT-$\Delta\Sigma$M performance has been well-documented in the literature [56, 57, 58]. Also, this error from the feedback DAC adds directly to modulator input. Therefore, this error is not noise-shaped and degrades the modulator performance.

To gain an intuitive understanding of the jitter noise on feedback DAC, consider a current mode feedback NRZ DAC, I_{DAC}. Every clock cycle the DAC transfers a net charge to the integrating capacitor, which ideally equals to the area under the

feedback waveform, which is given as

$$Q[n] = I_{DAC}[n].T_s \tag{3.17}$$

However, in the presence of jitter, the transferred charge will deviate from its ideal value by

$$\triangle Q[n] = (I_{DAC}[n] - I_{DAC}[n-1])\triangle T[n] \tag{3.18}$$

where $\triangle T[n]$ denotes the NRZ timing error due to clock jitter.

In order to evaluate the effect of jitter in the multi-bit NRZ $\Delta\Sigma$ modulator, consider Figure 3.16. From Figure 3.16, the jittery CT-DAC output signal is equivalent to the sum of an unjittered CT-DAC signal and a stream of DAC CT error signal, or net error charge, which can be estimated as follows [58]

$$e_j[n] = (v[n] - v[n-1])\left(\frac{\triangle t[n]}{T_s}\right) \tag{3.19}$$

In the above equation, $v[n-1]$ and $v[n]$ are two consecutive outputs of the modulator and $\triangle t[n]$ is the timing jitter corresponding to a Gaussian random process with zero mean and standard deviation $\sigma_{\triangle t}$. Using Equation 3.19, the in-band noise power due to jitter can be evaluated as [58]

$$S_j = \left(\frac{\sigma^2_{\triangle t}}{OSR}\ E\left\{(v[n] - v[n-1])^2\right\}\right) \tag{3.20}$$

In the above equation, $\sigma^2_{\triangle t}$ is the variance of normalized clock jitter. Further, the in-band jitter noise power is derived as [58]

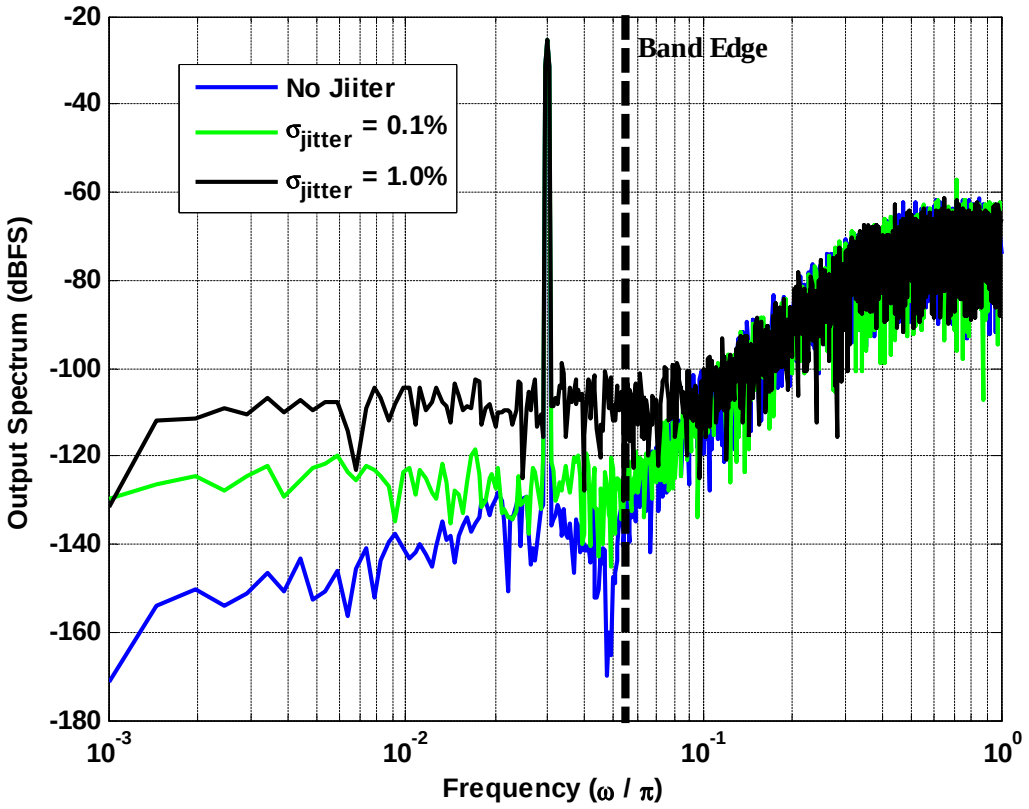

Figure 3.17: Output spectrum of a 3rd-order CT-$\Delta\Sigma$ modulator affected by jitter.

$$S_j = \left(\frac{\sigma^2_{\triangle t}}{T_s^2} \; \frac{\sigma^2_{LSB}}{\pi OSR} \int_0^{\pi} \left| \left(1 - e^{-j\omega}\right) NTF\left(e^{j\omega}\right) \right|^2 d\omega \right) \tag{3.21}$$

The integral term in Equation 3.21 is the product of the first-order high-pass filter $1 - z^{-1}$ and modulator's NTF. This predominantly suggests that the jitter noise is mainly influenced by the NTF response at higher frequencies. In other words, a more aggressive noise-shaping with larger NTF out-of-band gain will be more sensitive to clock jitter due to larger steps at its output. Equation 3.21 is extensively used in system-level design of traditional and proposed architecture to estimate and budget the degradation in SNR due to clock jitter [39] .

Figure 3.17 shows the output spectrum of a third-order CT-$\Delta\Sigma$M subjected to

1% and 0.1% jitter (normalized to T_s). The total in-band noise power, including the $-92\,dBFS$ quantization noise, is $-64\,dBFS$ and $-83\,dBFS$ for 1% and 0.1% jitter, respectively. From these numbers, the jitter-induced noise power is found as $-67\,dBFS$ and $-86\,dBFS$ for 1% and 0.1% jitter, respectively.

3.5.5 Non-Linearity of Feedback DAC

As discussed in Section 3.4.2, in order to achieve lower in-band noise power in low OSR $\Delta\Sigma$M, multi-bit quantizers are often used. However, the multi-bit $\Delta\Sigma$M in turn requires a multi-bit DAC in the feedback path. In a single-loop multi-bit CT-$\Delta\Sigma$M, the feedback DAC is implemented using a current-steering DAC, which is built using unit current sources [26, 33]. But, due to process variation and layout imperfections, the unit elements will be mismatched to each other and introduce non-linearity in the DAC transfer characteristics.

The non-linearity of the feedback DAC severely limits the performance of the modulator. This is due to the fact that any errors introduced by the feedback DAC are added at the same point as the input signal, so they appear directly at the output without any noise-shaping. Thus, the linearity of a $\Delta\Sigma$M cannot be better than the linearity of the DAC used in its feedback path. Therefore, if multi-bit ADCs are to be employed, either a linearization technique like DEM [33] or self-calibration [44] should be incorporated.

3.6 Summary

This chapter provided the synthesis of a CT-$\Delta\Sigma$ loop filter from a DT loop filter using IIT, along with background information on CT loop-filter architectures. It also

discussed basic limitations on selecting an appropriate parametric matrix of high-speed $\Delta\Sigma$M. Further, the complete non-idealities of $\Delta\Sigma$M circuit blocks as well as the clock source effects on the stability and performance of the overall modulator is demonstrated with simulation results along with solutions.

CHAPTER 4

A LOW-POWER, 1.25 GHZ, SINGLE-BIT SINGLE-LOOP CONTINUOUS-TIME $\triangle\Sigma$ MODULATOR WITH 15 MHZ BANDWIDTH AND 60 DB DYNAMIC RANGE

This chapter presents the complete system and circuit-level design details of a low-power, wideband single-bit CT-$\Delta\Sigma$ modulator, operating at $1.25\,GS/s$ output data rate and implemented in IBM $0.13\,\mu m$ CMOS technology. This is the highest reported sampling frequency in this process while achieving the overall competitive energy-efficiency and FoM. The modulator is targeted for applications that demand high bandwidth and resolution with low power dissipation, such as portable broadband wireless and wireline communication. The system-level design section details the determination of design parameters, optimization of the modulator architecture for attaining low power, noise budgeting, and the modeling of circuit non-idealities and simulation. Further, the complete circuit design of each block used in the high-speed modulator is presented with detailed simulation and test results.

4.1 Introduction

In order to achieve low-power, small layout area, and reduced circuit complexity for a $\Delta\Sigma$M, a single-bit quantizer is chosen. In Chapter 3, we have already explained the

advantages of a single-bit modulator over a multi-bit design in detail. This section summarizes the most significant benefits of a single-bit modulator, which are:

- Inherently linear feedback DAC (just two levels), hence no DEM or calibration is required. Thus, the power is reduced drastically with less circuit complexity.

- Single-bit design reduces excess-loop delay in the feedback path (especially from the DAC, DEM logic, and the DAC driver), which enables a higher sampling rate to obtain the desired SQNR.

- Simple 1-bit quantizer results in better energy-efficiency, while the area and layout parasitics are significantly reduced.

- The linearity of the last opamp is highly relaxed as the output of the last opamp does not have to accommodate a full-scale swing due to a single-bit quantizer.

In spite of the above advantages, the most important concerns in single-bit single-loop CT-$\Delta\Sigma$M are the slew rate requirement of the first opamp and higher in-band quantization noise due to the single-bit quantizer. The higher in-band quantization noise can be addressed by increasing the effective OSR. While, on the other hand, any slewing in the opamp introduces distortion and increases the in-band noise, which in turn results in reduction of the SQNR [32]. This turns out to be the main bottleneck in achieving the low-power in a high-speed CT-$\Delta\Sigma$ modulator, because any reduction in opamp power will results in degradation of the finite DC gain, f_{unity}, and slewing performance of the opamp. Also, the lower f_{unity} of the opamp impairs the characteristics of the loop filter and thus modifies the NTF with significant performance degradation. In order to achieve a low-power design with

acceptable performance, a systematic design-centering method proposed in [43] along with optimized modulator architecture proposed in [17] is adapted in this work.

4.2 System-Level Design of the Single-Bit CT-△ΣM

In this section, we describe the various architectural choices made in the single-bit CT-ΔΣM design, which includes the design of NTF, determination of design parameters from NTF, the optimization of the modulator architecture for attaining lower power, by considering the contribution of various noise sources to the total in-band noise of the modulator, DRS of loop-filter states, and complete estimation of SNDR degradation due to non-idealities using behavioral simulations.

4.2.1 Design of Noise-Transfer Function

The choice of the proper $NTF\,(z)$ plays a prominent role in the modulator performance. In a single-bit CT-ΔΣ modulator design, increasing the order of noise-transfer function greater than 3 renders the modulator to be prone to instability and also reduces the MSA of the input [19, 48]. Thus, to achieve a SQNR of above $66\,dB$ in a signal bandwidth of $15\,MHz$, a third-order $NTF\,(z)$ with oversampling ratio of $OSR = 42$ is chosen. Further, for better stability of the 3^{rd}-order single-bit single-loop modulator, the out-of-band gain is limited to $OBG = 1.5$ [59]. Also, the complex zeros are judiciously placed inside the signal band to improve the noise-shaping performance [19].

For a stable single-bit CT-ΔΣ modulator design, it is mandatory to calculate the quantizer gain (K_q). Using appropriate modeling of the single-bit quantizer in *SIMULINK*, quantizer gain has been calculated as $K_q = 1.3759$. Figure 4.1 shows

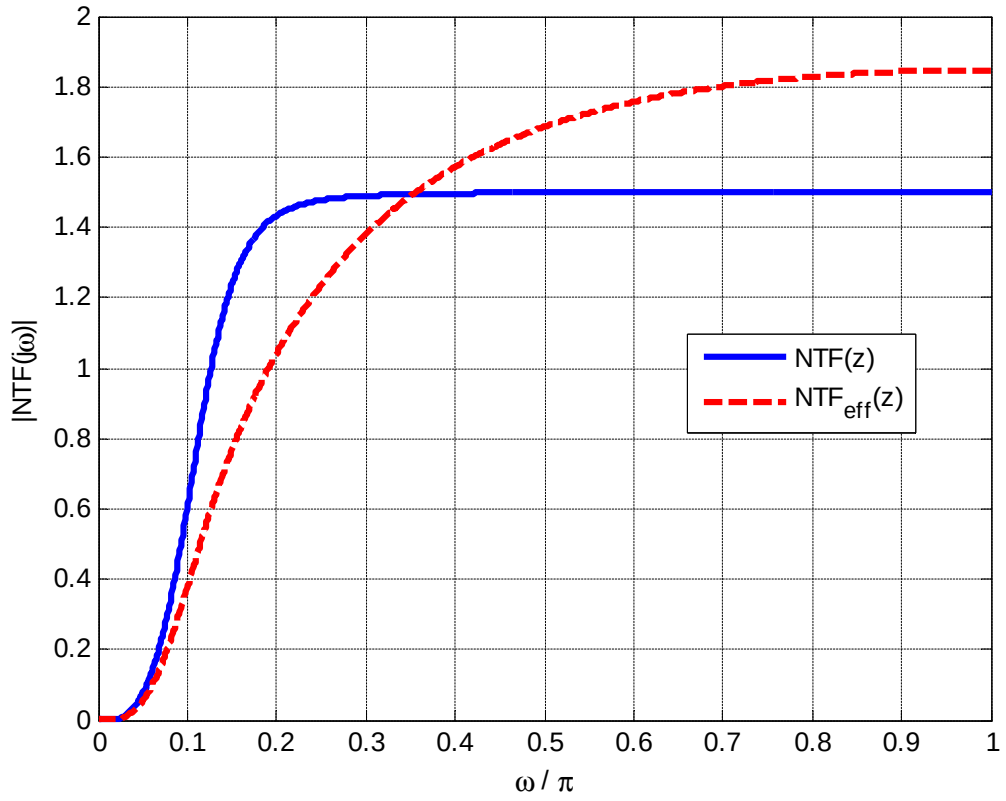

Figure 4.1: Magnitude response of the $NTF(z)$, with and without incorporating quantizer gain (K_q).

the magnitude response of the noise-transfer function with and without incorporating K_q. Thus, an effective $NTF_{eff}(z)$ is evaluated in Equation 4.1 and it can achieve a peak in-band SQNR of $77\,dB$, which is about $10\,dB$ above the desired SNR of the converter.

$$NTF_{eff}(z) = \frac{(z-1)(z^2-1.997z+1)}{(z-0.3805)(z^2-1.518z+0.6164)} \tag{4.1}$$

4.2.2 Modulator Architecture

A traditional CIFF and CIFB loop-filter architecture has already been explained in Section 3.2. In this work, in order to achieve an energy-efficient single-bit CT-$\Delta\Sigma$M, while maintaining reasonable anti-alias filtering characteristics, a combination of feed-forward and feedback compensation has been implemented, as shown in Figure 4.2(a) [60]. Although, this architecture reduces power with improved STF response, it still a requires high-speed power hungry summer for the ELD compensated direct path. In order to make this topology more power efficient, an ELD compensation scheme, which employs a digital differentiator, is used [17] as shown in Figure 4.2(b). This technique eliminates the requirement of a high-speed summing opamp. Also, note that the resonators feedback connections are not shown in Figure 4.2(a) and (b) for simplicity, but are used in the actual design described later.

There are several methods for implementing the feedback DAC, either using a SC DAC, which makes the modulator performance robust to clock jitter [58]; or CT DAC, which are either current-steering or resistive implementations [5, 6, 19]. Even though a SC DAC is robust to clock jitter, it is avoided as it severely compromises the alias-rejection of the modulator [25] and requires the first opamp f_{unity} to be at least $4-5$ times the sampling rate to avoid opamp slewing. However, achieving such an opamp f_{unity} at this sampling frequency is not a viable solution from the power dissipation prospective.

Thus, a resistive feedback NRZ DAC is used, which is highly linear and reduces the overall circuit complexity when compared to current-steering or SC ADCs. Though, a resistive DAC enables modulator operation at high sampling rate, it also increases the in-band noise contribution due to thermal noise from the large resistor and from

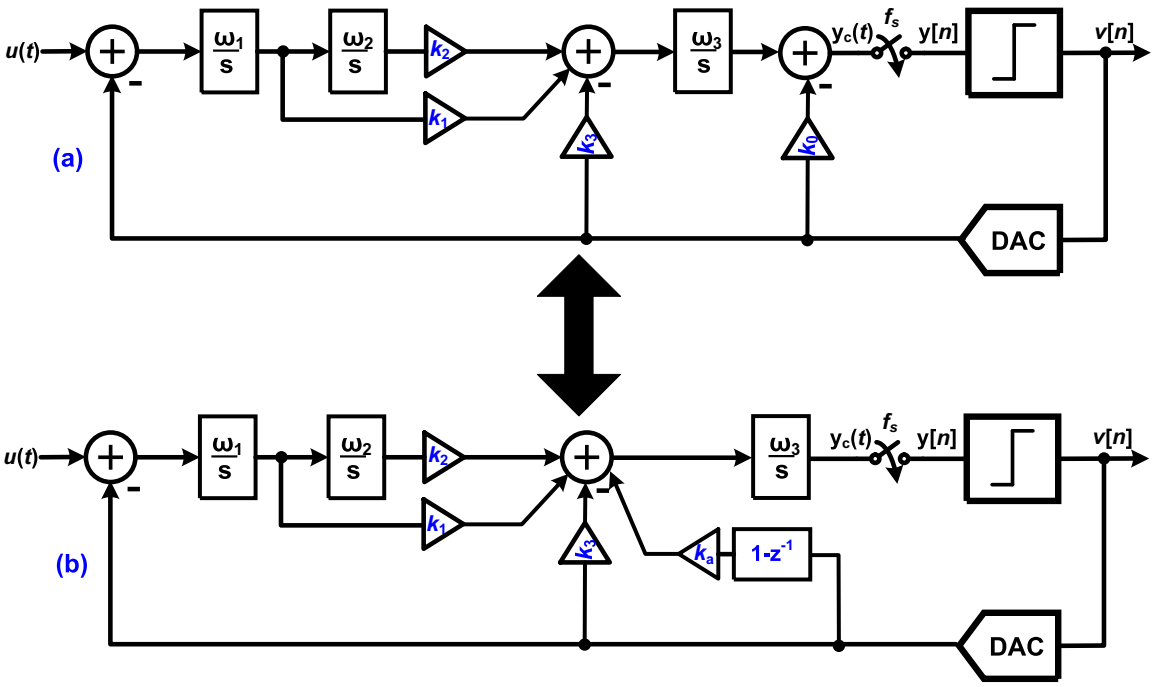

Figure 4.2: (a) Hybrid continuous-time $\Delta\Sigma$ modulator architecture with adder (b) without adder.

the clock jitter (i.e., the DAC reconstruction noise). Hence, it requires careful noise budgeting of the thermal and jitter noise sources and evaluation of the maximum tolerable clock jitter value prior to the ADC design.

4.2.3 Noise Budget

In a $\Delta\Sigma$M design, it is important to find a good balance between the different contributing noise sources [19]. Since, the quantization noise power is not purely random or white, its tonality must be considered when designing the modulator. Thus, by proper allocation of different noises in the total in-band noise budget, we estimate the expected ENOB. In this design, in order to obtain a 11-bit equivalent DR, we set the target SNR to be $67\,dB$ for an $-3\,dBFS$ sinusoidal input, which means that the power of the total in-band noise should be lower than $-70\,dBFS$. Here,

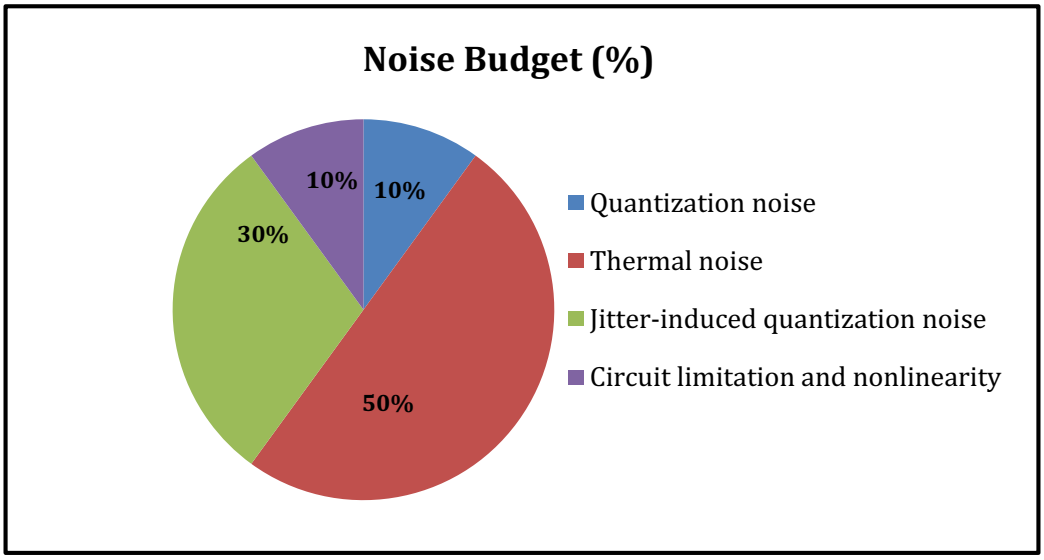

Figure 4.3: Noise Budget of single-bit CT-$\Delta\Sigma$ modulator.

dBFS denotes the power level (in dB) with respect to the full-scale input sinusoid applied to the modulator.

In the single-bit CT-$\Delta\Sigma$ modulator with NRZ DAC, we have the following noise contributions

- Quantization noise contribution from low-resolution quantizer
- Thermal noise contribution mainly from the first integrating opamp, input resistor, feedback DAC resistor, and the resistor forming the resonator
- Jitter-induced DAC reconstruction noise
- Quantizer offset and the non-linearity induced distortion resulting from circuit non-idealities

Figure 4.3 shows the pie chart of the ADC thermal noise budget in order to achieve the required ENOB. Also, Table 4.1 shows the corresponding SNR of each noise source with respect to $-3\,dBFS$ input. While only considering the thermal noise, its

Noise/Distortion Source	Noise Budget (%)	SNR (dB)
Quantization noise	10%	77
Thermal noise	50%	70
Jitter-induced quantization noise	30%	72
Circuit limitation and non linearity	10%	77

Table 4.1: Single-bit CT-$\Delta\Sigma$ modulator noise budget.

contribution in the total in-band noise is set to 40%, which means the SNR should be at least $70\,dB$ for a $-3\,dBFS$ input. Due to the gain of the first stage, the input-referred noise from following stages is greatly attenuated. If it is assumed that 80% of the total thermal noise is from the first stage, the power of the in-band thermal noise introduced by this stage should be as low as $-73\,dBFS$. The estimated noise is later used to determine the loop-filter components values.

As for the jitter-induced noise, a budget of 30% of total noise is a reasonable estimate, which implies that the SJNR should be at least $72\,dB$ to achieve the targeted SNR. Figure 4.4 shows SJNR Vs σ_{jitter} performance, normalized to T_s in percentage using a system-level simulation in *SIMULINK*. From the graph, it is clear that the jitter-induced noise power is close to $-74\,dBFS$ for 0.2% jitter. This dictates the rms jitter tolerance of the clock source as $1.6\,ps$. Although, carefully designed phase-locked loops (PLL) with LC-VCO can achieve sub-$100\,fsec$ jitter performance, it is not permissible to integrate them on the same chip in our design. Thus, special care has been taken on designing the PCB board by using an external bandpass filter, shielded clock routes off/on chip to make sure that the rms jitter of the final clock signal entering the modulator is less than $1\,ps$ [38].

Further, to determine the specifications of the quantizer offset and DAC resistor mismatch, a statistical simulation is performed in *SIMULINK*. The simulation result shows that if the value of the comparator input offset is bounded as $0.5\,LSB >$

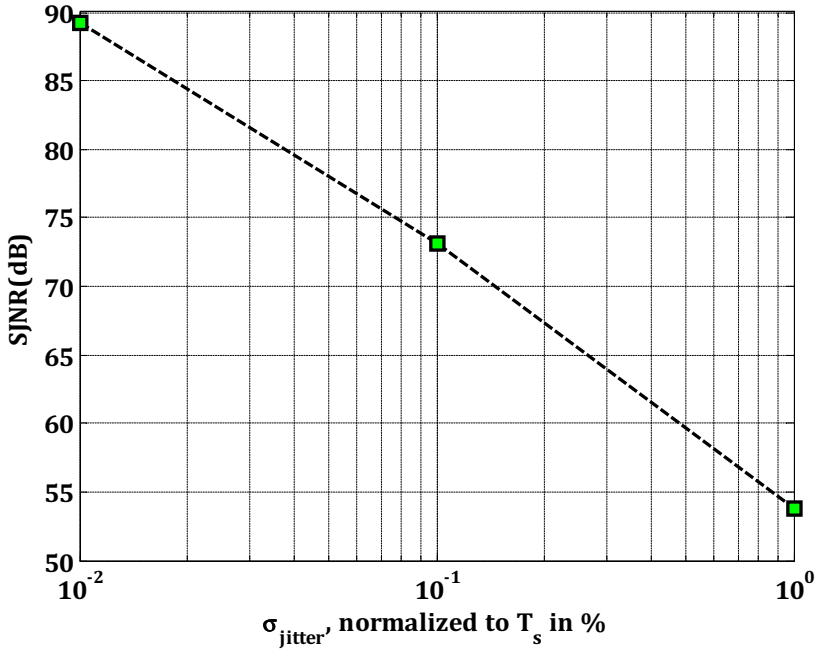

Figure 4.4: SJNR of a 3rd-order CT-$\Delta\Sigma$ modulator Vs σ_{jitter}, normalized to T_s in %.

$\sigma_{offset} > 0.1\,LSB$ and the relative mismatch between the DAC resistors is less than 1%, then the quantizer non-idealities will introduce less than 10% to the total in-band noise. Figure 4.5 shows the effect of comparator random offset and DAC resistor mismatch on in-band SNDR for each level of offset. For each offset level, 1000 trials were simulated. It is thus seen that to achieve an 11-bit performance from the modulator, random offsets in the comparator with a standard deviation of up to $0.5\,LSB$ can be easily tolerated.

4.2.4 The ABCD Matrix and Dynamic Range Scaling

The ABCD matrix representation of the CT loop-filter from Section 3.1 is indispensable for performing linear matrix operations like DRS, automated design mapping from behavioral to circuit-level schematics, systematic design centering, and for rapid

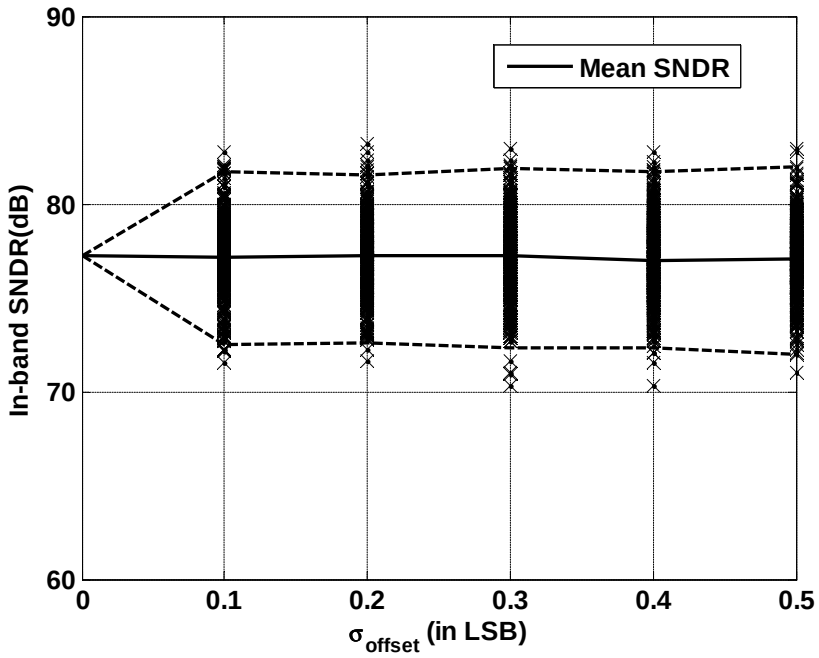

Figure 4.5: Effect of comparator random offset on in-band SNDR—for each level of offset, 1,000 trials were simulated. The lines show the modulators with the best 1% SNDR, mean SNDR and the worst 1% SNDR, respectively.

simulation of the modulator architectures. The ABCD matrix is a combination of four sub-matrices that describe the dynamics of any linear system. The state-space equations for the $\Delta\Sigma$ loop filter are described as

$$\begin{aligned} \mathbf{x}[n+1] &= A\mathbf{x}[n] + B \begin{bmatrix} u[n] \\ v[n] \end{bmatrix} \\ \mathbf{y}[n] &= C\mathbf{x}[n] + D \begin{bmatrix} u[n] \\ v[n] \end{bmatrix} \end{aligned} \tag{4.2}$$

where $\mathbf{x}(n) \in R^{M\times 1}$ is the state vector at time n for an M^{th}- order modulator. The matrix $A \in R^{M\times M}$ defines the interconnections within the loop filter. The matrix

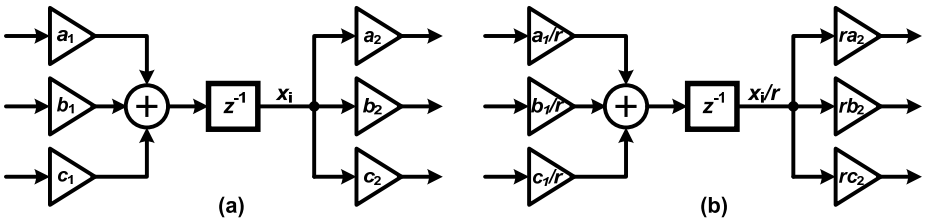

Figure 4.6: Dynamic range scaling of a loop-filter state from x_i to x_i/r.

$B \in R^{M\times 2}$ describes how the modulator input $u[n]$ and the feedback DAC output $v[n]$ are applied to the loop filter $H(z)$. The matrices $C \in R^{1\times M}$ and $D \in R^{1\times 2}$ describe the computation of the output $y[n]$ from the states $\mathbf{x}[n]$ and the loop-filter inputs $(\ u[n] \quad v[n]\ )^T$ [19]. The loop-transfer functions are obtained from the ABCD matrix as

$$\begin{bmatrix} L_0(s) \\ L_1(s) \end{bmatrix} = C\left(sI - A\right)^{-1} B + D \tag{4.3}$$

DRS is an important step in designing practical $\Delta\Sigma$ modulators. Once the CT loop-filter is synthesized from the DT loop-filter as explained in Section 3.1, the next step is to realize the loop-filter transfer function with a modulator architecture shown in Figure 4.2(b). In general, the co-efficients returned by the CT loop filter from Section 3.1 are unscaled, or the internal integrator states occupy an unspecified voltage range. In order to restrict the state range of the loop-filter states to known and practically realizable values in circuits, dynamic-range scaling must be performed [19].

In dynamic-range scaling, the ABCD matrix of the CT loop filter is mapped and scaled so that the individual state maxima are bounded by a specified limit x_{lim}. The value of x_{lim} is selected such that the opamp outputs lie within the $x_{lim} \cdot V_{DD}$ range

and linear operation of the loop filter is assured. This value is usually selected to be around $\frac{1}{3}$ to $\frac{1}{2}$ depending upon the linearity of the opamp in a feedback configuration. The maximum stable amplitude is also obtained as a result of this scaling process. In the range-scaling process, first the ratios $r_i = \frac{x_{max,i}}{x_{lim}}$ of the state maxima $x_{max,i}$ to x_{lim} are estimated through transient simulations. Then, the diagonal-scaling matrix S is formed with the inverse of these ratios and is given as [19, 61]

$$S = \begin{bmatrix} \frac{1}{r_1} & 0 & \cdots & 0 \\ 0 & \frac{1}{r_2} & \cdots & \vdots \\ \vdots & \vdots & \ddots & 0 \\ 0 & \cdots & 0 & \frac{1}{r_M} \end{bmatrix} \tag{4.4}$$

Then, the scaling matrix, S, is applied on the state vector to obtain the scaled state vector $\mathbf{x_s} = S\mathbf{x}$. This ensures that all the states are bounded within x_{lim}. The resulting ABCD matrix after dynamic-range scaling is given by

$$ABCD_s = \left[\begin{array}{c|c} SAS^{-1} & SB \\ \hline CS^{-1} & D \end{array}\right] \tag{4.5}$$

The dynamic range scaling process is illustrated in Figure 4.6 where a single state in the loop filter is range scaled by r. From the 3^{th}-order feed-forward and feedback hybrid topology shown in Figure 4.2, the state space (ABCD) matrices of the modulator can be written as

$$A = \begin{bmatrix} 0 & -g_1\omega_1 & 0 \\ \omega_2 & 0 & 0 \\ k_1\omega_3 & k_2\omega_2 & 0 \end{bmatrix} \quad B = \begin{bmatrix} -\omega_1 & \omega_1 \\ 0 & 0 \\ -k_3\omega_3 & 0 \end{bmatrix}$$
$$C = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix} \qquad D = \begin{bmatrix} k_a & 0 \end{bmatrix} \tag{4.6}$$

Thus, the resultant parametric transfer functions $L_0(s)$ and $L_1(s)$ are given by

$$\begin{bmatrix} L_0(s) \\ L_1(s) \end{bmatrix} = \begin{bmatrix} \frac{-\left(k_0 s^3 + k_3\omega_3 s^2 + (g_1 k_a \omega_1\omega_2 + k_1\omega_1\omega_3)s + (k_2\omega_1\omega_2\omega_3 + g_1 k_3 \omega_1\omega_2\omega_3)\right)}{(s^3 + g_1\omega_1\omega_2 s)} \\ \frac{(k_1\omega_1\omega_3)s + (k_2\omega_1\omega_2\omega_3)}{(s^3 + g_1\omega_1\omega_2 s)} \end{bmatrix} \tag{4.7}$$

Using Equation 4.5 and an appropriate scaling matrix, S, the states of each integrators are scaled to $\frac{1}{3}$ of full-scale when the input is at $-3\,dBFS$. Figure 4.7 shows the histogram plot of each state normalized to the full-scale range. This also clearly shows that the 3^{rd} integrator does not need to accommodate a full-scale swing when the input is at $-3\,dBFS$.

4.3 Circuit-Level Design

This section describes the comprehensive design of circuit blocks used in the wideband single-bit CT-$\Delta\Sigma$ modulator in detail with simulation results over different corners. Also, it presents the analytical results of noise analysis of the first opamp (dominant noise source) and the feedback DAC to meet the thermal noise contribution to the overall in-band noise.

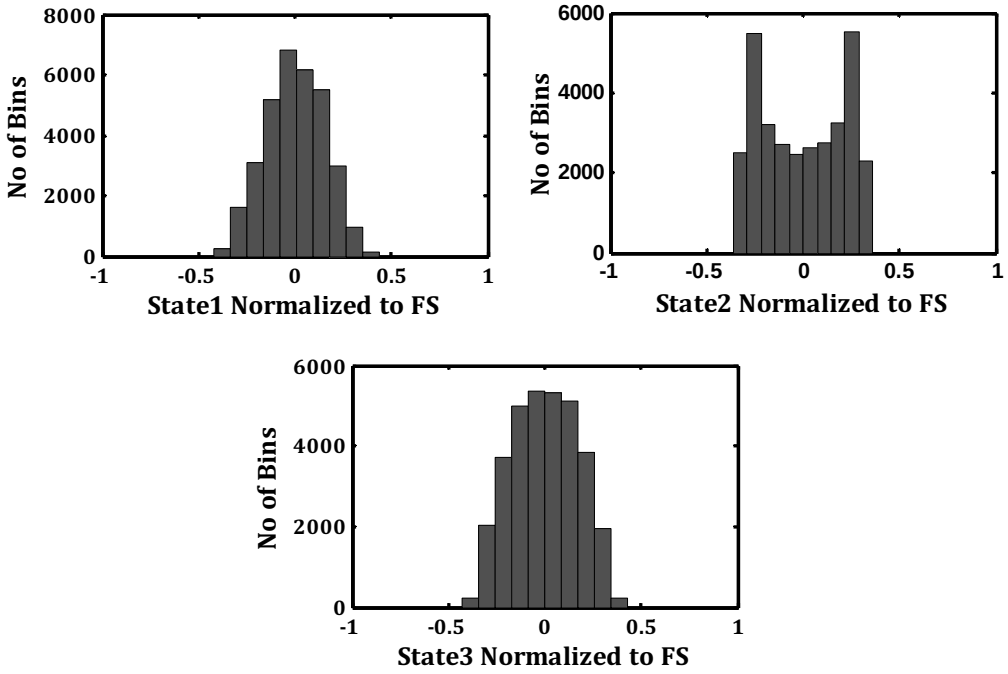

Figure 4.7: Histogram of scaled integrator states normalized to full-scale when input is $-3\,dBFS$.

4.3.1 Loop-Filter Design

Using the methodology discussed in the previous section, the architecture and loop-filter coefficients of the modulator were determined. Now, it is required to translate these coefficients into the practically realizable values of the resistors and capacitors in the transistor-level implementation of the modulator. As discussed in Section 3.5.1, the active-RC integrators exhibit better linearity and larger signal swing than the $G_m - C$ counterparts (for the same power budget), which are used to design the CT loop filter. Figure 4.8 shows the top-level circuit diagram of the modulator whose loop filter is composed of active-RC integrators, a single-bit quantizer (essentially a high-speed regenerative comparator) and feedback resistive DAC. Also, in Figure 4.8, it can be seen that the integration capacitor in each stage is realized using a capacitor

array whose equivalent capacitance is tuned digitally [19, 38, 39].

4.3.2 Component Selection Based on Thermal Noise Budget

As discussed in Section 4.2.3, the thermal noise contribution from the first integrator, feedback DAC, and resonator is 40% of the total in-band thermal and flicker noise. Thus, the proper selection of these components play a crucial role in overall modulator performance. Figure 4.9 shows the simplified front-end circuit schematic [19, 38, 39].

From the simplified circuit schematic, the total input-referred noise power spectral density from R_1 is given as

$$v_{R_1}^2 = 4kTR_1 \tag{4.8}$$

Similarly, the total input-refereed noise from R_{g1} can be written as

$$v_{R_{g1}}^2(f) = \frac{4kTR_{g1}\left|\frac{1}{j2\pi fR_{g1}C_1}\right|^2}{\left|\frac{1}{j2\pi fR_1C_1}\right|^2} = \frac{4kTR_1^2}{R_{g1}} \tag{4.9}$$

Thus, the total input-inferred noise PSD of R_1 (from the 1^{st} integrator and feedback DAC) and R_{g1}in the differential circuit can be approximated as

$$v_{Resistors}^2(f) = 4kTR_1\left(4 + \frac{R_1}{R_{g1}}\right) \approx 16kTR_1|_{R_{g1}>R_1} \tag{4.10}$$

Another main thermal noise contributor is from the 1^{st} stage of the opamp used in the 1^{st} integrator as shown in Figure 4.10. By performing noise analysis on the first stage, we get [62]

$$v_{Opamp}^2(f) = 4kT\left(\frac{4}{3g_{m1,2}} + 2\frac{2g_{m7,8}}{3g_{m1,2}^2}\right) \tag{4.11}$$

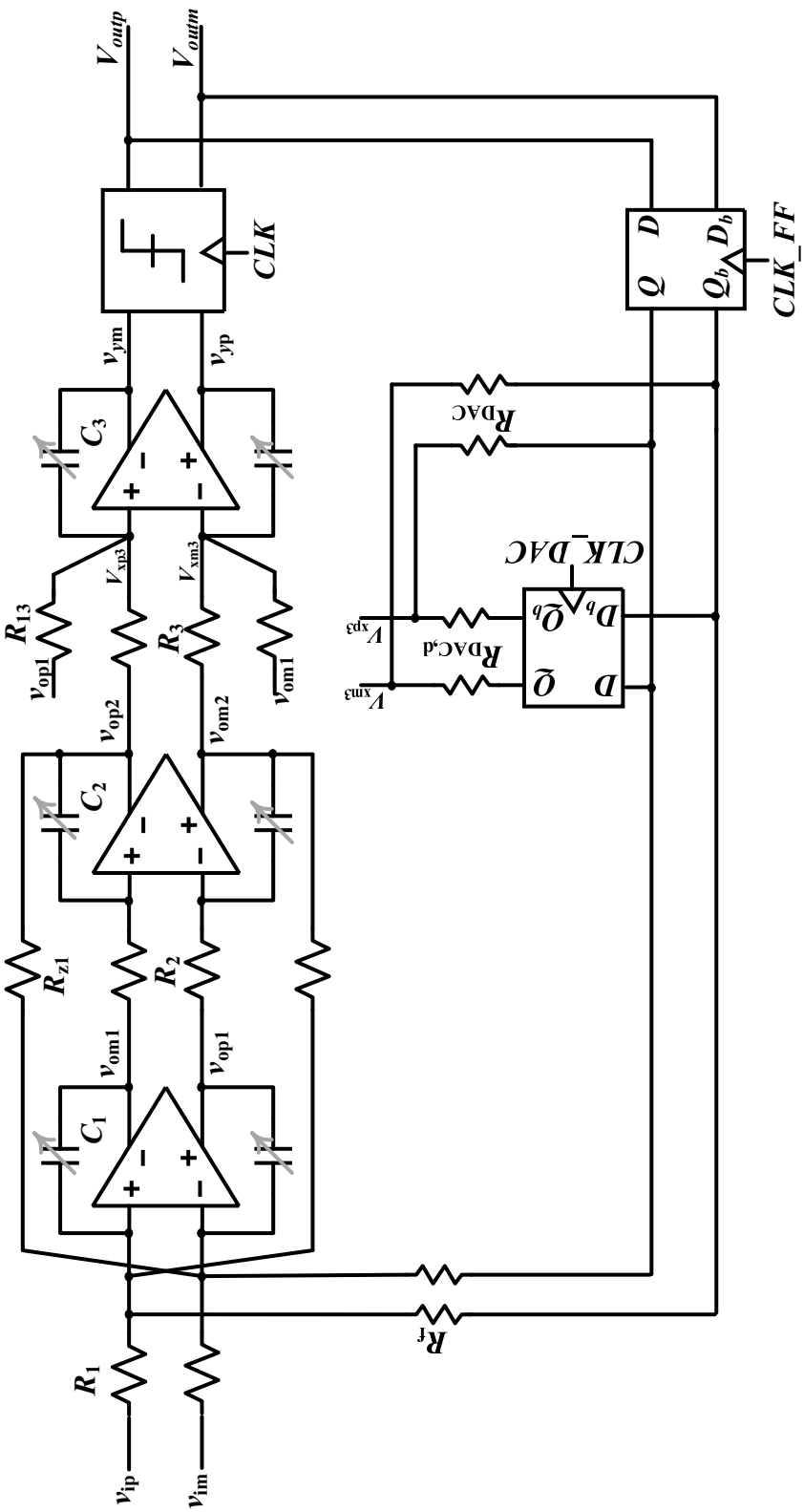

Figure 4.8: Top-level circuit diagram of the single-bit CT-$\Delta\Sigma$ modulator.

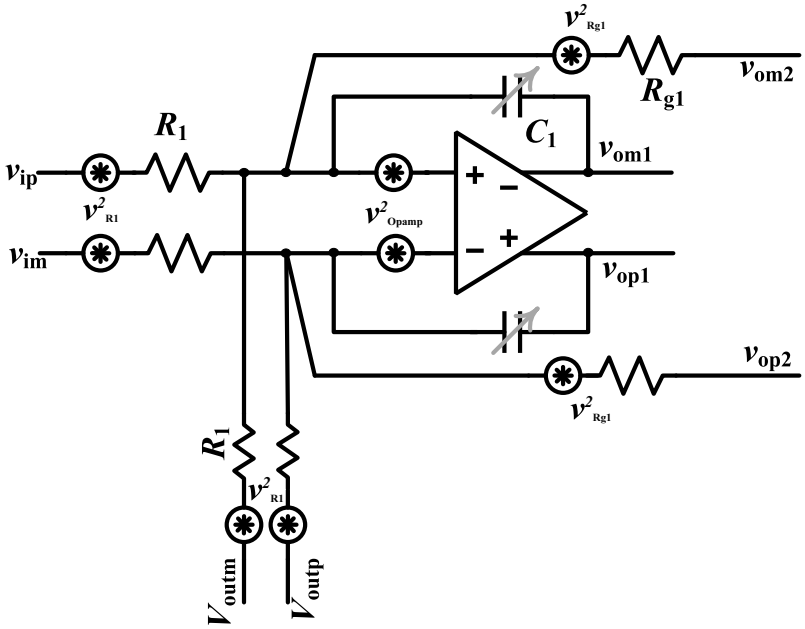

Figure 4.9: Simplified front-end circuit of $\Delta\Sigma$M with primary noise sources.

The above equations clearly show that the primary noise contributors are $M_1 - M_2$ and $M_7 - M_8$, excluding the cascode devices. After referring this noise to the input of the modulator, we can the get following input referred noise PSD of the opamp as

$$v^2_{Opamp,Modin}(f) = v^2_{Opamp}(f)\, R_{g1}\, |1 + j2\pi f R_1 C_1|^2 \tag{4.12}$$

According to the noise budget shown in Figure 4.3 and Table 4.1, the in-band thermal noise power should be less than $-74\,dBFS$, which leads to the following inequality

$$10log_{10}\left(\int_0^{BW}\left(v^2_{Resistors}(f) + v^2_{Opamp,Modin}(f)\right)\right) \leq -74\,dB \tag{4.13}$$

The noise analysis is performed using *spectre* with the designed opamp and selecting $R_1 = R_f = 6\,K\Omega$ and $R_{g1} = 44\,K\Omega$. The resultant total thermal and flicker noise

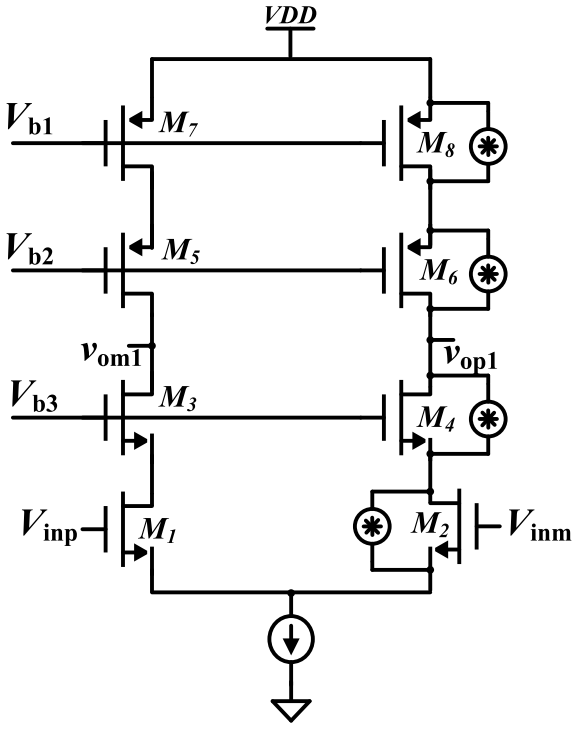

Figure 4.10: Noise in 1^{st} stage (telescopic) of 1^{st} integrator (For simplicity, noise is shown only on one side).

integrated across the band of interest is $15.778\,nV^2$ or $-78\,dB$. Of the total noise, 56% of thermal and flicker noise is introduced by the input, DAC, and resonator resistors and 44% of the thermal noise is generated by the first operational amplifier. Thus, the resultant SNR is $75\,dB$, which is $5\,dB$ more than the thermal noise budget. The other component values are chosen based on loading, linearity, and power budget of the opamps.

4.3.3 Operational Amplifier

The first integrator determines the overall noise and linearity of the modulator [33]. Therefore, the first opamp is required to a have a low input referred noise and a high unity gain frequency. The opamp topology shown in Figure 4.11 is used for

Corners	A_{dc}(dB)	f_{Unity}	PM_{DM}	UGB_{CMFB1}	PM_{CMFB1}	UGB_{CMFB2}	PM_{CMFB2}
Typical	61	$2.83\,GHz$	92°	$39\,MHz$	70°	$138\,MHz$	57.06°
SF (worst case)	62	$2.51\,GHz$	92.5°	$31.48\,MHz$	74.13°	$81.35\,MHz$	57.83°

Table 4.2: Simulation summary of the 1^{st}- integrator RC-extracted opamp using the second integrator as the load.

the first three active-RC stages, with a gradual reduction in bias currents (and hence power dissipation) from the first to third stage. The opamp is a two-stage design that uses feed-forward compensation [63]. The feed-forward compensated architecture is fundamentally more efficient when compared to a Miller compensated design, as the power is not wasted in charging and discharging of large compensation capacitors [63]. The first opamp sets the overall noise and non-linearity for the modulator and thus it consumes largest amount of power in the loop filter.

The first stage consists of long-channel large-area devices to lower the input referred flicker (or $\frac{1}{f}$) noise. A telescopic cascode load with NMOS input-pair stage ($M_1$and M_2) is used to obtain a high DC gain in the first stage. The feed-forward path is realized using another NMOS differential pair (M_{10} and M_{11}), which reuses the bias current of $M_{12}$and M_{13}, or second-stage, g_{m2}. Since the feed-forward path, g_{m3}, shares the bias current with g_{m2}, the opamp topology results in highly optimized power dissipation. The total current drawn by the first stage of the opamp including bias is $216\,\mu A$.

The output of first stage (v_{o1p} and v_{o1m}) is averaged through a differential pair and compared to reference V_{b2} to tune the output common-mode feedback voltage (V_{CMFB1}). Since the transistor-based detector is used to detect the common-mode voltage of the first stage, the DC gain is not degraded. Also, to help stabilize the loop formed by the 1^{st}-stage and CMFB1 detector, $300\,fF$ Miller compensation capacitors

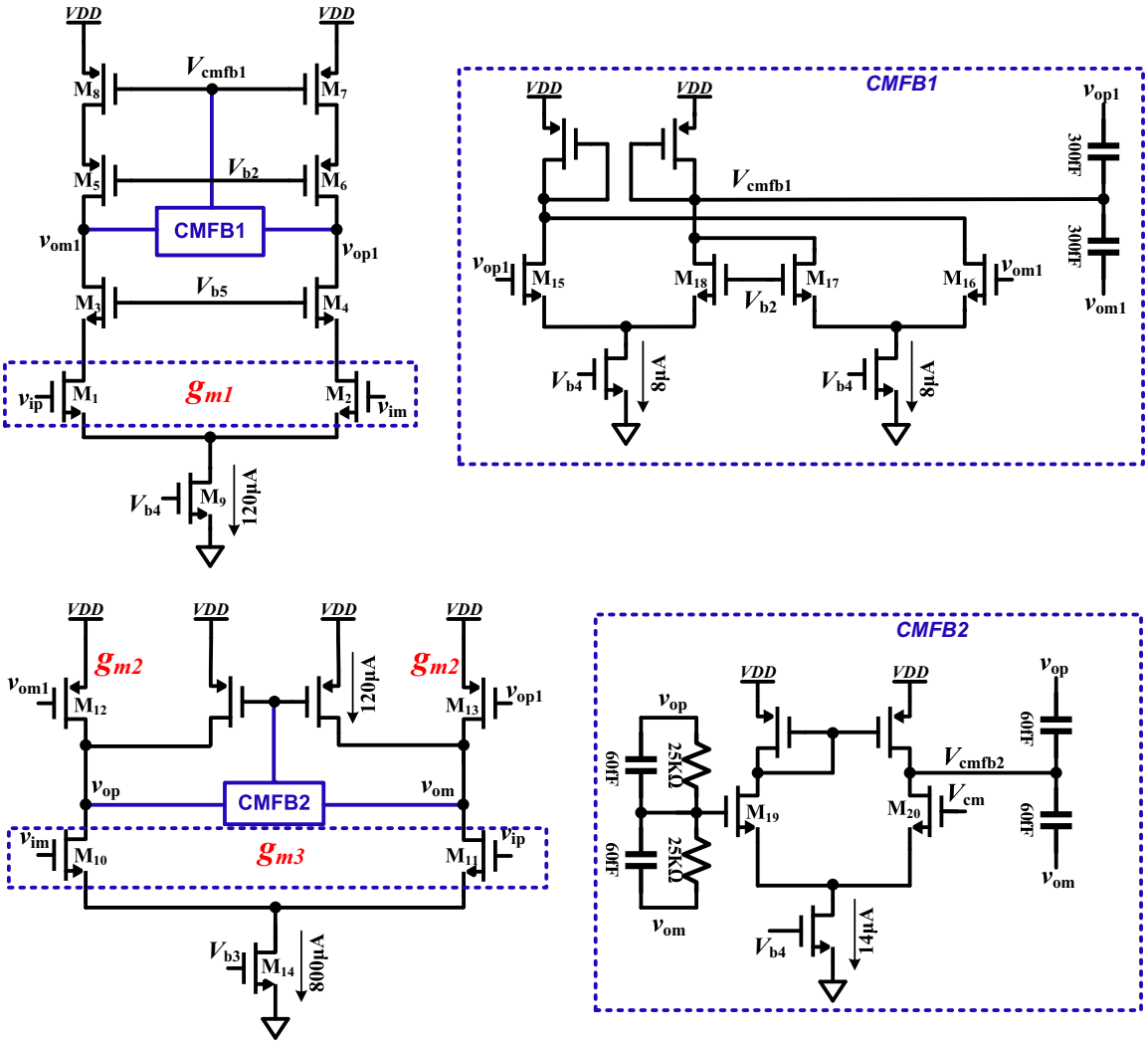

Figure 4.11: Two-stage feed-forward compensated opamp with CMFB circuit used in first three integrators.

are used for pole-spitting in the common-mode (CM) signal path. Similarly, the CMFB2 circuit shown in Figure 4.11 uses resistors to average the output nodes (v_{op} and v_{om}) and feed to the input transistor (M_{19}) and compare it to V_{cm} to tune the output common-mode feedback voltage (V_{CMFB2}). The $60\,fF$ capacitors in parallel with the $25\,K\Omega$ resistor provide a fast high-frequency path, bypassing the resistive common-mode detector and the error amplifier. The total current drawn by the first

opamp, including the CMFB circuitry and bias, is $1.03\,mA$ from the $1.2\,V$ supply. The opamp used in the subsequent integrators are similar to the first opamp, except that they are appropriately power scaled. Further, to accommodate process variation, opamp currents can be tuned using digital control bits.

Table 4.2 summarizes the simulation results for the 1^{st} integrator opamp in typical and worst (SF :-3σ variations on NMOS and PMOS and $+3\sigma$ variation on resistor) corner models. The open-loop DC gain (A_{dc}) of the opamp is $61\,dB$ (typical) and $62\,dB$ (SF). The unity gain frequency of the differential loop (f_{Unity}) is $2.85\,GHz$ with a phase margin of 92°, which is 2.5 times the sampling frequency. And the worst case UGB_{DM} is $2.51\,GHz$ with a 92.5° phase margin. Figure 4.12 shows the UGB_{DM} and PM_{DM} from the stability analysis of the 1^{st}- integerator's RC-extracted opamp using second integrator as load. Figure 4.13 and 4.14 show results of stability analysis of CMFB1 and CMFB2. The total current current drawn by all three opamps or the loop filter is $2.5\,mA$.

4.3.4 High-Speed Comparator

In this design, the ADC must complete its quantizing operation in half a clock period ($< 400\,ps$), which severely limits the choice for a suitable comparator architecture. Considering the need for speed and dynamic power, a two-stage regenerative comparator consisting of a double-tail sense amplifier, an input latch stage and a sense-amplifier-based flip-flop as the second stage are used. Since it is a single-bit quantizer, the last integrator itself can be used for pre-amplification, thus the comparator doesn't require an additional pre-amplifier, which further saves power.

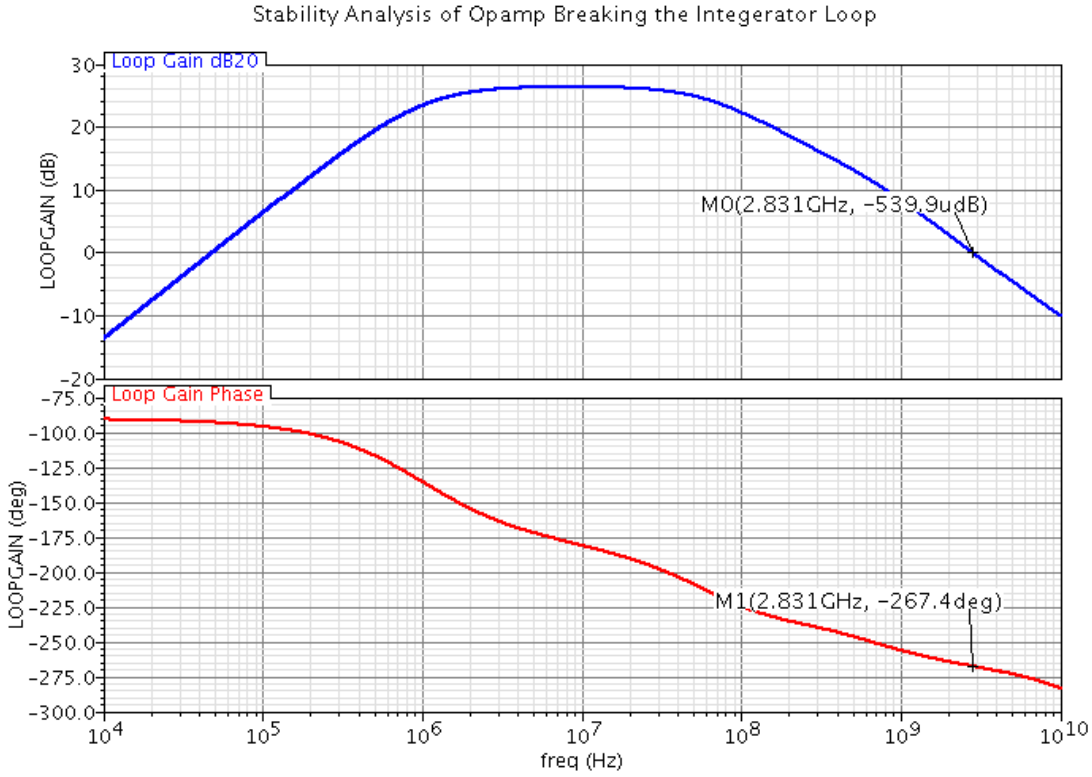

Figure 4.12: Stability analysis of 1^{st}-integrator RC-extracted opamp using the second integrator as load.

4.3.4.1 Double-Tail Sense Amplifier

Figure 4.15 shows the double-tail sense amplifier used in the comparator [64]. It is comprised of two tails: a tail for an input stage and another for the latching stage. The input tail has a wide input range and consumes small current. The output latching stage consumes large current based on the requirement of the regenerative time constant [64]. Also, the input stage has been decoupled from the output regenerative latch stage and thus the kickback noise is mitigated.

The operation of the double-tail sense amplifier is described as follows. When $CLK = 0$, transistors M_4 and M_5 will precharge the V_{xp} and V_{xm} nodes to V_{dd},

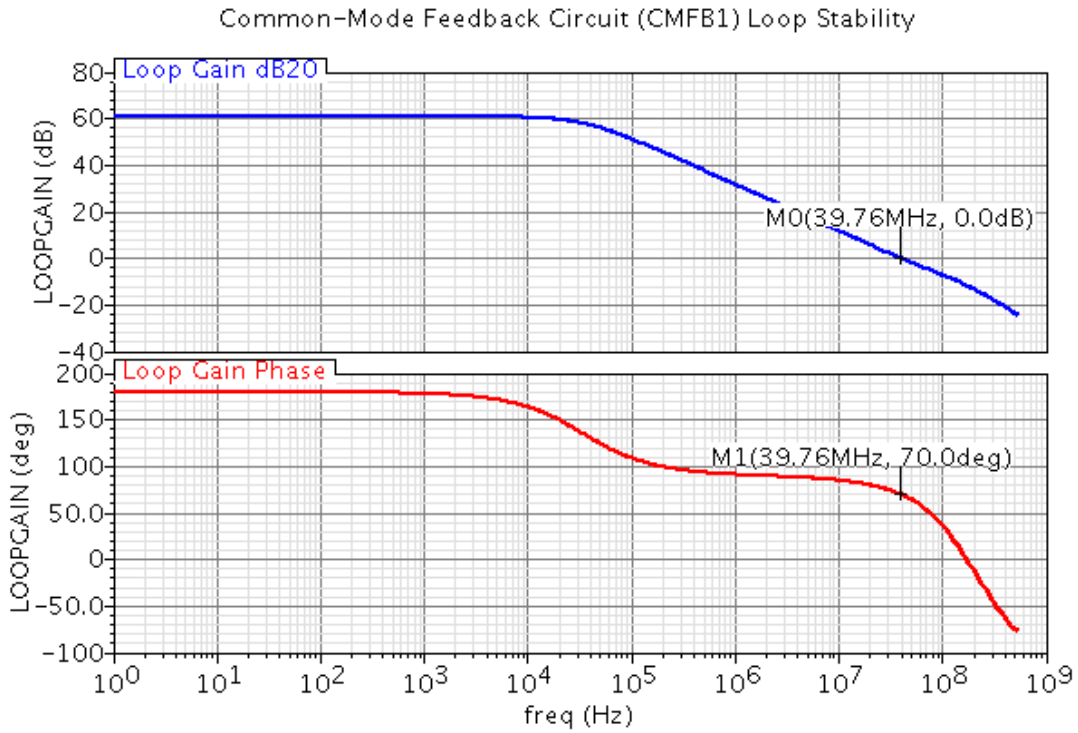

Figure 4.13: Stability analysis of 1^{st} stage CMFB.

which in turn causes M_6 and M_7 to discharge the output nodes (V_{outp} and V_{outm}) to ground. Therefore, there is no need of a reset phase at the output nodes. After the reset phase or $CLK = V_{dd}$, the tail transistors M_3 and M_{12} turn on and make V_{xp} and V_{xm} nodes to drop with a rate defined by $\frac{I_{M3}}{C_{xp}}\triangle t + \triangle V_{in}$ where $\triangle V_{in}$ is an input-dependent differential voltage. The intermediate stage formed by M_6 and M_7 creates an imbalance at the cross-coupled inverters regenerative nodes (V_{outp} and V_{outm}) [64]. The cross-coupled inverters start to regenerate the voltage difference and clamp the outputs to ground and V_{dd}. Figure 4.16 shows the regeneration time of the comparator when the input signal is $1\,mV$ using typical and SF corners. The worst case regeneration time of the comparator under loaded condition is $310\,ps$ in simulation.

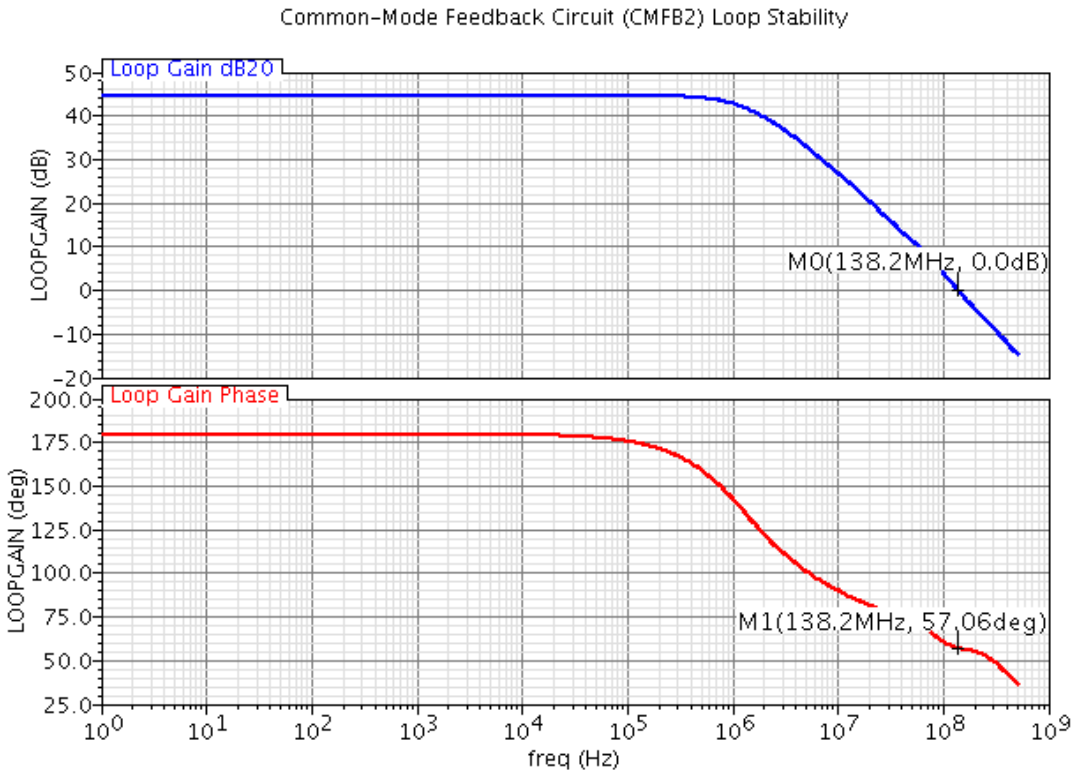

Figure 4.14: Stability analysis of 2^{nd} stage CMFB.

4.3.4.2 Sense-Amplifier-Based Flip-Flop

The Sense-Amplifier-Based Flip-Flop (SAFF) consists of two stages: the sense amplifier in the first stage and the slave set-reset (SR) latch in the second stage, as shown in Figure 4.17 [65]. The complete operation of the SAFF is as follows [65]. The input sense amplifier stage (M_1 and M_2) senses the true and complementary differential input signals (V_{inp} and V_{inm}). Following the leading clock edge ($CLK = 0$), the output nodes of the sense amplifier stage, V_{xp} and V_{xm}, are precharged to V_{dd} through M_8 and M_9, respectively [65]. Also, the drains of the input pairs are brought together or charged to $V_{dd} - V_{thn,M4,5}$ as M_3 is off or has no path to ground. The sizes of these transistors (M_8 and M_9) are chosen based on their ability to precharge these nodes

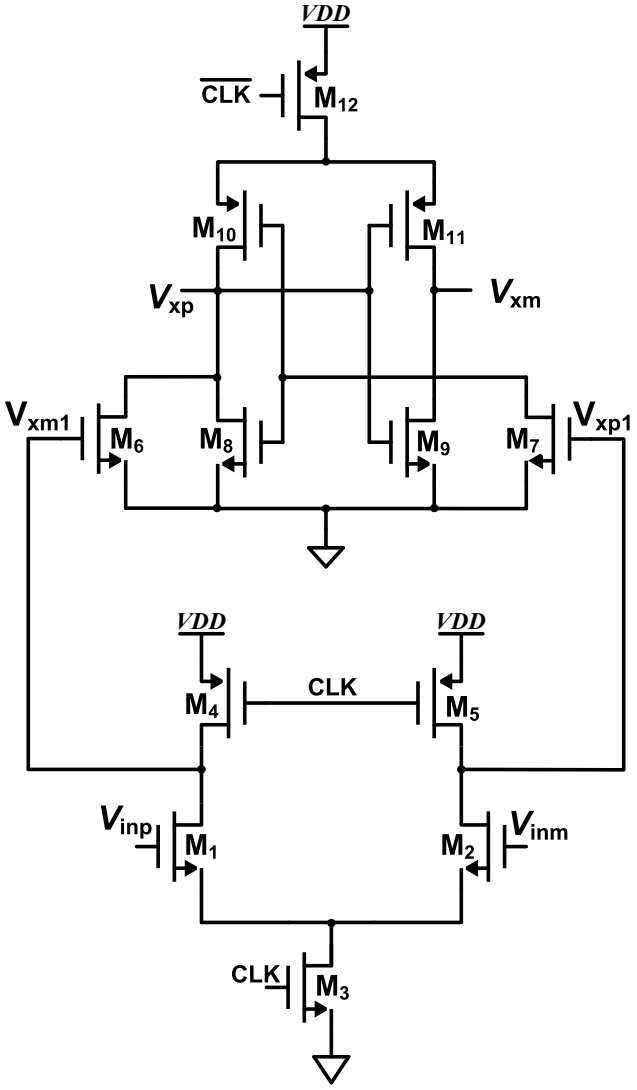

Figure 4.15: High-Speed double-tail latch-type voltage sense amplifier used as a comparator.

in half of the clock cycle. Therefore, prior to the rising edge of the clock, all the capacitances in the circuit are precharged to their respective voltages.

When CLK is high ($CLK = V_{dd}$), depending upon the differential inputs, either V_{xp} or V_{xm} is discharged either through M_4, M_1, and M_3 or M_5, M_2, and M_3, respectively. This creates an imbalance in the cross-coupled latch and pulls these nodes to

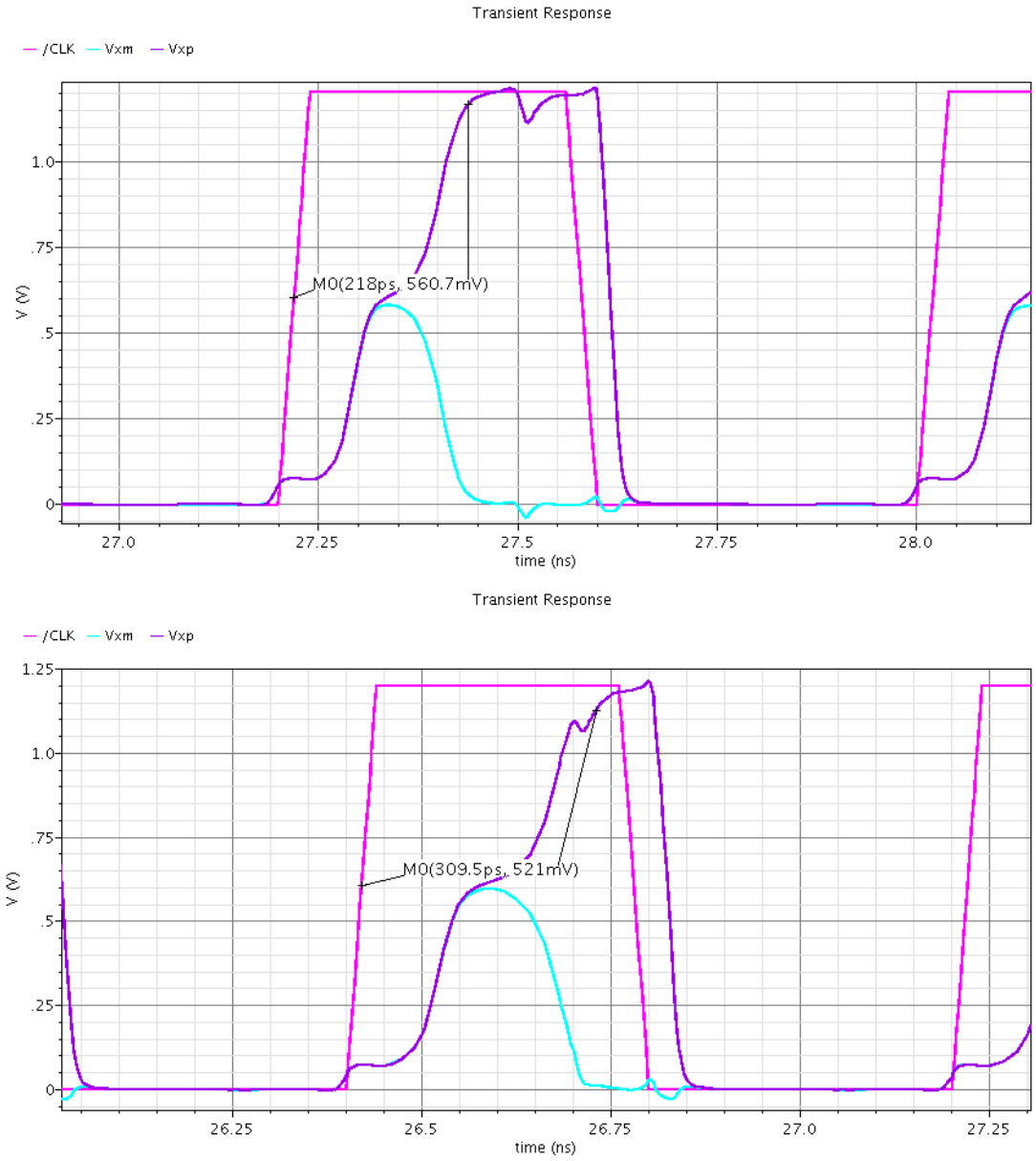

Figure 4.16: RC-extracted comparator regeneration time for 1 mV differential signal (top: typical and bottom: SF corner models).

either V_{dd} or 0, which sets the SR latch. Any subsequent change of the data during the active clock interval will not affect the output of the sense amplifier due to the presence of M_{10}. The SR latch captures the transition and holds the state until the

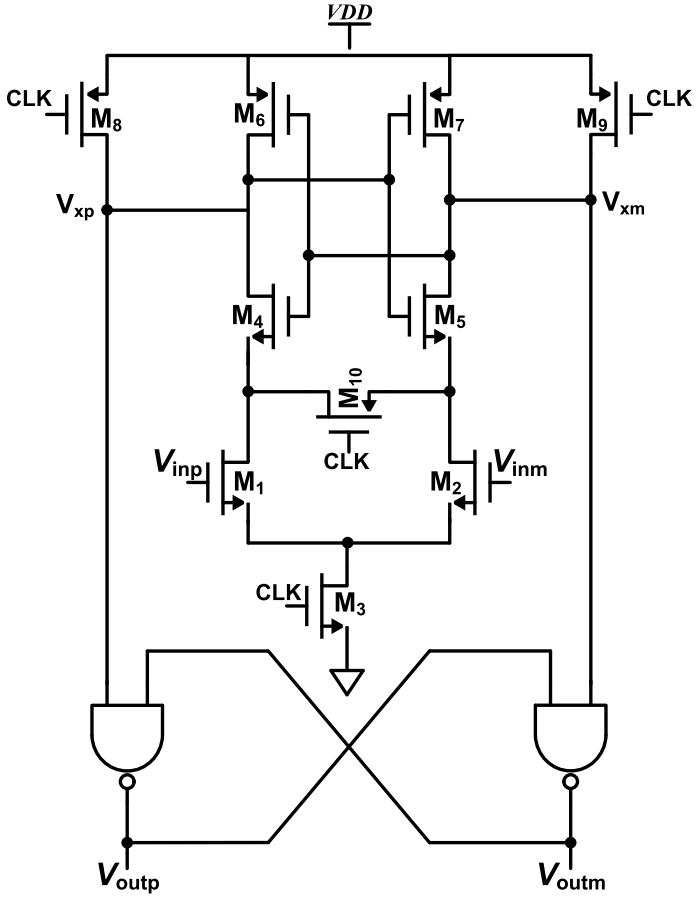

Figure 4.17: Schematic of sense-amplifier-based flip-flop.

next rising edge of the clock arrives. After the clock returns to the inactive state or the other half of the cycle, both outputs of the sense amplifier stage assume logic one or V_{dd} value. Therefore, the whole structure acts as a high-speed flip-flop.

Figure 4.18 shows the Monte-Carlo simulation results of the comparator input referred offset for 300 simulation runs. The input transistors are chosen such that the random offset of the comparator (i.e., $\sigma_{offset} < 0.05\,LSB$). Thus, the comparator non-idealities do not affect the SNDR performance of the modulator.

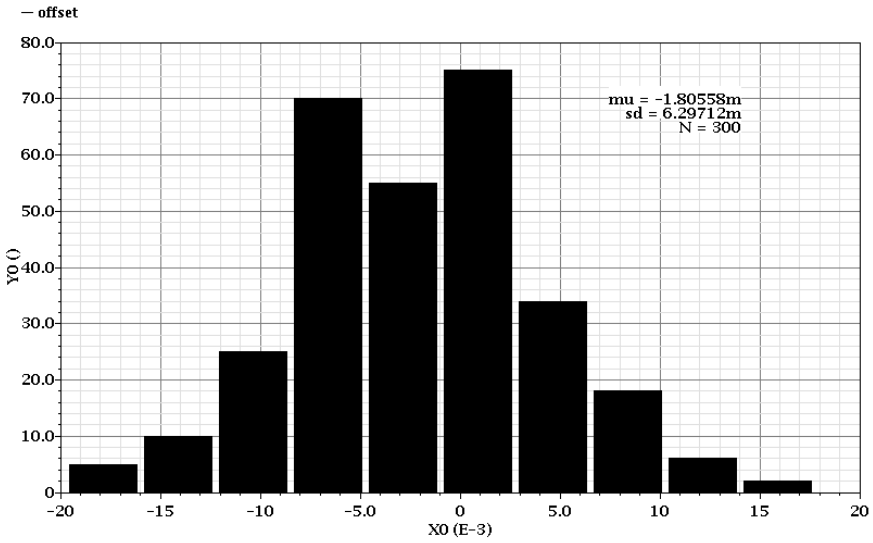

Figure 4.18: Monte-Carlo simulation of comparator input referred offset.

4.3.5 Clocking and Timing

To preserve a low jitter clock on-chip from the board, an experimental set up shown in Figure 4.19 is used. A pair of sinusoidal differential clock inputs are generated on the board and fed to the chip pad (CLK_{inp} and CLK_{inm}) [38]. Inside the test chip, this differential clock signal is transformed to a single-ended clock using a simple differential input to the single-ended output amplifier. This way, any common-mode noise coupled from the test board to on-chip is removed [38]. Also, it is better to use as few clock driver stages as possible to generate the low-jitter clock with sufficient driving capability, because any extra stages will introduce extra device noise, which will increase the clock jitter (or equivalently the phase noise). To reduce the effect of supply noise, a dedicated and clean supply $CVDD$ is used solely for the low-jitter clock generation circuit.

In this single-bit CT-$\Delta\Sigma$M, the clock signals are mainly used in the comparator

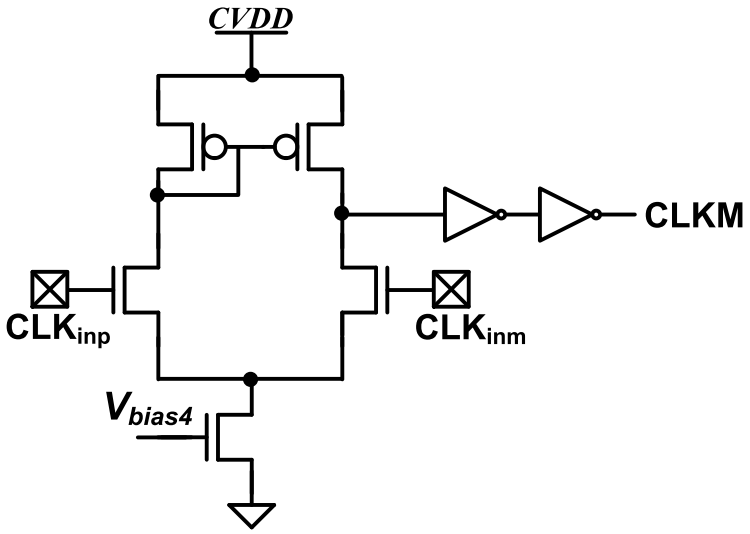

Figure 4.19: On-chip low-jitter differential-to-signal ended clock generator.

and flip-flops. Figure 4.20 shows the simplified schematic diagram of the multi-phase clock generator used to generate clocks for the comparator and the feedback flip-flop clocking. The simplified timing relationship between these clock signals are shown in Figure 4.21. $CLKM$ in Figure 4.20 is generated from Figure 4.19.

With reference to the timing diagram, the ADC is clocked at the rising edge of the CLK phase. After allowing a maximum regeneration time of $\approx 300\,ps$ (simulated under different process corners), the comparator flip-flop is clocked in $CLK\,FF$ phase. The maximum estimated delay of the flip-flop is $< 100\,ps$. Thus, the total maximum delay from rising edge of the clock to the DAC output is set to $\leq 400\,ps = 0.5T_s$. Ideally, the differentiator fast path has to be clocked at the CLK phase. However, the excess delay introduced by the flip-flop, in the critical signal path, can degrade the performance or even render the modulator unstable. Thus, to avoid the instability concerns, the feedback fast path is clocked by the CLK_{DAC} phase (i.e., an earlier phase than the conventional design to compensate for this delay).

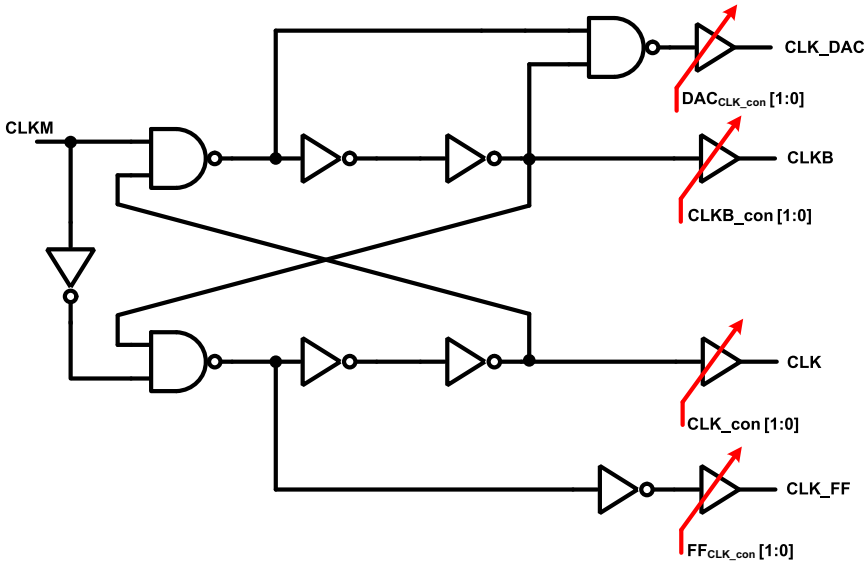

Figure 4.20: Schematic of the multi-phase clock generator.

Considering various PVT, the required amount of this time advance is variable. Thus, the variable delay cells with MUX-ed output are used on all the clock phases to suitably adjust the delays. Ideally, the delays on the path is initially set to zero. And, the delay value can be adjusted by controlling the digital control bits of the MUX.

4.3.6 Time Constant Tuning

As discussed in Section 3.5.2, due to the PVT variation, the RC time-constant of the integrators can vary by as much as ±40%, which will significantly affect the noise shaping performance of the modulator and even drive it to instability [38]. A 4-bit binary-weighted tunable capacitor array is used for the integration capacitor in each of the integrators. In each of these banks, a fixed capacitor, C, is used as the base capacitance. The minimum and maximum available capacitances of the capacitor bank are

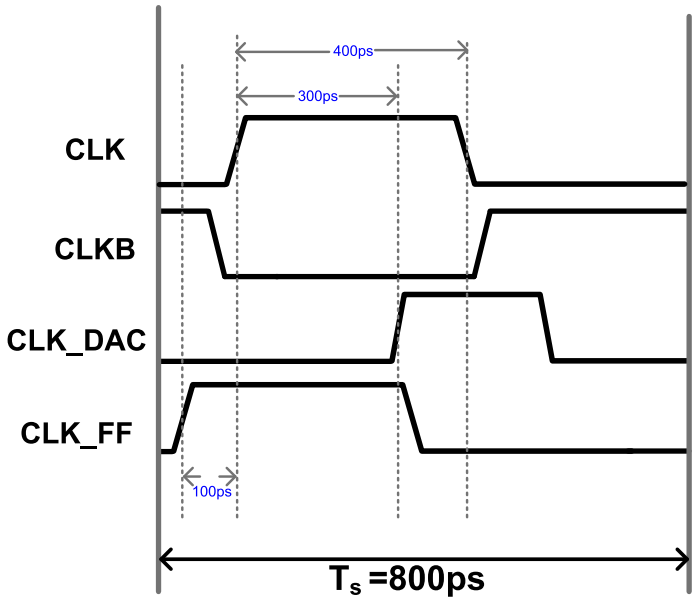

Figure 4.21: Timing relationship between different clock signals.

$$C_{min} = C; \;\; C_{max} = 2.31C \tag{4.14}$$

Thus, the tuning range of the capacitor array is

$$Tuning\,range = \frac{C_{max}}{C_{min}} = 2.31 \tag{4.15}$$

and the tuning resolution from the nominal value is

$$Tuning\,Resolution = \frac{C_{LSB}}{C_{nominal}} = \frac{0.08C}{1.71C} = 4.6\% \tag{4.16}$$

4.4 PCB Test Board Design and Test Setup

To achieve a low-noise experimental environment, a good prototyping board design and equipment setup are of utmost importance. A four-layer printed circuit board

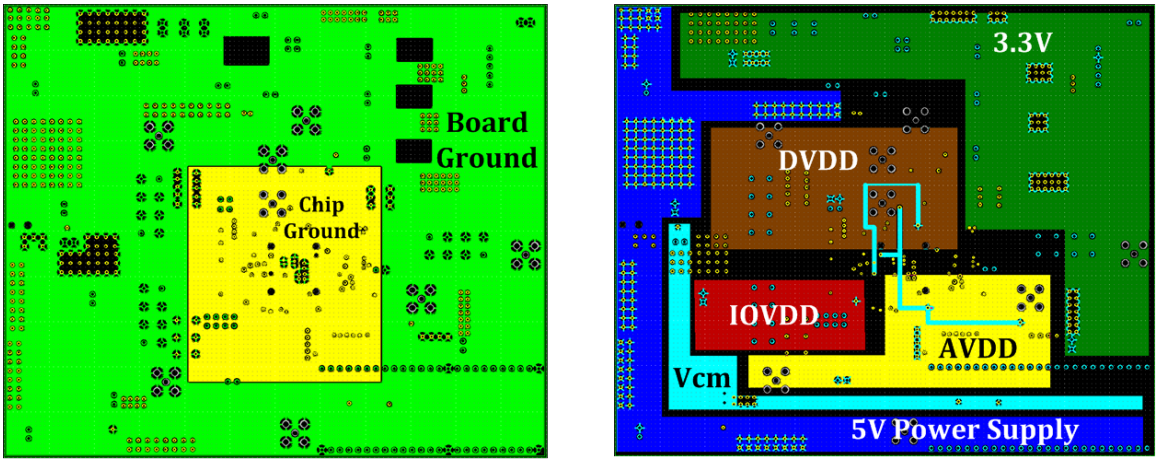

Figure 4.22: (a) Ground plane and (b) power plane of the test board.

(PCB) is designed, whose top and bottom layers are mainly used to route the components and signal traces. The second layer is dedicated to the ground, where it is divided into chip ground and board ground as shown in Figure 4.22(a). Both the grounds are connected using appropriate ferrite beads for noise isolation. Similarly, the third layer is used for power, where it is divided into several power sub-planes (*AVDD*, *DVDD*, *IOVDD, VCM,* and $\pm 3.3\,V$) as shown in Figure 4.22(b). Each of these power supplies are generated using a low noise, high PSRR, low dropout (LDO) regulator, *LD1117S12TR*. The regulator outputs are properly decoupled by a $10\,\mu F$ tantalum capacitor to keep the utmost constant output voltage with as low dropout as possible during any transient. In addition, at each supply pin of the prototype chip, a ceramic capacitor bank, which comprises $0.1\,\mu F$, $0.01\,\mu F$, and $10\,\mu F$, are placed as close as possible to decouple the high-frequency noise.

The PCB block diagram along with the test setup is shown in Figure 4.23. From Figure 4.23, it is clear that the reference voltages are generated by the low-noise $12-bit$ DAC ($AD5624R$), which are buffered using an ultra-low noise opamp ($AD8045$) and given to the test chip. All these reference voltages are appropriately bypassed with

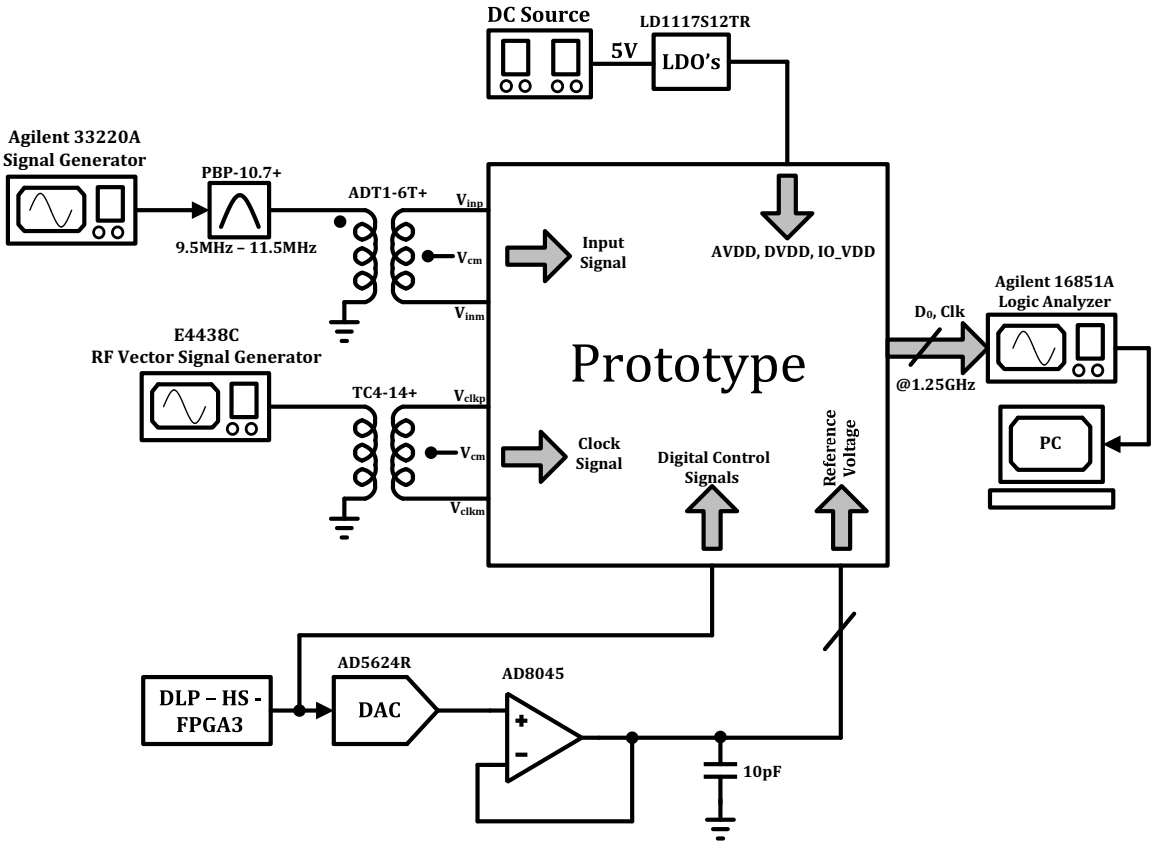

Figure 4.23: Block diagram of test setup.

ceramic capacitor banks. The power and ground pins of the prototype chip are connected to the corresponding planes through enough vias and wide traces, which were made as short as possible to minimize the wire resistance.

All differential high-frequency signal traces are routed symmetrically with proper control of the line width. The distances between the signal traces are kept reasonably wide (20 mils line width) and 10 mils side ground plane to reduce crosstalk (here, 1 mil = $\frac{1}{1000}$ inch). The circuits that generate sensitive analog signals (e.g., the inputs of the modulator and the clock generator), are placed as close as possible to the prototype chip. The high frequency digital signal traces are also as short as possible to reduce electromagnetic interference (EMI). For the modulator input,

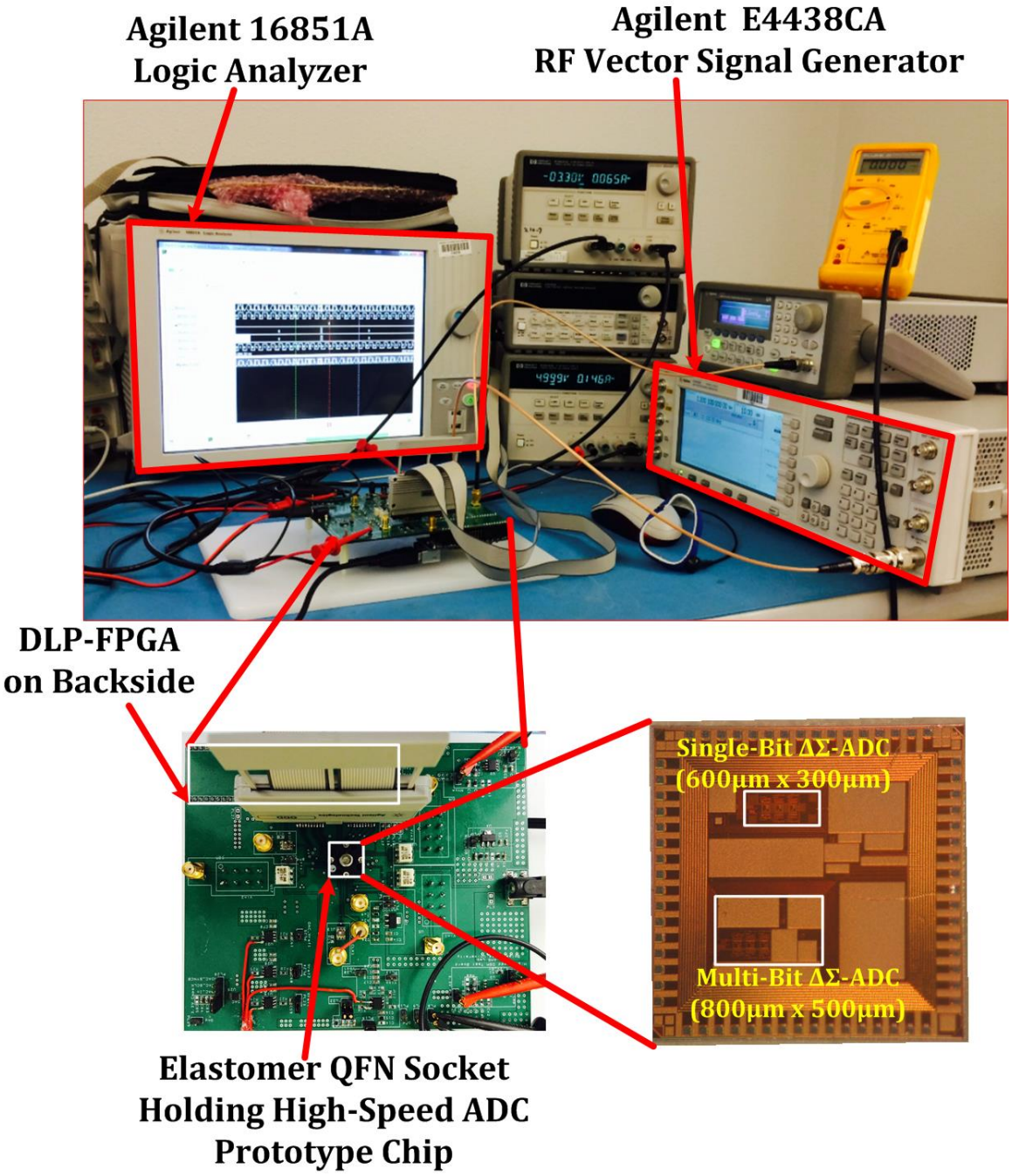

Figure 4.24: Complete test setup for prototype characterization.

the high-frequency single-ended signal from the radio frequency signal generator is used (*Agilent* 33220*A*). In order to characterize the modulator properly, this

signal is filtered by high performance passive bandpass filters ($PBP-107+$) and transformed into the differential signal by the on-board balun ($ADT1-6T+$) before it is fed into the prototype chip. The $1.25\,GHz$ clock signal is obtained from the RF vector analyzer (*Agilent* $E4438C$), and transformed to a differential clock on the board, which is transformed back to a single-ended clock signal on the chip by a diff-pair/input buffer.

The power supply for the regulators is provided by the DC supply equipment. Other power supplies for the device under test (DUT) as well as on-board discrete components uses $1.2\,V$ and $\pm 3.3\,V$, which are generated by low-noise LDOs. Thus, the noise on-board is highly controlled. The modulator outputs are internally buffered and connected to a high-speed logic analyzer (*Agilent* $16851A$) for effective data transfer. The acquired data is transferred to the PC and re-sampled and post-processed using *MATLAB* for spectral performance analysis of the ADC. Figure 4.24 shows the complete test setup for prototype characterization as described above.

4.5 Measurement Results

Using the test setup shown in Figure 4.24, the fabricated high-speed CT-$\Delta\Sigma$M chip assembled on a high-speed elastomer socket is tested with an available high-speed logic analyzer in asynchronous sampling mode (i.e., at the rate of $5\,GS/s$), and processed on a PC. A $32\,K$ samples Blackmann-Harris FFT window was used for spectral estimation for maximum side-lobe suppression. Figure 4.25 shows the spectrum of the output sequence when the converter is excited by a $-2.8\,dBFS$ tone at $10\,MHz$. Figure 4.26 shows the measured SNDR of the modulator. The SNDR was determined using a $10\,MHz$ sinewave input. Due to the unavailability of a high-precision signal

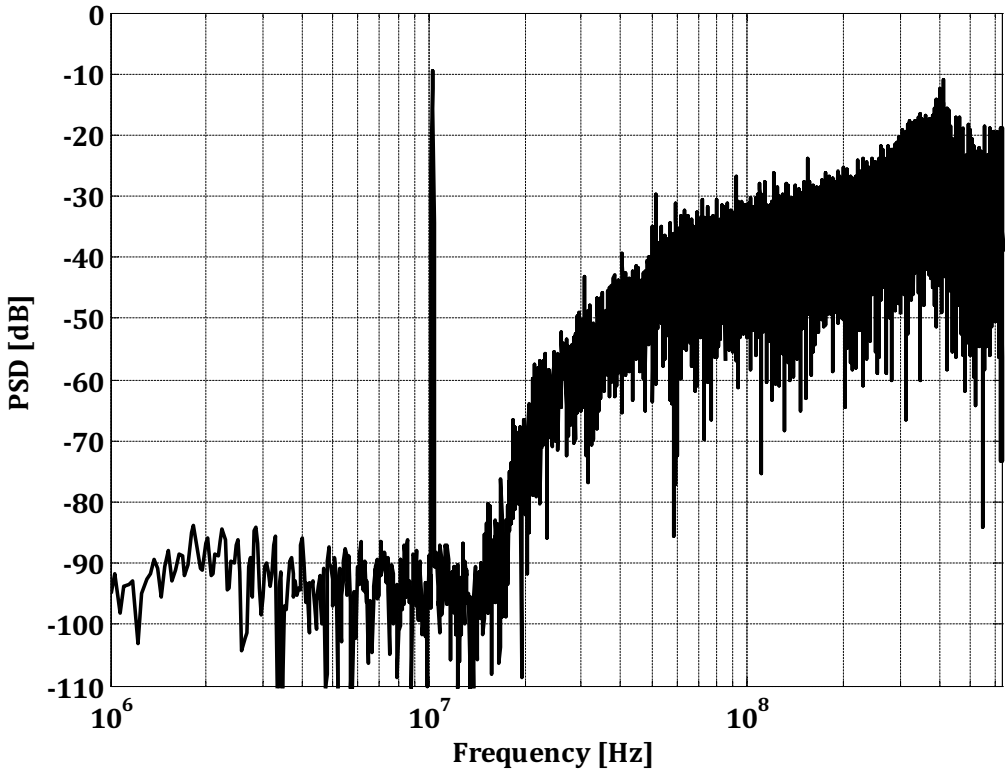

Figure 4.25: PSD for a $-2.8\,dBFS$ tone @$10\,MHz$.

Parameter	Measured Results
Signal Bandwidth/Clock Rate	$15.6\,MHz/1.25\,GHz$
Full Scale	$2.4V_{pp,diff}$
Input Swing for peak SNR	$-2.3\,dBFS$
SNR/Dynamic Range	$54/60\,dB$
Active Area	$0.18\,mm^2$
Process/Supply Voltage	CMOS $0.13\mu m$ IBM
Power Dissipation	$3.5\,mW$
Figure of Merit	$154\,fJ/level$

Table 4.3: Summary of measured ADC performance.

generator, the test board is designed with a bandpass filter with a bandwidth of $9-11\,MHz$. Thus, the design couldn't be evaluated for the third harmonic distortion contribution to the SNDR.

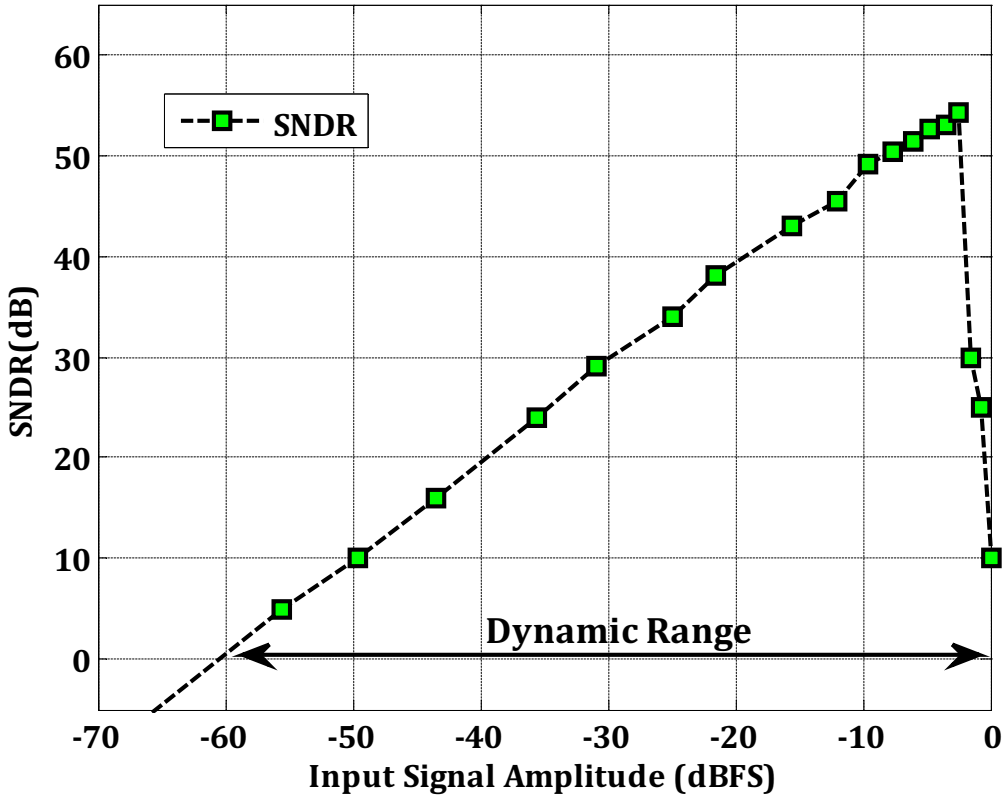

Figure 4.26: Measured SNR - the dynamic range is $60\,dB$.

Reference	Feature Size (nm)	BW (MHz)	SNDR/SNR/DR (dB)	Power (mW)	FOM (fJ/level)
[47]	130	15.6	59.8/64.5/67.0	4	93
[66]	90	10	62.0/-/67.0	6.8	185
This work	130	15.6	54.2/56.1/60.0	3.5	154

Table 4.4: Comparison with other $\Delta\Sigma$ modulators.

A summary of measured performance is given in Table 4.3. From Table 4.3, the designed modulator achieves a dynamic range of $60\,dB$ in $15.6\,MHz$ bandwidth while consuming only $3.5\,mW$ from the $1.2\,V$ power supply. The figure of merit for the designed modulator is $154\,fJ/level$. The FoM of the converter is determined as $FoM = \frac{PD}{2.BW.2^{\frac{(SNR-1.76)}{6.02}}}$, where PD, denotes the power dissipation. Table 4.4

compares the performance of our design with that of state of the art single-bit high speed $\Delta\Sigma$ modulators reported in a 130/180 nm CMOS processes. The resultant performance of the high-speed CT-$\Delta\Sigma$M is $10\,dB$ less than the expected value. The main reason could be the board noise, data corruption due to crosstalk between output signal and reference output clock (i.e., due to QFN package inductance) or asynchronous sampling of CT-$\Delta\Sigma$M high-speed data.

4.6 Summary

An ultra-low power 3^{rd}-order continuous-time $\Delta\Sigma$ modulator sampling at $1.25\,GS/s$ (highest in this technology) was designed, fabricated and tested. The modulator achieves $9.5 - bit$ resolution with $15.6\,MHz$ conversion bandwidth. As a result of a combination of several techniques discussed in Chapter 3 and 4, the designed modulator consumes only $3.5\,mW$ and achieves a figure of merit of $154\,fJ/level$.

CHAPTER 5

DESIGN OF A HIGH-SPEED, LOW POWER MULTI-BIT SINGLE-LOOP CT-△ΣM

This chapter details the complete design of a wide bandwidth CT-△Σ ADC, operating at a 640 MS/s sample rate, implemented in a 130 nm IBM CMOS process. The circuit is targeted for applications that demand high-bandwidth, moderate to high-resolution, and low-power specifications, such as the receivers used in IEEE 802.11 a/b/g/n Wireless LANs. The comprehensive system and circuit-level design of the wide bandwidth CT-△Σ ADC is detailed with complete analysis of non-idealities effect, especially the quantizer, on overall modulator performance. Further, the complete circuit design of each block used in the high-speed modulator is presented with simulation and test results.

5.1 Introduction

A detailed discussion on the advantages of a multi-bit modulator over a single-bit design was detailed in Chapter 3. In summary, the important benefits of a multi-bit modulator over a single-bit design are:

- **Lower In-Band Quantization Noise:** A multi-bit quantizer inherently contributes lower quantization noise due to a smaller LSB size. Thus, for the same NTF, the in-band quantization noise would decrease by 6 dB for every

additional quantizer bit. More importantly, a multi-bit quantizer allows an aggressive NTF, resulting in a significant reduction in the in-band quantization noise.

- **Lower Noise Due to Clock Jitter:** As the clock jitter affects the sampling instant of the quantizer, which results in a jittery feedback DAC pulse (assuming NRZ ADCs, as RZ ADCs have worse jitter performance). This jittery feedback is nothing but the modulation of the width of the DAC feedback pulse, which is the dominant source of jitter-induced noise and is given by the equation below from Section 3.5.4.

$$S_j = \left(\frac{\sigma_{\triangle t}^2}{T_s^2} \; \frac{\sigma_{LSB}^2}{\pi OSR} \int_0^{\pi} \left| \left(1 - e^{-j\omega}\right) NTF\left(e^{j\omega}\right) \right|^2 d\omega \right) \tag{5.1}$$

From the above equation, it is clear that as the σ_{LSB}^2 decreases when using a multi-bit quantizer, the sensitivity to clock jitter is greatly reduced when compared with a single-bit design.

- **Lower Slew-Rate Requirements from the Loop-Filter Opamp:** The input to the loop filter contains noise-shaped quantization noise, whose amplitude excursions are much smaller in a multi-bit design when compared to a single-bit design. Thus, the loop-filter opamps do not need to accommodate large current jumps injected at their virtual ground, which translates into a lower power dissipation for the entire modulator.

5.2 System-Level Design

In this section, the architectural choices made in the design of a high-speed multi-bit CT-$\Delta\Sigma$ modulator are described. These include the design of the NTF for given specifications, the impulse invariant transformation to arrive at the CT loop-filter architecture, the dynamic range scaling of loop-filter states, the determination of circuit design parameters while considering the contribution of various noise sources to the overall in-band noise of the modulator, the excess loop-delay, and the overall power optimization; and estimation/optimization of SNDR (and dynamic range) performance in the presence of circuit non-idealities using behavioral simulation prior to transistor-level implementation.

5.2.1 Design of Noise-Transfer Function

Selection of the proper NTF along with other system-level design parameters, which include f_s, OSR, order, OBG, and quantizer resolution, determine the performance of a multi-bit modulator. From the discussion in the previous chapter, it was demonstrated that a sampling frequency of $1.25\,GHz$ is possible in a $0.13\,\mu m$ CMOS technology. However, the sampling rate needed to achieve desired performance is highly relaxed due to the use of a multi-bit quantizer. Nevertheless, the power consumption of the quantizer increases proportionally to the number of quantization levels. From section 3.4, it is understood that the circuit complexity increases exponentially when the resolution of the flash ADC is higher than 4-bit. Thus, we settled for a four-bit quantizer as a compromise between the contrasting benefits offered by multi-bit quantization and the increased complexity of circuit-level implementation.

To achieve a SNR of above $72\,dB$ in a signal bandwidth of $20\,MHz$, a third-order

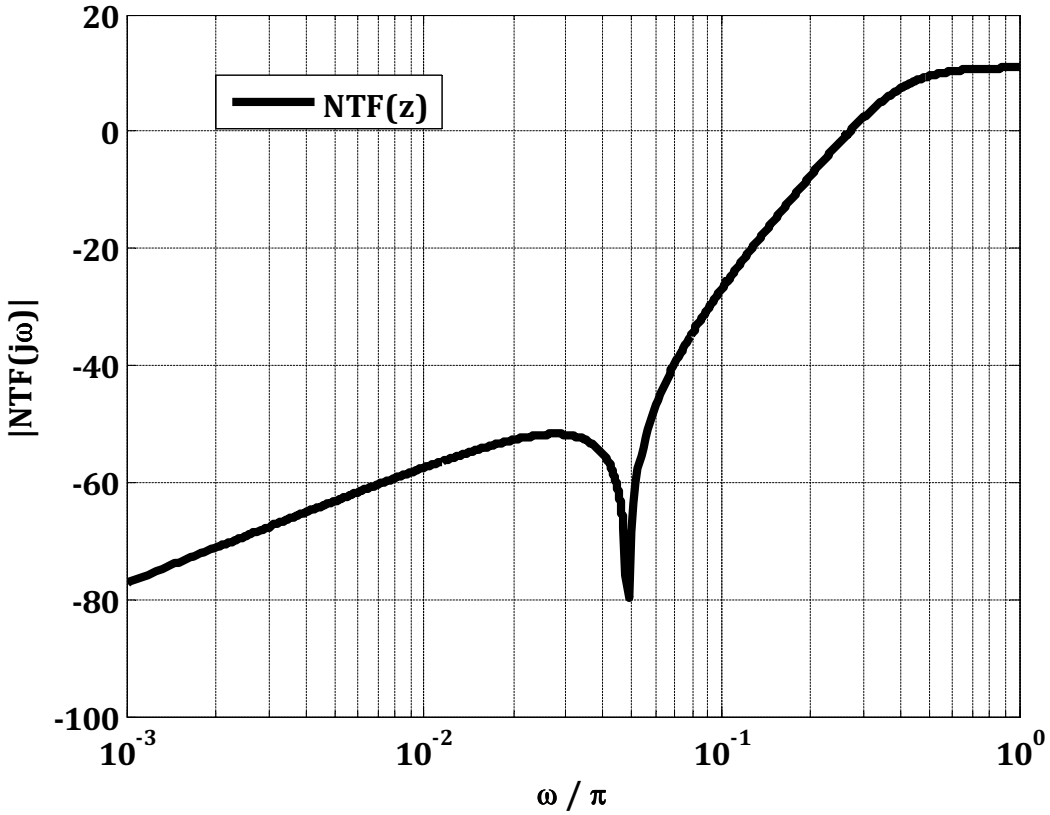

Figure 5.1: Magnitude response of the noise-transfer function, $|NTF(z)|$.

$NTF\,(z)$ with a low oversampling ratio of $OSR = 16$ is chosen. Further, for better stability of the 3^{rd}-order multi-bit single-loop modulator, the out-of-band gain is limited to $12\,dB$ or $OBG = 3.5$, with complex zeros spread out in the signal band to improve the noise shaping performance [19]. Figure 5.1 shows the magnitude response of the noise-transfer function. $NTF\,(z)$ is evaluated as in Equation 5.2 and it can achieve a peak in-band SQNR of $86\,dB$, which is about $14\,dB$ above the desired SNR of the converter.

$$NTF_{eff}\,(z) = \frac{(z-1)\,(z^2 - 1.997z + 1)}{(z - 0.3108)\,(z^2 - 0.4878z + 0.2459)} \tag{5.2}$$

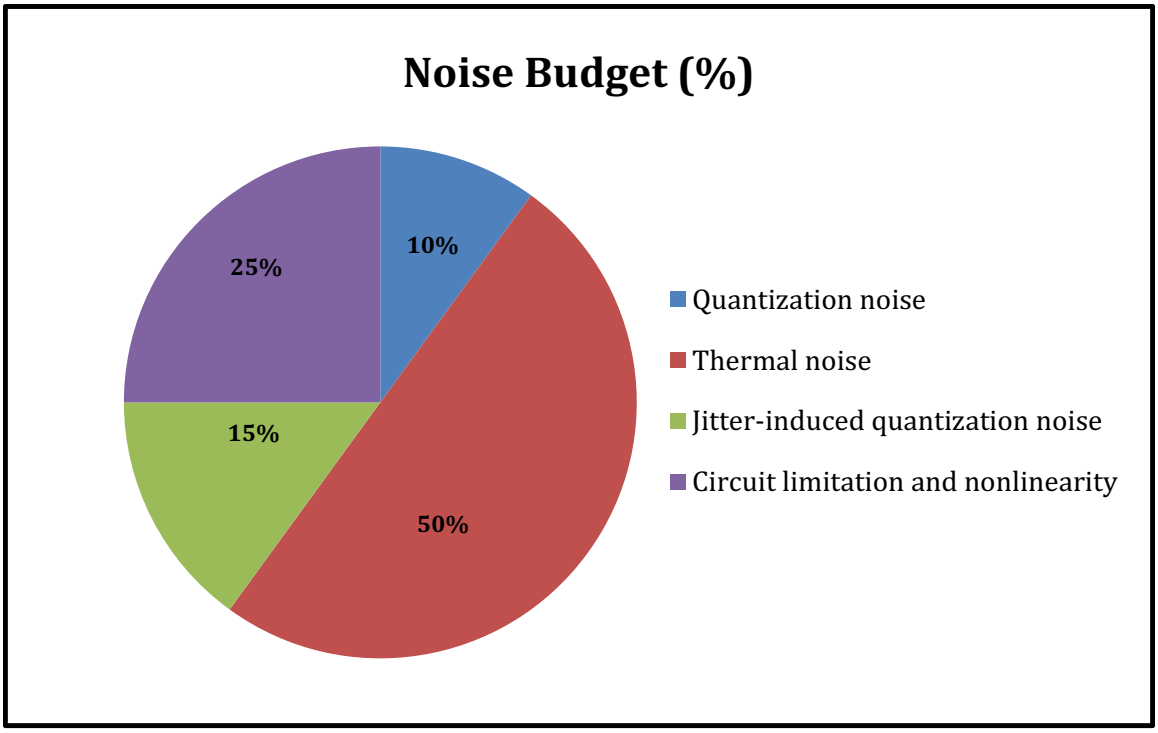

Figure 5.2: Noise Budget of the multi-bit CT-$\Delta\Sigma$ modulator.

5.2.2 Modulator Architecture, Noise Budget

The modulator architecture adopted in this design is derived from the architecture used in the previous chapter, to attain robust anti-alias filtering characteristics and to eliminate the high-speed and power-hungry summing opamp. Also, to obtain reduced sensitivity of the modulator due to clock jitter, a $4-bit$ Flash ADC with an NRZ current-steering feedback DAC is employed. The detailed design of each of these blocks will be explained later in this chapter.

Similar to Section 4.2.3, Figure 5.2 shows the pie chart of the multi-bit $\Delta\Sigma$M noise budgeting in order to achieve the required ENOB performance. Further, Table 5.1 shows the corresponding maximum achievable SNR limited by noise source to $-3dBFS$ input. As far as thermal noise is concerned, a noise budget of 50% of total

Noise/Distortion Source	Noise Budget (%)	SNR (dB)
Quantization noise	10%	86
Thermal noise	50%	79
Jitter-induced quantization noise	15%	84
Circuit limitation and non linearity	35%	81

Table 5.1: Multi-bit CT-$\Delta\Sigma$ modulator noise budget.

in-band noise is a reasonable estimate, which is 20% more than the single-bit $\Delta\Sigma$M design. This results from the fact that the thermal noise contribution from the $4-$bit current steering feedback DAC is more than the noise from a single feedback resistor in a single-bit $\Delta\Sigma$M. The detailed noise analysis considering the effect of feedback DAC noise on the total thermal noise in the signal band will be addressed later in this chapter. Overall, to achieve an ENOB of 12-bits, the in-band thermal noise power should be less than $-82\,dBFS$.

Following similar arguments, a budget of 15% of total noise is allocated for the jitter-induced noise, captured by the signal-to-jitter noise ratio. To obtain the target SNR of $72\,dB$, an SJNR greater than $83\,dB$ is required. The allocation for SJNR for the multi-bit $\Delta\Sigma$M is 15% less than the single-bit design. The reason being that the multi-bit quantizer and a moderate OBG value help reduce in-band noise contributed by the DAC reconstruction jitter. Figure 5.3 shows SJNR vs σ_{jitter}, normalized to T_s in percentage (%) using *a Matlab Simulink* behavioral simulation. From the plot, it can be observed that the jitter-induced noise power is $-89\,dBFS$ for 0.1% jitter. This dictates that the rms jitter tolerance of the clock source should be less than $1.6\,ps$. This jitter requirement on the clock can achieved by careful printed circuit board design and using on-board filtering for the clock signal. Finally, a thermal noise budget of 25% is allocated to the in-band noise contribution arising due to the circuit non-idealities in the multi-bit design. In spite of all the advantages of multi-bit $\Delta\Sigma$M

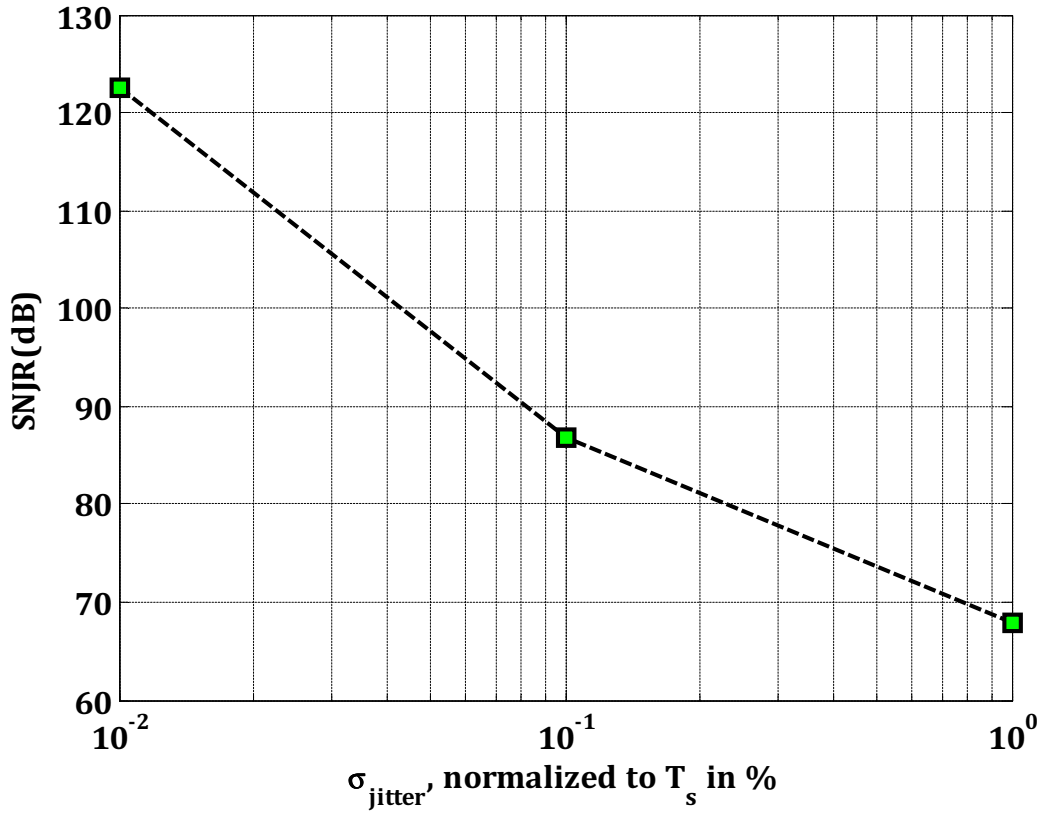

Figure 5.3: SJNR of a 3rd-order CT-$\Delta\Sigma$ modulator Vs σ_{jitter}, normalized to T_s in %.

over its single-bit counterpart, as summarized in section 5.1, the circuit complexity of multi-bit $\Delta\Sigma$M is significantly increased due to the circuit-level limitations involved in a high-speed multi-bit quantizer and the feedback DAC.

The dominant non-idealities in a Flash converter, which degrades the SNDR performance of the overall modulator, is the deviation in quantizer thresholds from their ideal values due to device mismatch in the comparators. It is generally assumed that any non-idealities introduced by the flash ADC are noise shaped by the loop. However, it necessary to understand the maximum tolerable mean square error allowed by the comparator offset for overall design optimization. Thus, the offset in the comparator

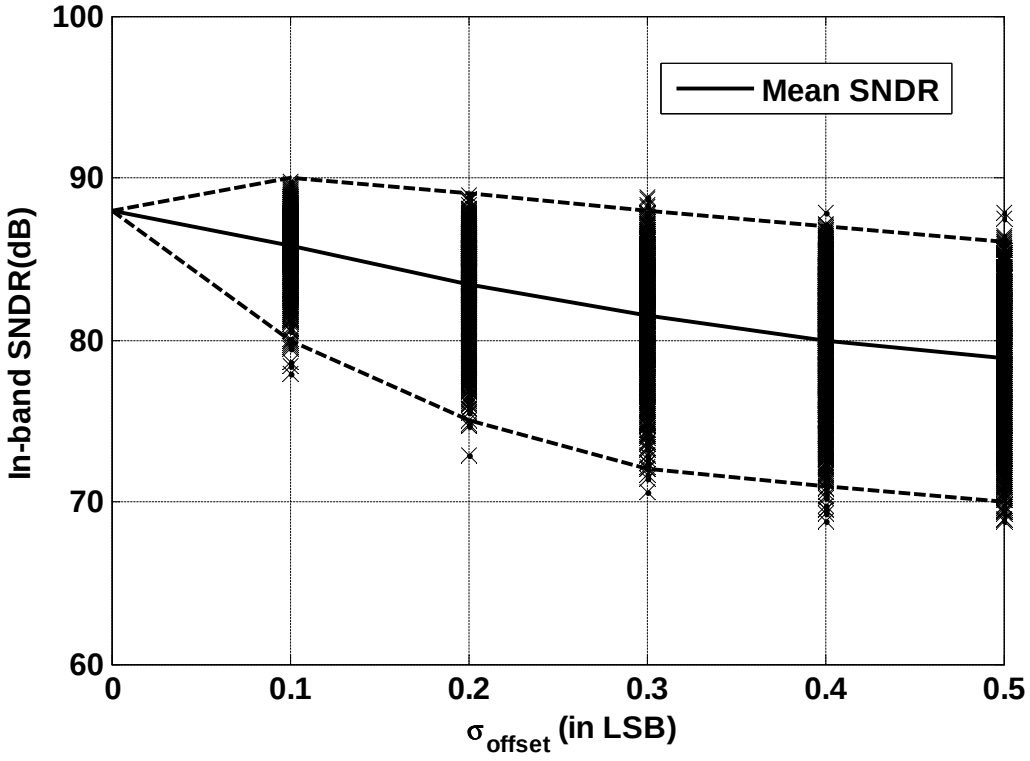

Figure 5.4: Effect of comparator random offset on in-band SNDR—for each level of offset, 1,000 trials were simulated. The lines show the modulators with the best 1% SNDR, mean SNDR and the worst 1% SNDR, respectively.

is modeled in *Simulink,* and simulated the modulator for SNDR performance. Figure 5.4 shows the effect of comparator random offset on in-band SNDR for each level of offset. For each offset level, 1000 trials are simulated. Here, it can be observed that to achieve a 12-bit SNDR performance from the modulator, random offsets in the comparator with a standard deviation of up to $0.1 - 0.2\,LSB$ can easily be tolerated. However, this is only true as long as the input-output characteristics of the quantizer are monotonic. Any non-monotonicity in the quantizer can result in the overall feedback loop getting confused and it can vacillate about a local minima in the loop-transfer characteristics [32].

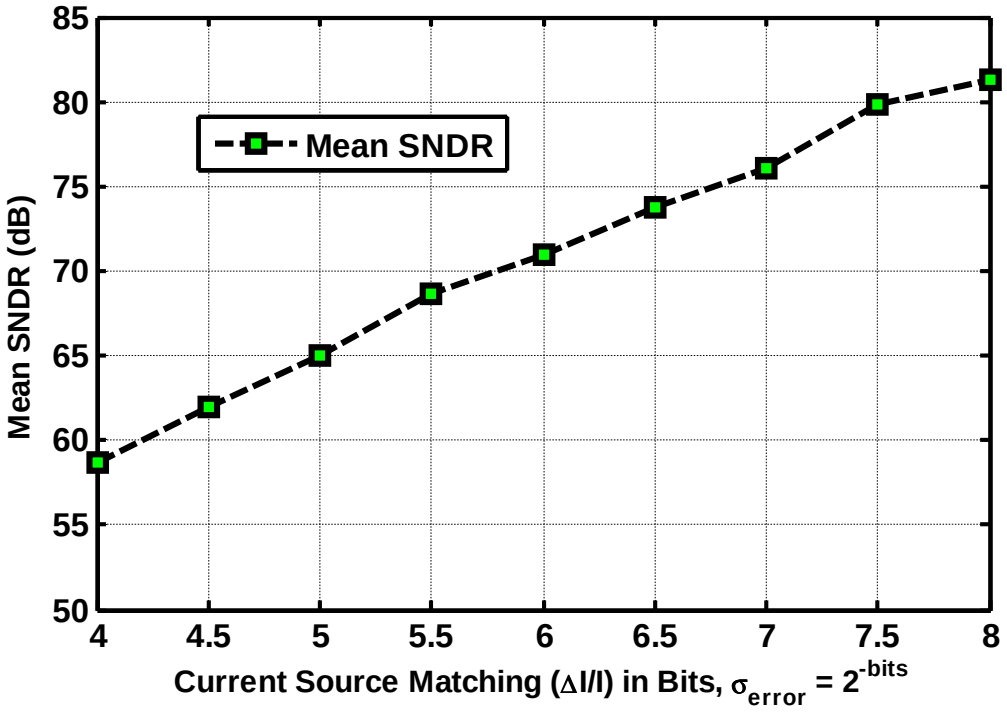

Figure 5.5: Behavioral-level simulation of modulator SNDR versus fast-loop DAC unit element mismatch−for each level of bits, 1,000 trials were simulated.

Another important non-ideality resulting from the multi-bit quantizer is the feedback DAC non-linearity. This is because any errors due to non-linearity introduced by the feedback DAC are directly added at the same point as the input signal. As a result, the error appears directly at the output, dictated by the inverse function of the DAC transfer characteristics, without undergoing any noise-shaping by the feedback loop. Consequently, the overall linearity of a $\Delta\Sigma$ ADC cannot exceed the linearity of the DAC used in its feedback path. This is a critical concern when designing multi-bit $\Delta\Sigma$ ADCs. In Figure 4.2, the illustrated modulator employs three DACs for realizing distributed feedback. DAC_0 is the main feedback DAC, and k_3 and k_a implement the fast feedback loop required for excess loop-delay compensation.

The feedback DAC in the fast-loop can tolerate a considerable extent of unit-

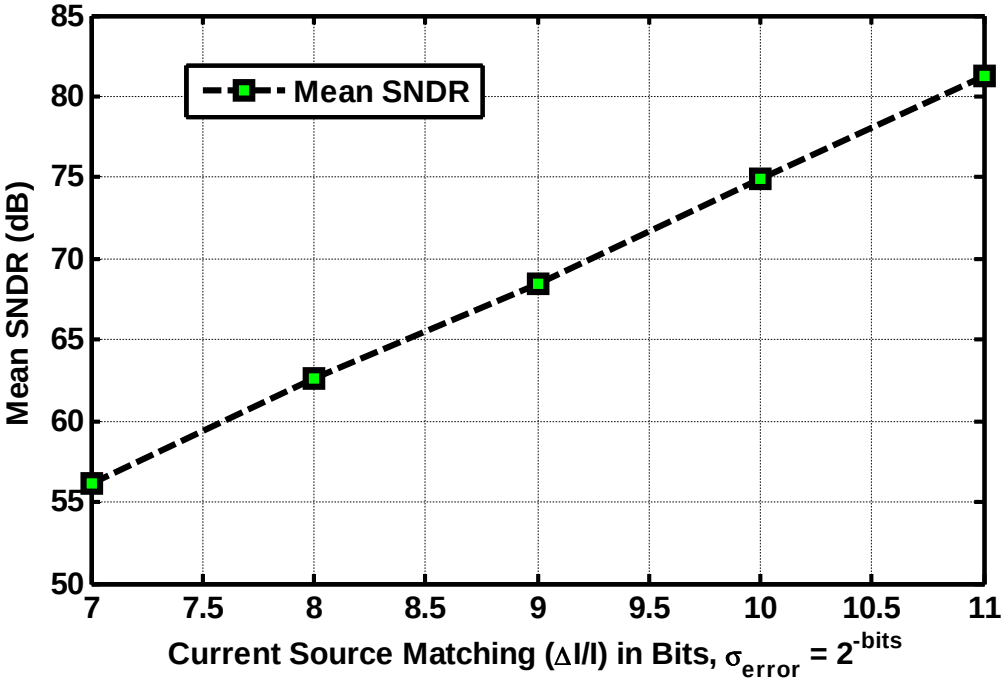

Figure 5.6: Behavioral-level simulation of modulator SNDR versus slow-loop DAC unit element mismatch−for each level of bits, 1,000 trials were simulated.

current mismatch errors when compared to the main feedback DAC, since any error introduced is injected into the loop at the same place as the quantization noise. Thus, it is noise-shaped by the the $\triangle\Sigma$ loop with some limitations. Figure 5.5 shows the behavioral-level simulation results for the modulator, where mean-SNDR is plotted against the mismatch in the fast-loop DAC unit-elements. From this result, it can be deduced that at least 8-bit DAC linearity is mandatory to avoid any performance degradation from the targeted SNDR. Similarly, Figure 5.6 shows the behavioral-level simulation of the modulator SNDR versus the DAC unit-element mismatch in the main feedback path. Here, it clearly shows that the linearity of the main feedback DAC has to be at least equal to or greater than the targeted SNDR of the overall modulator. Consequently, the design of the main feedback DAC, DAC_1, is of critical

importance to the overall $\Delta\Sigma$ ADC design.

5.3 Circuit-Level Design

This section provides a detailed description of the circuit-level blocks employed in the wideband multi-bit CT-$\Delta\Sigma$ modulator.

5.3.1 Loop Filter

Figure 5.7 shows an active-RC implementation of the CT-$\Delta\Sigma$M architecture from Figure 4.2. In order to optimize power consumption in the design, the last integrator is also used as a summer, along with analog differentiation of the k_0 feedback path using an NRZ DAC, similar to [17, 67]. The resonator feedback g_1 is implemented using the R_{z1} resistors. The integrating capacitor is implemented as a programmable bank using four control bits to tune the design to compensate for the RC time-constant variation with process. The output of the last integrator needs to drive the large input capacitance of the Flash ADC and is designed for high-speed, large swing, and strong drive capacity, which is further explained in Section 5.3.2. Deleterious effects due to the excess loop delay and finite opamp bandwidth are compensated by using a direct path (or fast path) around the quantizer using $DAC_0$and DAC_3. The main feedback path coefficient is realized using DAC_1.

5.3.2 Operational Amplifier

From the top-level schematic, shown in Figure 5.7, three opamps are employed in the loop filter. These opamps are implemented using a feedforward frequency compensated topology, similar to Figure 4.11. As the sampling frequency is halved

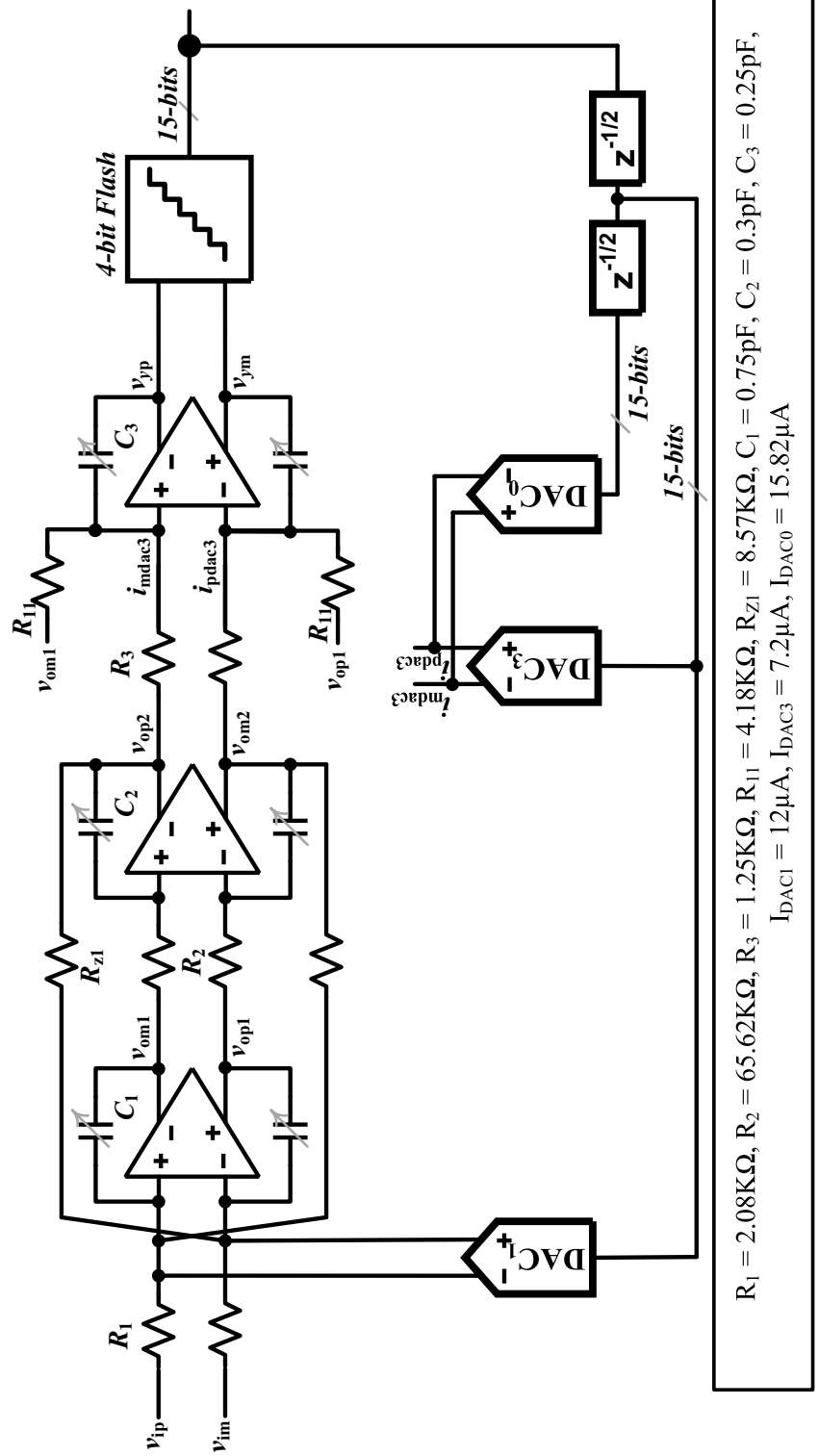

Figure 5.7: Top-level circuit diagram of the multi-bit CT-$\Delta\Sigma$ modulator.

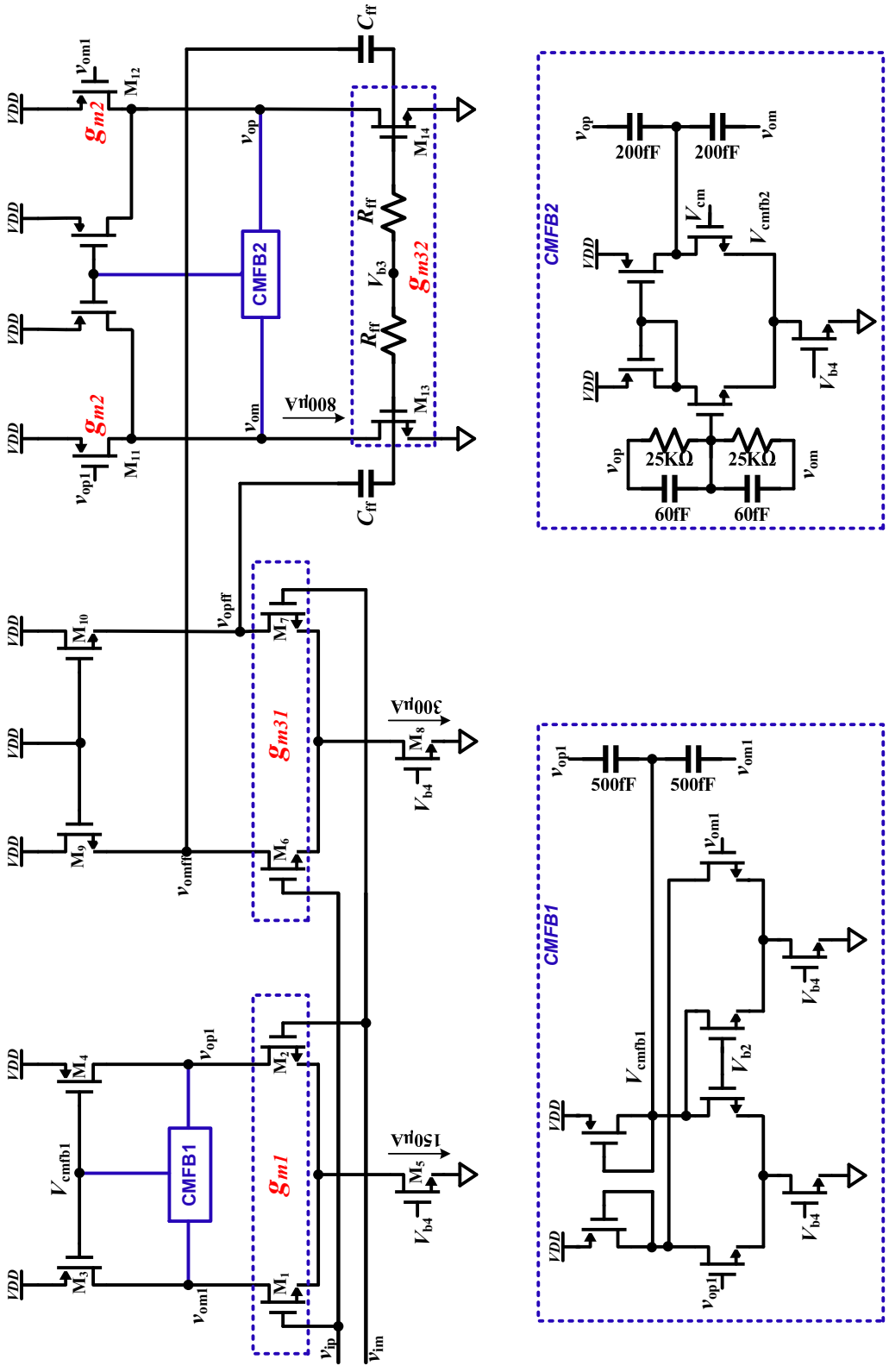

Figure 5.8: Two-stage feed-forward compensated opamp with CMFB circuit used in last integrators.

Table 5.2: Simulation summary of the 3^{rd}-integrator RC-extracted opamp using Flash ADC as load.

Corners	A_{dc}(dB)	f_{Unity}	PM_{DM}	UGB_{CMFB1}	PM_{CMFB1}	UGB_{CMFB2}	PM_{CMFB2}
Typical	42	$1.95\,GHz$	58.98°	$43\,MHz$	65°	$78\,MHz$	56°
SF (worst case)	41	$1.339\,GHz$	62.6°	$41\,MHz$	68°	$36.5\,MHz$	61°

from the single-bit design, seen in the last chapter, and the LSB size is four-times smaller, the opamp power dissipation is optimized and consequently reduced. The same topology is used for the first two opamps with appropriate power scaling in the second stage. Thus, the total current drawn by the 1^{st} and 2^{nd} opamp, including the bias circuit, is $1.5\,mA$ and $900\,\mu A$ respectively.

The opamps in the first two integrators of the loop filter do not require large output swings due to the scaled integrator states, after appropriate dynamic range scaling. However, the opamps in the last integrator of the loop filter is required to drive the flash ADC with a $2\,V_{pp,d}$ output swing. From Figure 4.11, it is clearly seen that the opamp output swing is highly limited by the input transistors (M_{19} and M_{20}) of the feed-forward stage. Thus, to meet the large output swing requirement set by the input range of the Flash ADC, an alternative opamp topology is needed.

Figure 5.8 shows the opamp used in the last integrator. This topology is similar to Figure 4.11, except that the first gain-stage is not cascoded, thanks to the relaxed opamp open-loop DC gain requirements. Moreover, the feed-forward stage is in turn modified to include two gain stages. The first-stage of the feed-forward path is realized using $M_{6\,\&\,7}$, which forms a low-gain and high-speed stage due to the NMOS active load (i.e., $M_{9\,\&\,10}$). While the second-stage of the feed-forward branch are essentially common-source amplifiers, realized by $M_{13\,\&\,14}$, which re-use the current from the second stage of the opamp. The second stage supports a high output swing, while first stage provides the moderate gain with higher linearity. Further, to decouple the

DC biasing from the first-stage of the feed-forward path, an AC coupling capacitor ($C_{ff} = 800\,fF$) is employed. In this scheme, to set the DC bias level of $M_{13\,\&\,14}$, a resistor $R_{ff} = 10\,K\Omega$ resistor is used. Table 5.2 summarizes the simulation results for the last integrator opamp in typical and worst (SF) corner models. Across the corners, the opamp f_{unity} is simulated to make sure that the f_{unity} is at least equal to $2f_s$. The total power consumption of the third opamp, including the bias circuits, is $2\,mW$.

5.3.3 Design of $4-$bit Flash ADC

A simplified block diagram of the 4-bit Flash sub-ADC used in the CT-$\triangle\Sigma$ modulator is shown in Figure 5.9. The sub-ADC consists of a differential comparator array, a resistor ladder, and a digital back-end, which includes a thermometer-to-binary encoder. The comparator array is comprised of 15 differential comparators, which compare the input signal with the reference voltages generated by the resistor ladder to produce a $15-$bit equivalent thermometer-coded quantized representation of the input signal. To potentially correct and suppress the bubble errors introduced in the Flash ADC and to generate an equivalent binary output, a Wallace-Tree encoder is used. The high-speed encoder is implemented using 11 full-adders (FAs) [68]. Further, the encoder is placed outside the modulator loop and is used to interface with the pads. Their design considerations will be detailed in Section 5.3.5.

The reference ladder is placed between the differential DC references $V_{bot} = 0.2\,V$ and $V_{top} = 1\,V$, as shown in Figure 5.9. The reference ladder generates differential references spanning the input range of $[-0.8\,V, +0.8\,V]$, around the common-mode voltage ($V_{CM} = 0.9V$) for the Flash ADC. Thus, the full-scale input range of the converter is $[-0.8\,V, +0.8\,V]$ differentially, resulting in a nominal quantizer-step or

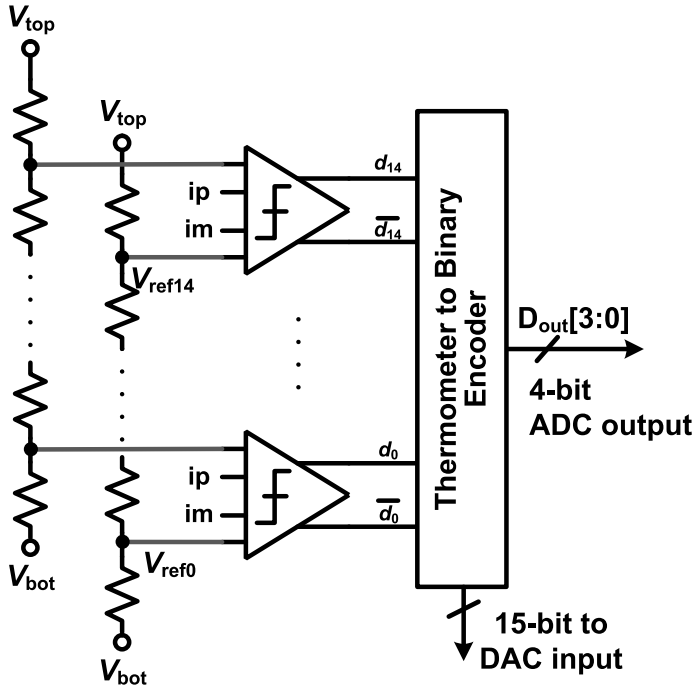

Figure 5.9: The 4-bit quantizer used in the CT-$\triangle\Sigma$ modulator.

LSB size of $100\,mV$. The relatively large LSB size relaxes the offset compensation requirements for the comparators to some extent. To further mitigate the effect of comparator offsets, a resistor averaging technique is implemented at the output of the preamplifier [5, 69]. The reference voltages (V_{bot} and V_{top}) for the ladder are generated off-chip using a discrete component $AD8138$ [70]. Also, additional on/off-chip capacitors are used to bypass the V_{bot} and V_{top} nodes of the reference ladder to hold the reference voltages constant in the presence of any kickback disturbance generated by the fast switching transients in the modulator.

5.3.3.1 Comparator Design

The simplified block diagram of the comparator and the corresponding clock phase waveforms are shown in Figure 5.10(a). The comparator consists of a preamplifier,

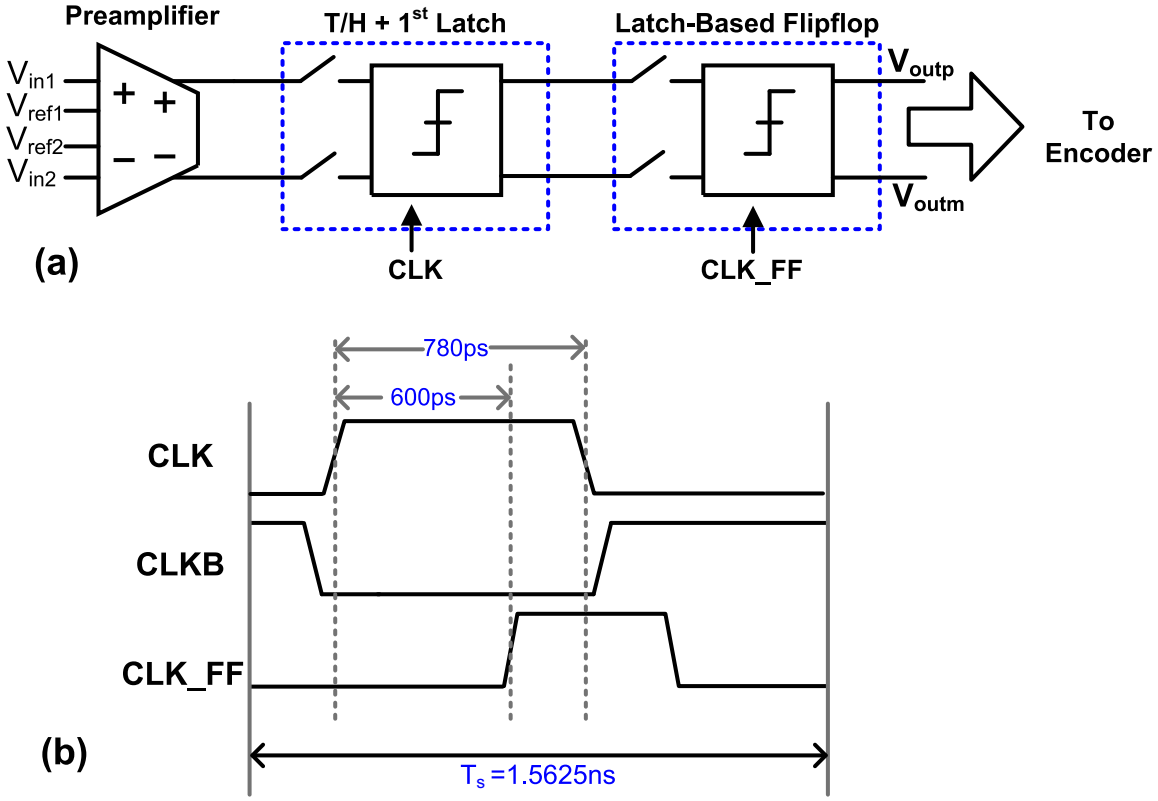

Figure 5.10: (a) Block diagram of the comparator and (b) timing diagram for the comparator operation.

a regenerative latch that also works as a sampling stage (or distributed track and hold), and a latch-based flip-flop. The timing of the Flash ADC is shown in Figure 5.10(b). The preamplifier is not clocked, therefore the first latch receives the amplified continuous-time signal from last integrator (which also includes the summer).

In the first latch, when clock CLK is low, the circuit is in track mode. When the CLK goes high, the circuit goes to a simultaneous sampling and regeneration mode where the signal is sampled, compared, and amplified due to the high-gain of the positive feedback of the latch stage. Then, the regenerated signal is delivered to the next latch-based flip-flop stage. A latch-based flip-flop not only stores the resolved logic level, it also provides extra regeneration gain for the low-difference input signals

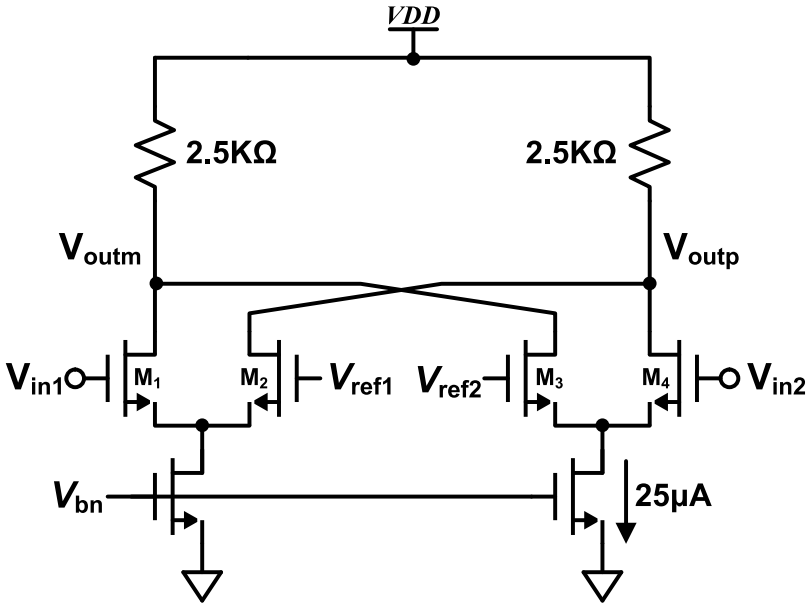

Figure 5.11: Schematic of preamplifier used in comparator.

from the $1^{st}-$latch stage. Two cascaded latches at the output, in addition to the large preamplifier gain-bandwidth product, preclude any possibility of comparator metastability. The device sizes in the difference stages of the comparator are chosen to achieve high-component matching in the preamplifier as well as in the latching stage. The latch and flip-flop architecture used in this comparator are same as the topology used in the single-bit CT-$\triangle\Sigma$M seen in Chapter 4. The only modification is that this comparator design is further optimized for power dissipation, thanks to the reduced sampling clock rate.

The preamplifier used at the input of the comparator is shown in Figure 5.11. It is a *differential difference amplifier* (DDA) with resistive loads. The gain and the output voltage of the preamplifier can be expressed as

$$(V_{outp} - V_{outm}) = g_m R_D \left((V_{in1} - V_{in2}) - (V_{ref1} - V_{ref2})\right) \tag{5.3}$$

where V_{in1} and V_{in2} are the differential inputs, and V_{ref1} and V_{ref2} are the differential reference voltages generated by the resistor ladder. Further, the preamplifier input devices (M_{1-4}) are sized for $\sigma_{offset} = 0.1\,LSB$ random offset. To verify the random offset in the circuit, the standalone transistor-level comparator is simulated using the Monte-Carlo method using the foundry statistical models for the devices. The result from the Monte-Carlo simulation is shown in Figure 5.12. Though, the comparator meets the offset requirement set by the system-level design, it calls for large device sizes, which further result in large parasitic capacitance at the drain node of the input transistors. This, in turn, results in reduced bandwidth of the preamplifier stage. Thus, to simultaneously achieve moderate gain with higher bandwidth over different process corners, the resistive load of $2.23\,K\Omega$ is chosen over an active load (i.e., realized using transistors).

5.3.3.2 Resistor Ladder

The $4-$bit resistor ladder consists of 16 equal unit resistors. As long as the resistors are well-matched, independent of their absolute values, the resistor ladder produces evenly-spaced voltage references. However, any random mismatch between the resistors of the resistor ladder will result in voltage offsets in the reference voltages. These voltage offsets would also contribute to the total offset of the Flash ADC. However, resistor matching in modern CMOS processes is typically on the order of 10-bit accuracy [5, 71]. As resistor matching exceeds the resolution of the Flash ADC, resistor matching is typically not a concern in our designs. Still, special layout techniques, such as common centroid and respect symmetries, are used to keep the effect of such mismatches as small as possible.

There is a fundamental trade-off between the power consumption of the resistor

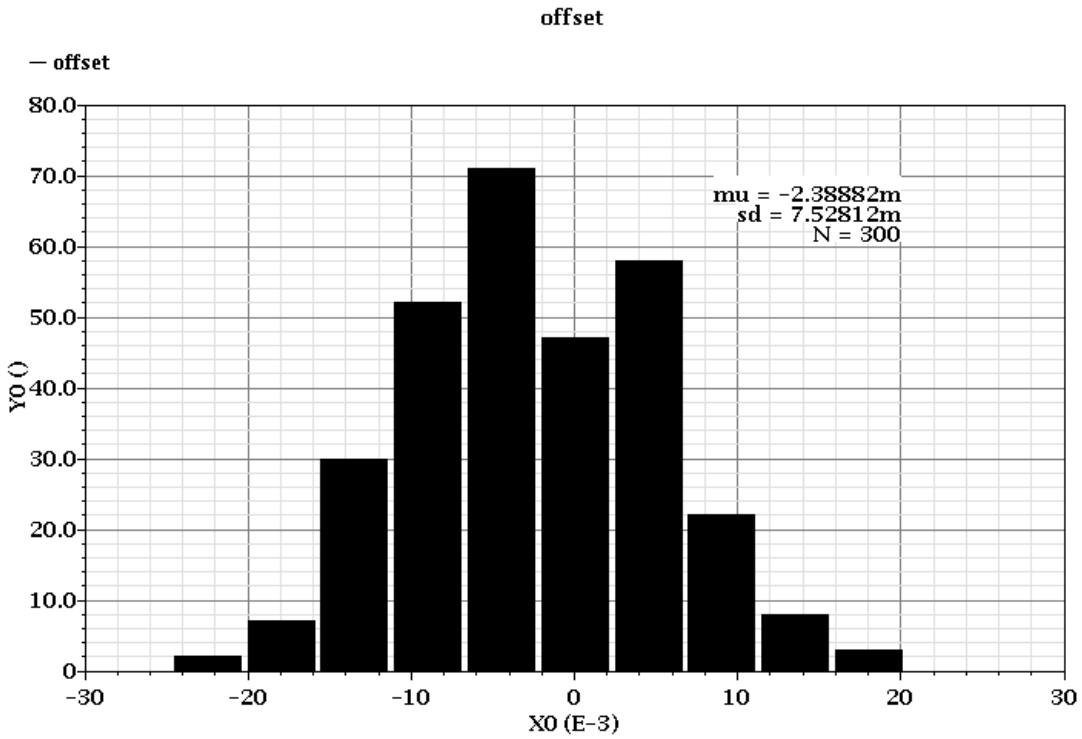

Figure 5.12: Monte-Carlo simulation of comparator input referred offset.

ladder and the susceptibility of noise injection in choosing the proper unit value of the resistor. A smaller resistor value results in higher power consumption, while they reduces noise injection at the reference voltages. Also, the input signal feed-through or kick-back noise due to the gate-drain coupling capacitor of the preamplifier also disturbs the reference voltages in the ladder. Therefore, the settling or transient behavior of these nodes are based on effective resistance at that node. In general, the worst case settling or transient would be at the middle reference voltage since that node has the highest resistance. After considering all of the above discussion, a unit resistor value of $100\,\Omega$ is chosen for the resistor ladder of the $4-$bit Flash ADC.

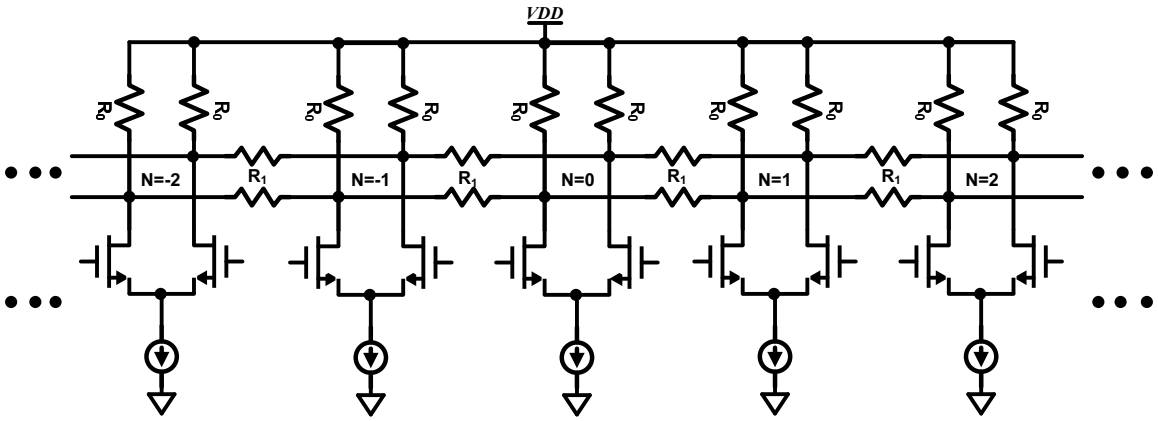

Figure 5.13: Preamplifier array with resistor averaging network.

5.3.3.3 Resistor Averaging in the Preamplifier

In general, to remove or mitigate the comparator offset, one of three methods are often used; input offset storage [5], offset averaging [5, 69], and digital calibration [21]. Since, the $\triangle\Sigma$M itself can tolerate some extent of offset in the Flash ADC ($\sigma_{offset} = 0.3\,LSB$), it relaxes the need for an efficient and power hungry offset canceling method such as input offset storage and digital calibration. Thus, an inexpensive resistor averaging technique is implemented in the 4-bit Flash ADC.

In this method, as shown in Figure 5.13 [69, 72], a resistor network is used to connect the outputs of the adjacent preamplifier in the preamplifier array (for schematic simplicity, the differential difference amplifier is shown as a simple differential amplifier). When the devices are matched, the resistor network has no impact on the circuit operation. When there is a random mismatch, where it causes a non-linearity error, the resistor network uses the average of many preamplifier outputs and produces a restoring force that pushes the errors toward zero and reduces differential non-linearity (DNL) [5, 69].

Error correction factor (ECF) is defined as the percentage improvement in the

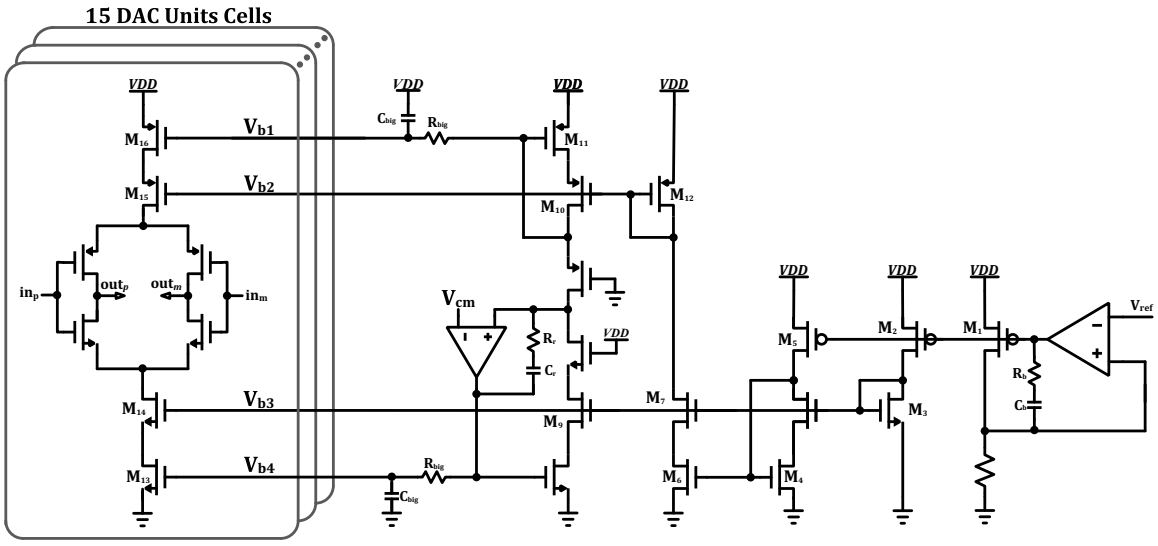

Figure 5.14: Simplified schematic of DAC bias with DAC unit cell.

DNL performance for a given $\frac{R_1}{R_0}$ ratio [69, 72], where R_1 is the resistance of the averaging network and R_0 is the output resistance of the preamplifier array.

$$ECF = \left[1 - R_x \frac{1 - \frac{R_0}{R_0 + R_x}}{2\left(R_0 + \frac{R_x}{2}\right)}\right] \times 100, \quad R_x = \frac{R_1 + \sqrt{R_1^2 + 4R_0R_1}}{2} \tag{5.4}$$

Also, it can be shown that for values of $\frac{R_1}{R_0}$ smaller than two, the DNL becomes negligible and the INL remains as the main error [69, 72]. Thus, the value of R_0 is chosen as $3.8K\Omega$.

5.3.4 DAC Design

From the modulator architecture shown in Figure 5.7, three NRZ ADCs are employed; 2 fast loop and 1 slow loop DAC (main feedback path). There are two possibilities for the NRZ feedback DAC implementation (i.e., resistive or current steering DAC). A resistive DAC is attractive for its low noise property, but in high-speed design such

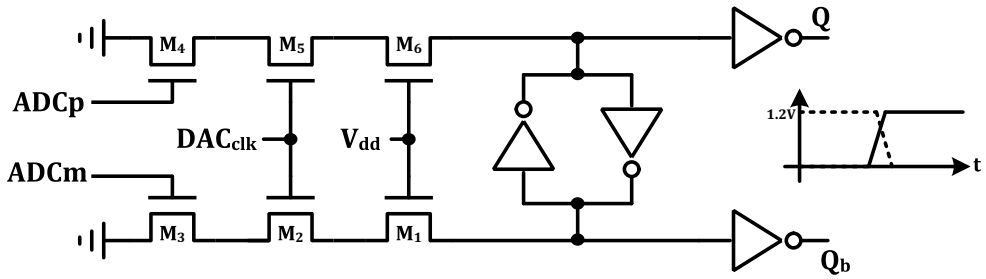

Figure 5.15: Schematic of DAC driver cell.

ADCs have several problems that make their implementation difficult. While, the current mode DAC supports high-speed and simplifies its interfacing to the first integrator, where the amplifier summing nodes provide a low-swing and low-impedance sink for the DAC current outputs. Thus, a NRZ complementary current mode DAC is employed in the modulator feedback path [39].

Figure 5.14 shows the simplified DAC bias along with a complementary current steering DAC unit-cell. Using the internal reference voltage, V_{ref}, the main DAC reference current is generated using a $V_{dd} - R$ bias structure. To avoid mismatch between the up and down current of the DAC cell, replica bias is used and the loop is compensated using R_r and C_r. The main up/down current source transistor M_{16} and M_{13} uses long devices and has large overdrives to reduce thermal and $\frac{1}{f}$ noise. Also, the generated bias voltages from reference generator are low-pass filtered using $R_{big} = 5\,K\Omega$ and $C_{big} = 25\,pF$ to filter all the reference voltages.

Also, the following concerns are carefully taken into consideration to achieve better dynamic performance from the unit DAC cell: (i) imperfect synchronization of the control signals at the switches, (ii) source-coupled node variation of the current-source transistors (i.e., M_{14} and M_{15}), and (iii) coupling of the control signals through the switches to the output. A high crossover DAC driver as shown in Figure 5.15 is

employed to reduce the glitching energy and to optimize the dynamic performance of the DAC [6].

Using DAC behavioral simulations results from Section 5.2.2, the required matching of the fast and slow unit current sources is known. To guarantee a minimum SNDR of $72\,dB$, the width (W) and length (L) of the NMOS/PMOS current source (M_{16} and M_{13}) were selected for $12-$bit (i.e., $\sigma\left(\frac{\triangle I}{I}\right) = 2^{-7}$) matching accuracy, according to the expressions given in Equation 5.5 and 5.6 [73]. Further, perfect symmetry and common centroid layout techniques are used through the complete DAC design. The total current consumed by all three DACs including bias circuits is around $600\,\mu A$.

$$W^2 = \frac{2I}{\mu C_{ox}\sigma^2\left(\frac{\triangle I}{I}\right)}\left[\frac{A_\beta^2}{V_{ov}^2} + \frac{4A_{VT}^2}{V_{ov}^4}\right] \tag{5.5}$$

$$L^2 = \frac{\mu C_{ox}}{2I\sigma^2\left(\frac{\triangle I}{I}\right)}\left[A_\beta^2 V_{ov}^2 + 4A_{VT}^2\right] \tag{5.6}$$

5.3.5 Interface Circuit

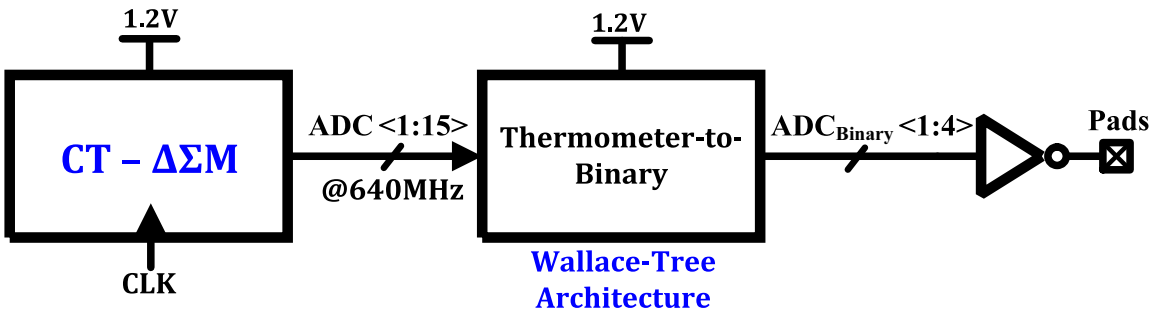

Figure 5.16: Block diagram of the interface circuit.

The output of the CT-$\triangle\Sigma$M is a $15-bit$ thermometer coded signal at the data rate of $640\,MHz$. In order to perform the chip evaluation without limiting the dynamic

performance of the output driver due to common-mode noise, it is necessary to reduce the data bus width. Thus, an interface circuit, which includes a Wallace-Tree thermometer-to-binary circuit [68], is employed on-chip, as shown in Figure 5.16.

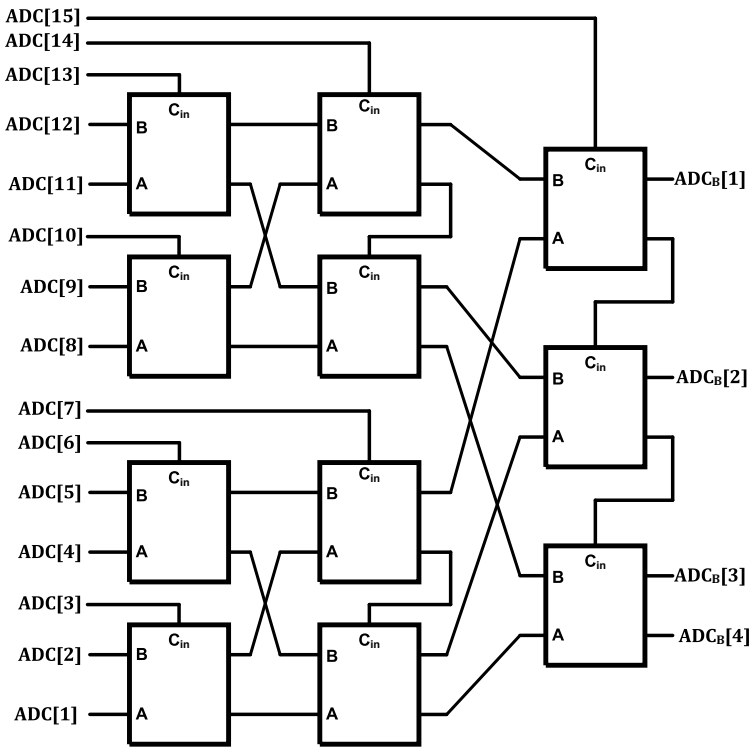

Figure 5.17: Block diagram of the Wallace-Tree thermometer-to-binary encoder

Figure 5.17 shows the Wallace-Tree thermometer-to-binary decoder, which counts the number of $1's$ in the $15-bit$ input signal and gives an equivalent $4-bit$ binary value. The $4-bit$ binary outputs are generated using 11−full-adders. The main advantage of this architecture when compared to others is the global bubble error correction and suppression (i.e., it effectively corrects the bubble error which may occur at the output of the flash ADC) [68]. The worst case conversion time of a Wallace-Tree thermometer-to-binary decoder is more than a couple of clock periods as it is not synthesized. Thus, to avoid the latency, a pipelining technique has been

Parameter	Measured Results
Signal Bandwidth/Clock Rate	$20MHz/640MHz$
Full Scale of Flash ADC	$1.6V_{pp,diff}$
Input Swing for peak SNR	$-1.93dBFS$
SNDR/SNR/Dynamic Range	$60/61.5/60dB$
Active Area	$0.4mm^2$
Process/Supply Voltage	CMOS $0.13\mu m$ IBM / $1.2V$
Power Dissipation (core)	$14mW$
Figure of Merit	$380fJ/level$

Table 5.3: Summary of measured ADC performance.

implemented in the encoder. Though it increases the hardware complexity, it greatly relaxes the design requirement of high-speed adder. Thus, the logic delay of each stage is limited to less than a clock cycle.

5.4 Test Setup and Measurement Results

The test setup for high-speed multi-bit $\Delta\Sigma$ ADC is the same as for the single-bit $\Delta\Sigma$ ADC in Chapter 4 as shown in Figure 4.24, except for a few additional discrete components that are added on the same board to facilitate multi-bit testing requirements. Figure 5.18 shows the block diagram of the complete test setup for prototype multi-bit $\Delta\Sigma$ ADC characterization. The required reference voltages (i.e., V_{bot} and V_{top}) for the 4-bit Flash ADC are generated off-chip using a discrete component $AD8138$ [70], and the outputs are sufficiently bypassed by using both on-chip and off-chip capacitor banks. The input reference voltage for the $AD8138$ is generated from a low-noise, high precision DAC. Thus, the noise on the reference voltages are highly controlled.

The modulator outputs are brought out of the chip using on-chip CMOS buffers. The coupling and crosstalk between the $4-bit$ data bus/reference output clock pins and bond wires resulted in slight corruption of the output clock and data. Thus,

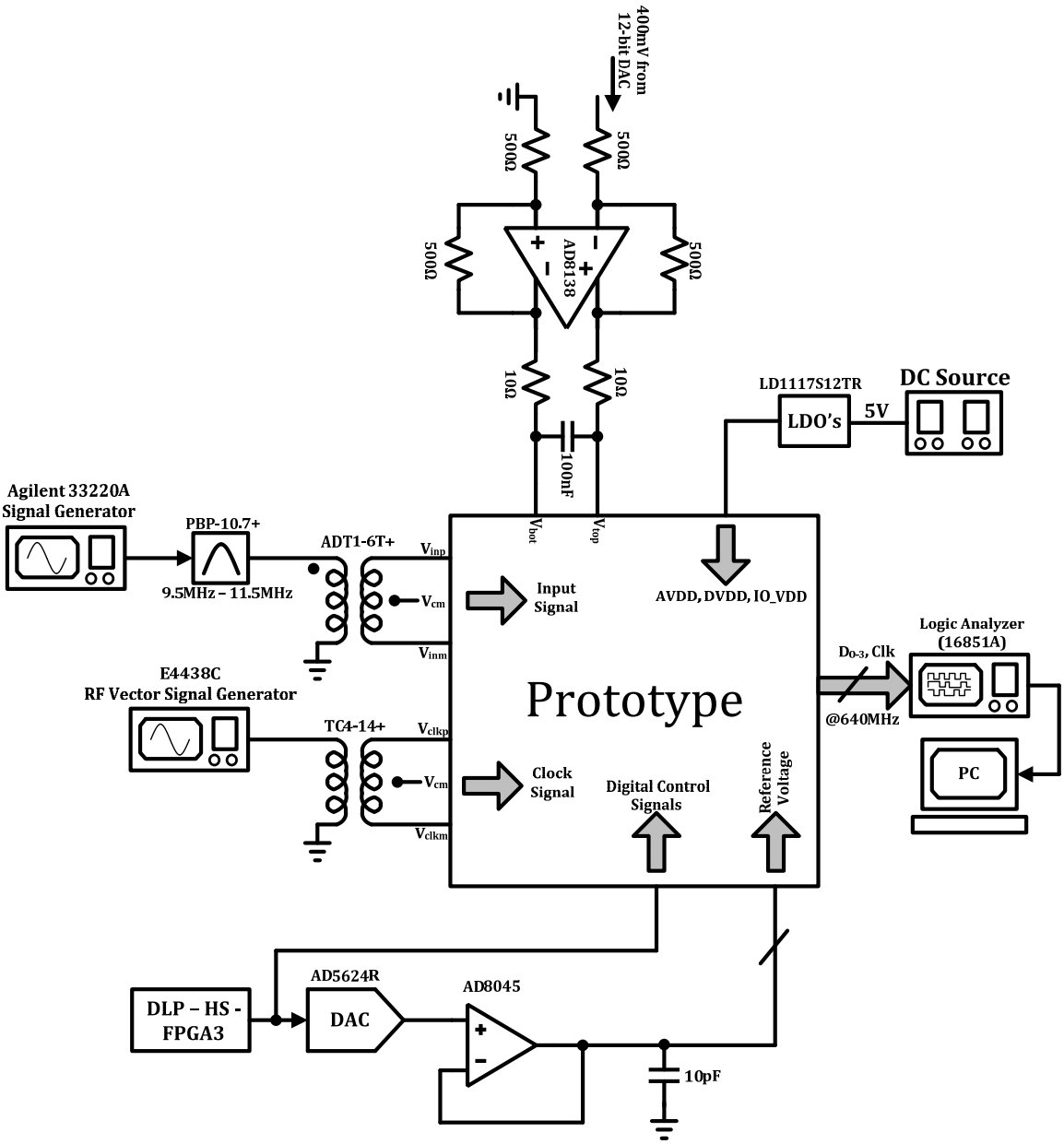

Figure 5.18: Block diagram of test setup.

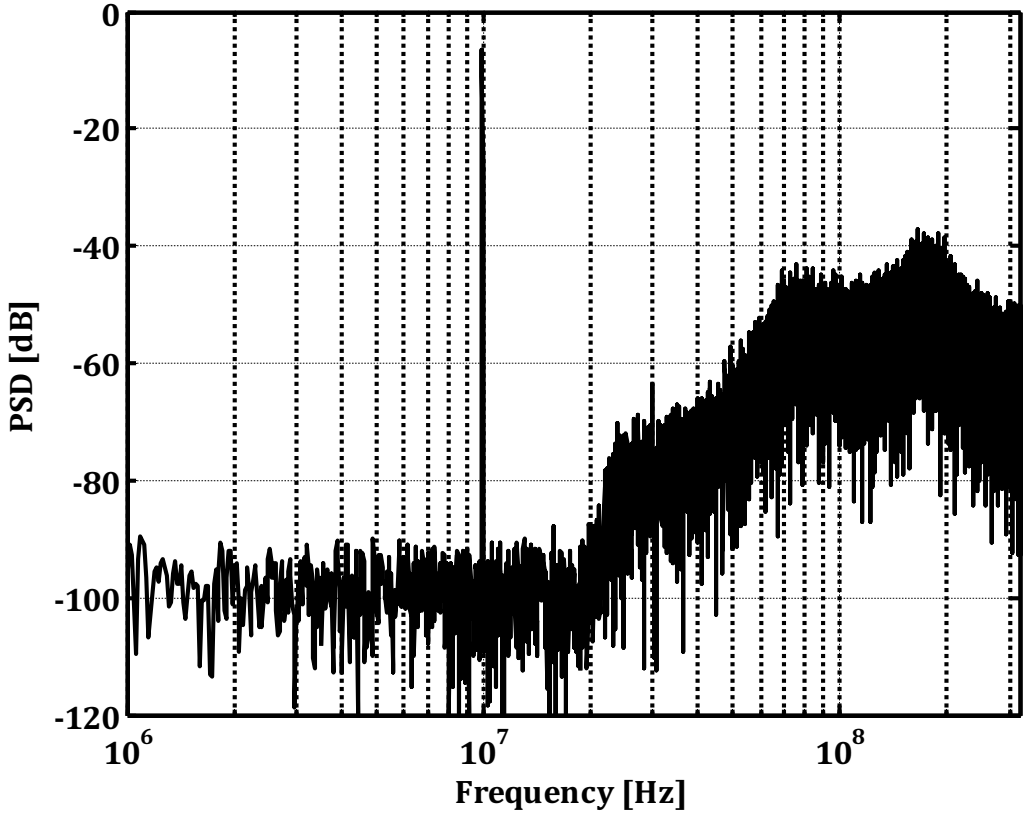

Figure 5.19: PSD for a $-2.8dBFS$ tone @$9MHz$.

the asynchronous sampling feature is used and data are captured using an Agilent 16851A Logic Analyzer. The data was processed offline on a PC and re-sampled using the recovered clock. In this work, a $32K$ point Blackman-Harris window is used to evaluate the FFT on the collected data. Figure 5.19 shows the power spectral density of the modulator output for a $10\,MHz$ input tone for an amplitude that results in the peak SNDR. The peak SNDR is $60\,dB$. The measured dynamic range of the modulator is $66\,dB$. The maximum stable amplitude is measured to be $-1.93\,dBFS$. A summary of measured performance is given in Table 5.3. Also, Table 5.4 compares the performance of our design with that of state of the art multi-bit high speed $\Delta\Sigma$

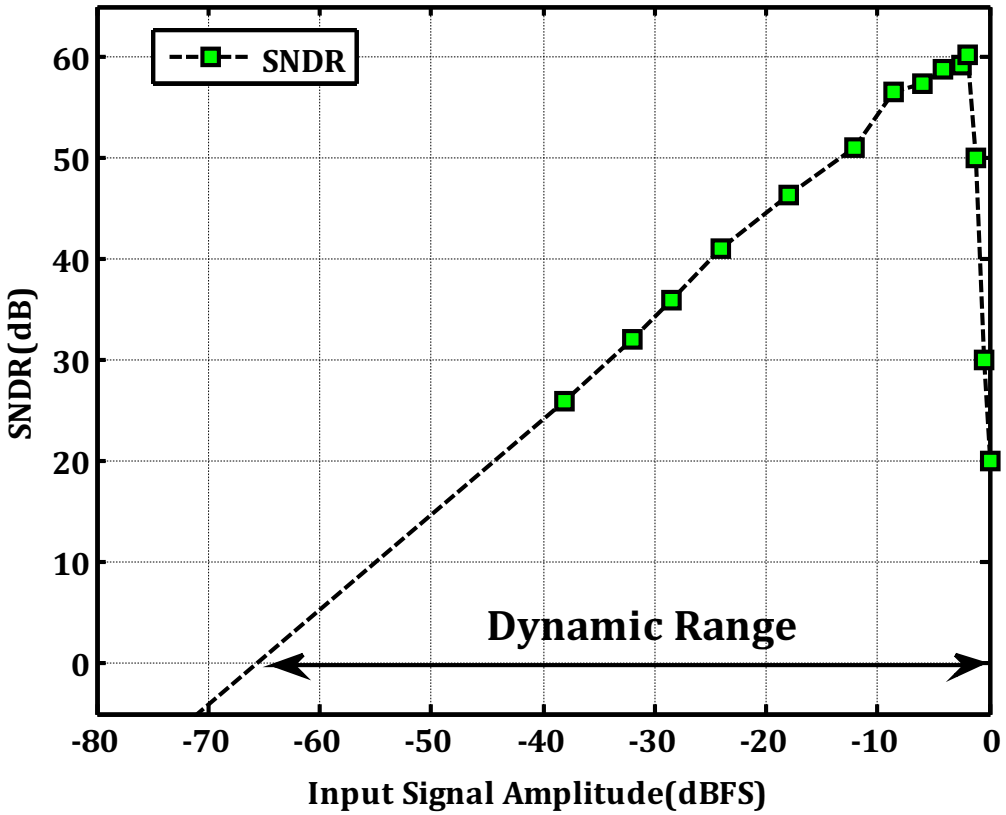

Figure 5.20: Measured SNDR - the dynamic range is $66dB$.

modulators in 130/180 nm CMOS process. The peak SNR expected from simulations is about $70\,dB$, which is $10\,dB$ more than what was measured. The loss is attributed to spurious coupling (through the package pins and the bond wires) of the high-speed signals on the the board due to the use of high voltage swing CMOS buffers. In order to avoid the same errors in subsequent high-speed chips by our group in the future, low-voltage differential signaling drivers (LVDS) were designed and used for data as well as clock outputs.

Reference	Feature Size (nm)	BW (MHz)	SNR/DR (dB)	Power (mW)	FOM (fJ/level)
[17]	130	20	76.0/80.0	20	97
[33]	180	15	67.2/70.0	20.7	368
[44]	180	32	57/64	47.6	152
[51]	130	20	81.2/80.0	87.0	231
[74]	130	10	86.0/90.0	40.0	122
This work	130	20	61.2/66	14	380

Table 5.4: Comparison with other $\Delta\Sigma$ modulators.

5.5 Summary

An 3^{rd}-order continuous-time $\Delta\Sigma$ modulator sampling at $640\,MS/s$ (the highest speed in this technology) is designed, fabricated in a $0.13\,\mu m$ CMOS process and tested. The complete system and circuit-level design of wide bandwidth CT-$\triangle\Sigma$ ADC is detailed with complete analysis of non-idealities effect, especially quantizer, on overall modulator performance. The modulator achieves $10-bit$ resolution with $20\,MHz$ conversion bandwidth. As a result of a combination of several techniques discussed in the Chapter 3 and 5, the designed modulator consumes only $14\,mW$ and achieves a figure of merit (FoM) of $0.38\,pJ/level$.

CHAPTER 6

PROPOSED WIDEBAND MULTI-BIT CT-$\triangle\Sigma$ ADC WITH TWO-STEP QUANTIZER

In this chapter, we propose the first hybrid continuous-time multi-step quantizing delta-sigma ADC architecture. The wideband $\Delta\Sigma$ modulator in the ADC employs a two-step 5-bit quantizer, consisting of only 13 comparators designed in a $0.13\mu m$ CMOS technology. The chapter also expounds how the proposed $\Delta\Sigma$ modulator architecture takes advantage of (i) higher resolution resulting from the two-step quantization technique, and (ii) excess loop-delay compensation of more than one clock cycle; to achieve a power optimized, high dynamic range modulator with a wide conversion bandwidth at a reduced sampling frequency. To facilitate design with the proposed architecture, a robust systematic design method is introduced to determine the loop-filter coefficients by taking into account the non-ideal integrator response, such as the finite opamp gain and the presence of multiple parasitic poles and zeros. Further, the complete system-level simulation is presented, to analyze the effect of quantizer non-idealities such as the offset and gain error in the two-step sub-ADC, and the current mismatch between the most-significant bit (MSB) and LSB elements in the feedback DAC. The pertinent design trade-offs involved with the proposed architecture have been discussed throughout the chapter and corroborated with simulation and measurement results.

6.1 Introduction

As discussed earlier in Chapters 3 and 5, further increasing the quantizer resolution is a favorable architectural choice in low-OSR CT-$\triangle\Sigma$ modulator designs. Further, we saw that larger number of levels in the quantizer (i.e., lower LSB size) allows a higher OBG, which results in overall higher noise-shaping performance [19, 33]. However, increasing the quantizer resolution above 4-bit results in an exponential increase in circuit complexity, as an increase in 1-bit in the quantizer resolution requires doubling the number of comparators. Also, the number of unit elements in the feedback DAC are doubled, leading to higher complexity and an increased loop-delay contributed by the DAC DEM or data-weighted averaging (DWA) logic. These require power hungry analog driving circuitry to drive the large capacitive load formed by the multi-bit quantizers (for any increase in resolution > 4), and also increases the area and circuit complexity exponentially. Recently, hybrid DT-$\triangle\Sigma$ modulators with multi-step quantization, where the resolution of quantizer > 4, have been reported [75, 76]. These modulators exploit the lower quantization noise available with multi-step quantizers by developing techniques to accommodate the increased quantizer latency (z^{-N}). This is achieved by canceling the coarse quantization noise, and employing distributed feedback into the input of intermediate MDAC stages of the pipelined quantizer to introduce desired transfer function coefficients corresponding to a higher-order NTF, with the order set by the quantizer latency ($N \cdot T_s$). However, a simple analysis of these architectures reveals that they implicitly require precise cancellation of analog-transfer functions in order to realize an higher-order NTF for the LSB quantization noise. MSB and LSB quantization noise leakage due to the imperfect analog-cancellation limits the achievable dynamic performance of these

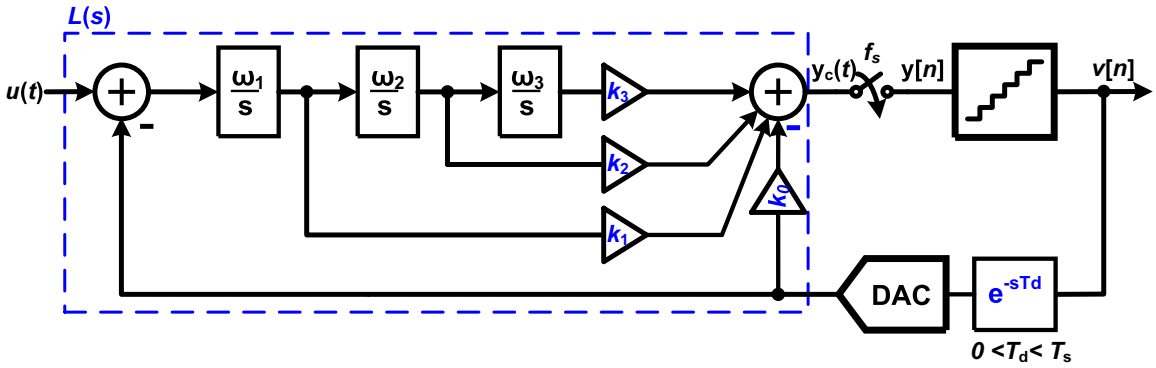

Figure 6.1: General block diagram of a traditional 3^{rd}- order CT-$\triangle\Sigma$ modulator.

designs. Thus, it is desired that a new architecture is evolved where the MSB decision in the quantizer, made within the clock period, is not directly fed to the input of the feedback loop. Instead, only the LSB quantization noise is fed back, albeit with higher latency, into the loop and the loop is stabilized for an excess delay larger than one clock cycle.

In order to take advantage of quantizer resolution above 4-bit, we propose the first CT-$\triangle\Sigma$M, which employs a two-step quantizer [35, 36, 37]. Due to two-step quantization, an additional delay greater than the clock period is compensated using a sample-and-hold (S/H) based technique illustrated in [77]. Typically in a conventional CT-$\triangle\Sigma$M, ELD is selected to be smaller than 0.5 for reduced sensitivity of the loop-filter coefficients with process variation. However, with this ELD compensation method, an ELD of 1.5 can be allowed that can lead to up to a three-fold increase in the maximum possible sampling rate in the selected technology. Alternatively, for a constant sampling rate, the OSR can be further reduced to allow a larger conversion bandwidth to achieve the same SNDR and dynamic range specifications. In this prototype design, the sampling frequency is chosen as $400\,MS/s$, which is 1.5 times lower than $640\,MS/s$, while employing a two-step quantizer to achieve the same

dynamic performance specifications from Chapter 5. The proposed design is meant to demonstrate the performance advantages of the CT-$\triangle\Sigma$ architecture with multi-step quantization. Further, this novel approach paves the path towards hybrid CT-$\triangle\Sigma$ and pipelined ADCs, which combine the strengths of pipelined ADCs (high quantizer resolution) with the noise-shaping and anti-alias filtering feature of $\triangle\Sigma$, to meet the ADC specifications required in the next-generation wireless standards such as IEEE 802.11ac+ [7, 10].

6.2 System-level Design

The system-level design for the proposed architecture follows from the multi-bit CT-$\triangle\Sigma$ design from Chapter 5. This section discusses the various architectural choices made in the proposed CT-$\triangle\Sigma$ modulator, which arise from incorporation of a two-step quantizer with latency greater than a clock cycle. Other system design considerations such as circuit noise budgeting are similar to the discussion in the previous chapter.

6.2.1 Systematic Design of Noise-Transfer Function and Modulator Architecture with ELD >1 Clock Cycle

Figure 6.1 shows the block diagram of the traditional single-loop CT-$\triangle\Sigma$ modulator. In this figure, $L(s)$ is the 3^{rd}order continuous-time loop filter architecture, implemented using CIFF architecture, whose output is sampled and quantized at frequency, f_s , or equivalent time period T_s. Further, k_0 is the gain of the direct path introduced to compensate for an ELD of less than one clock cycle. Conventionally, the loop-filter coefficients $K = [k_0\, k_1\, k_2 \ldots k_N]$, where N is the order of the loop filter, are obtained by least-square fitting the impulse response of discrete-time loop filter

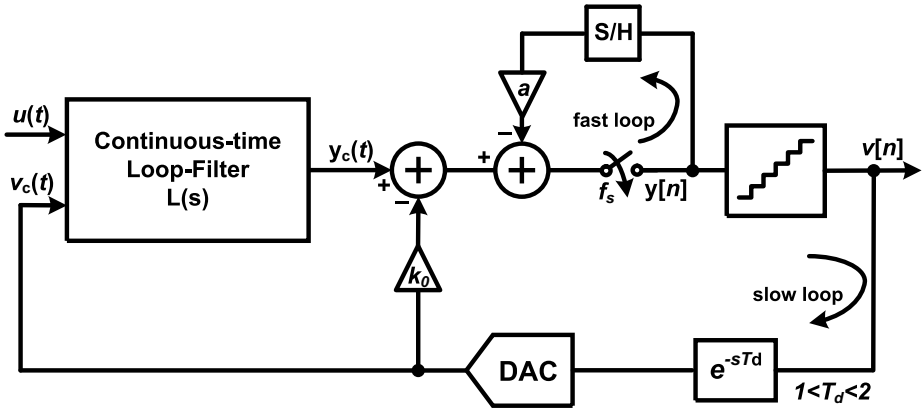

Figure 6.2: Block diagram of the CT- $\triangle\Sigma$ modulator with a S/H based fast-loop.

$L_d(z) = 1 - NTF^{-1}(z)$ to the continuous time loop filter, $L_c(s)$, using the impulse invariance transformation for a given delayed feedback DAC pulse shape as discussed in Section 3.5.3 [19, 78]. Also, the ELD compensation method using the direct path around the quantizer (k_0) performs adequately as long as the excess delay is less than a clock cycle (i.e., $ELD < T_s$).

Figure 6.2 shows the modified CT-$\triangle\Sigma$M block diagram, incorporating an ELD compensation technique of more than one clock cycle [77]. Here, the ELD compensation is achieved by using an additional feedback path around the sampler using a S/H with a gain $'a'$. The purpose of this fast loop is to restore the second sample (i.e., $l[1]$) of the open-loop response, $l[n]$. Then, the remaining samples of $l[n]$ are restored by appropriately choosing loop-filter coefficients $K = [k_0\, k_1\, k_2 \ldots k_n]$. It is thus ensured that all the samples of $l[n]$ are restored and CT-$\triangle\Sigma$ loop stability is preserved. However, due to this additional loop formed by the S/H, an extra zero appears at $z = -a$ in the resulting noise-transfer function. The resulting noise-transfer function $NTF_{new}(z)$ is of the form

$$NTF_{new}(z) = (1 + az^{-1}) \cdot NTF_{orig}(z) \tag{6.1}$$

where $NTF_{orig}(z)$ is the originally desired NTF [77]. The numerical open-loop impulse response fitting method used in [41] doesn't perform well in the presence of additional poles and zeros in the opamp and may even lead to instability in the ADC. In order to consider the effect of integrator non-idealities, including the finite op-amp gain (A_{DC}) and the presence of additional poles and zeros, a systematic method has been developed, similar to [43], to find the loop-filter coefficients. The loop-filter coefficients ($\mathbf{K}$) are calculated by fitting the closed-loop response of the CT-$\triangle\Sigma$ loop to the desired NTF, by using the condition 6.2.

$$[h_0\, h_1\, h_2 \ldots h_n]\mathbf{K} = f[n] - h[n] \otimes f[n] \tag{6.2}$$

Here $h[n]$ and $f[n]$ are the impulse response of the $NTF_{orig}(z)$ and $(1 + az^{-1})$, respectively. Further, $h_0[n] = l_0[n] \otimes h[n]$, $h_1[n] = l_1[n] \otimes h[n]$, ..., where $l_0[n]$ and $l_i[n]$ represent the sampled DAC pulse response of the direct path and at the output of the i^{th} integrator.

Even though, the ability to tolerate an ELD in the range of 1 to 1.5 clock cycle increases the achievable sampling rate by a factor of 2, there are a few drawbacks. Figure 6.3 shows the comparison between the resultant OBG (OBG_{new}) with $1 < ELD < 2$ with the desired OBG (OBG_{orig}). The larger OBG_{new} of the NTF_{new} results in increased wiggling of the quantizer output sequence. As a consequence, the signal variation at the input of the quantizer ($y_c(t)$) is increased by a larger extent and thus overloads the quantizer more often, which significantly reduces the MSA and renders the modulator to be predisposed to instability. Therefore, in order to design a stable CT-$\triangle\Sigma$ modulator with $ELD > 1$, either a lower OBG should be used ($OBG \leq 2$) or a higher resolution quantizer (resolution > 4) utilizing a lower

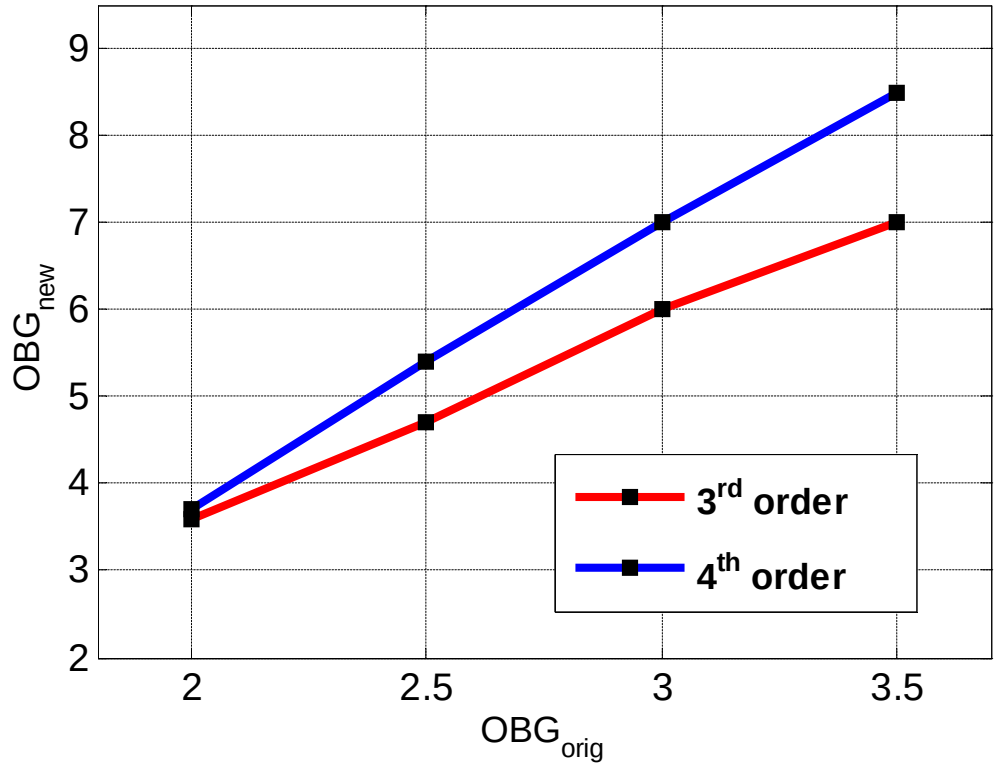

Figure 6.3: $OBG_{orig}\,Vs\,OBG_{new}$ for $3^{rd}$and 4^{th}order CT-$\triangle\Sigma$ modulators.

LSB size must be used to achieve the desired MSA in the range of 0.8. Since, the proposed $\triangle\Sigma$M uses a 5-bit two-step quantizer, which allows for an aggressive OBG of $NTF_{orig}(z)$ to 3, and achieves the desired performance with just 13 comparators (as opposed to 31 for a 5-bit Flash sub-ADC). Also, for the low-OSR $\triangle\Sigma$ designs, increasing the order above three does not provide significant improvement in SQNR [33]. However, to compensate for the increase in the in-band noise floor due to the additional zero in $NTF_{new}(z)$, an extra order is required in the modulator.

In this work, a $4^{th}-$order CT-$\triangle\Sigma$ modulator architecture is investigated with a 5-bit two-step quantizer. In this design, the $OBG_{orig} = 3$ is selected to restrict the corresponding OBG_{new} to an acceptable limit for stability. Thus, to achieve a SNR of

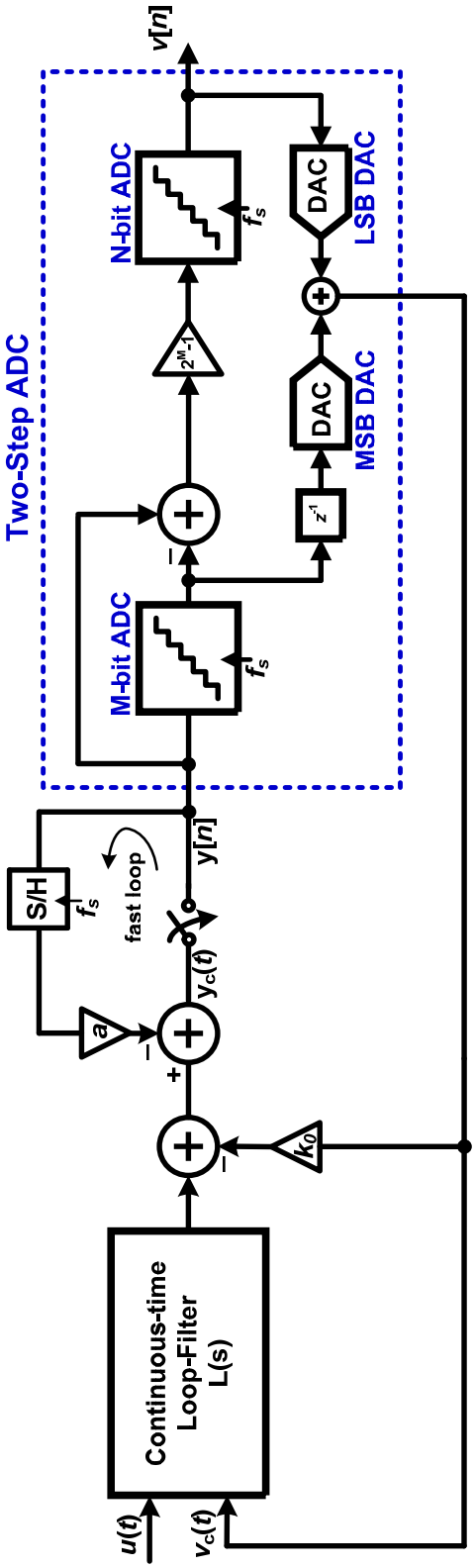

Figure 6.4: Block diagram of proposed CT-$\Delta\Sigma$ modulator with two-step quantizer.

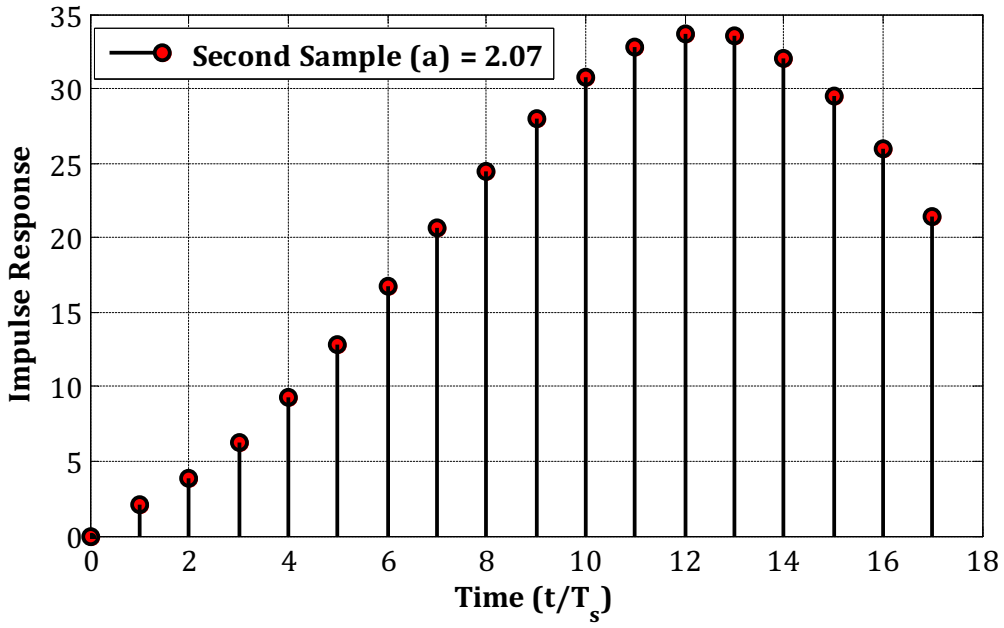

Figure 6.5: Discrete-time equivalent impulse response of the loop filter $L(s)$ for the chosen $NTF(z)$.

above $72\,dB$ in a signal bandwidth of $20\,MHz$, and a forth-order $NTF_{Orig}(z)$ with a low oversampling ratio of $OSR = 10$ is chosen. Figure 6.4 shows the block diagram of the proposed modulator with two-step ADC. The system-level requirement of these ADCs and DACs will be discussed in details later in this chapter.

The systematic design procedure for the modulator architecture is as follows: First, a desired 4^{th}-order inverse-Chebyshev $NTF(z)$, given in equation 6.3 synthesized using *Schreier Toolbox* [19], is chosen for the target SQNR of $72\,dB$.

$$NTF_{Orig}(z) = \frac{\left(z^2 - 1.985z + 1\right)\left(z^2 - 1.916z + 1\right)}{\left(z^2 - 0.8102z + 0.1955\right)\left(z^2 - 1.025z + 0.5691\right)} \tag{6.3}$$

Then, by using the *impL*1 command in the *Schreier's Toolbox* [19], the value of the second sample '**a**' is found.

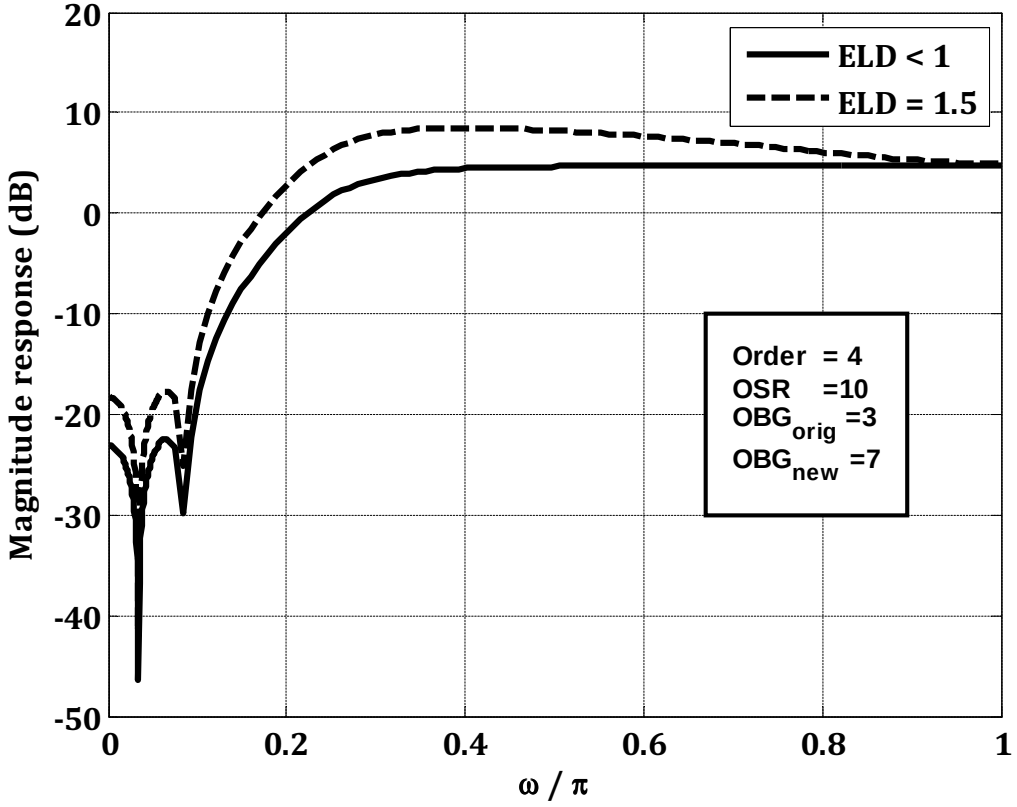

Figure 6.6: $|NTF_{orig}(e^{j\omega})|$ showing the effect of $(1 + az^{-1})$ in the $NTF_{new}(e^{j\omega})$.

Figure 6.5 shows the discrete-time equivalent impulse response, $l[n]$, of the loop filter $L(s)$ for the chosen $NTF_{orig}(z)$. Thus, the NTF_{new} is evaluated as

$$NTF_{new}(z) = (1 + 2.07z^{-1}) \cdot NTF_{orig}(z) \tag{6.4}$$

Figure 6.6 compares the desired $NTF_{orig}(z)$ with the resulting $NTF_{new}(z)$ for the design. In other words, Figure 6.6 illustrates the magnitude responses of $NTF_{orig}(e^{j\omega})$ and $NTF_{new}(e^{j\omega})$ before and after the ELD compensation, greater than one clock cycle, respectively. Originally the NTF is designed for an OBG of 3, and once the ELD is compensated, the resulting OBG is observed to be equal to 7. As the proposed

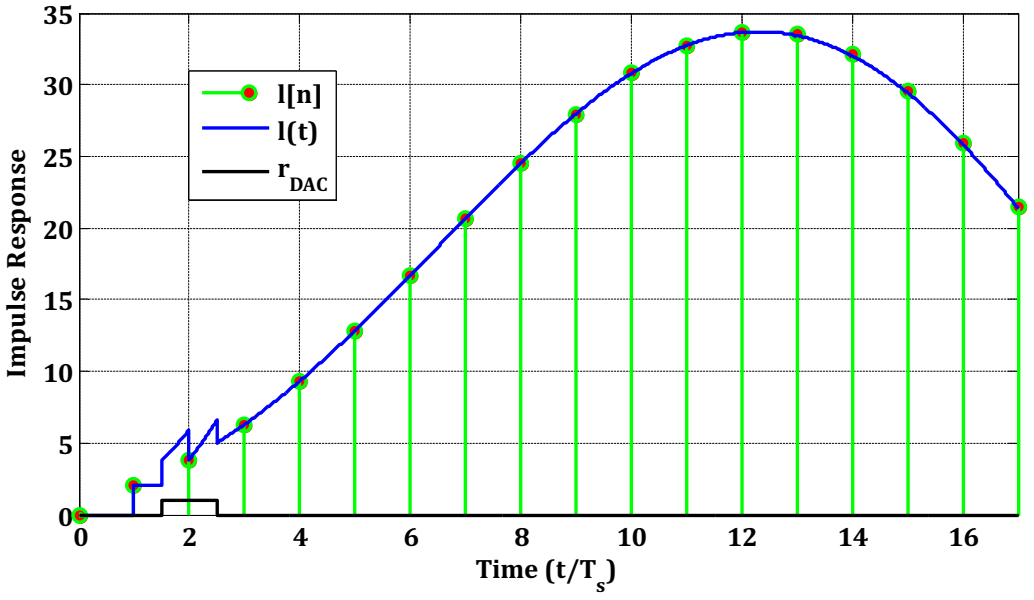

Figure 6.7: Impulse response at the output of 4^{th}- order CT-loop filter, $L_{new}(s)$, for the delayed DAC pulse (ELD = 1.5) and sampled impulse response of $L(z)$.

design uses the 5-bit two-step quantizer, the increased OBG is tolerated due to the smaller LSB size, and achieves a reasonable MSA value of 0.8. Then, after removing the second sample and advancing the remaining samples, the new $l_{new}[n]$ is evaluated (i.e., $[0\ l_2\ l_3 \ldots]$). Using the resultant $l_{new}[n]$, and the half clock cycle delayed DAC pulse shape, $L(s)$ is computed using *SIMULINK* without considering opamp non-idealities, and is given as

$$L_{new}(s) = \frac{\left(1.6633s^4 + 3.8265s^3 + 2.2719s^2 + 1.0267s + 0.2076\right)}{\left(s^2 + 0.0991s^2 + 0.0012\right)} \tag{6.5}$$

After this, using the *MATLAB* fitting function *prony*, the equivalent IIR transfer function ($L_{new}(z)$) is calculated with opamp non-idealities and the resulting NTF degradation can be observed and corrected using Equation 6.2. Figure 6.7 shows the impulse response at the output of the 4^{th}-order CT loop filter, $L_{new}(s)$, for the

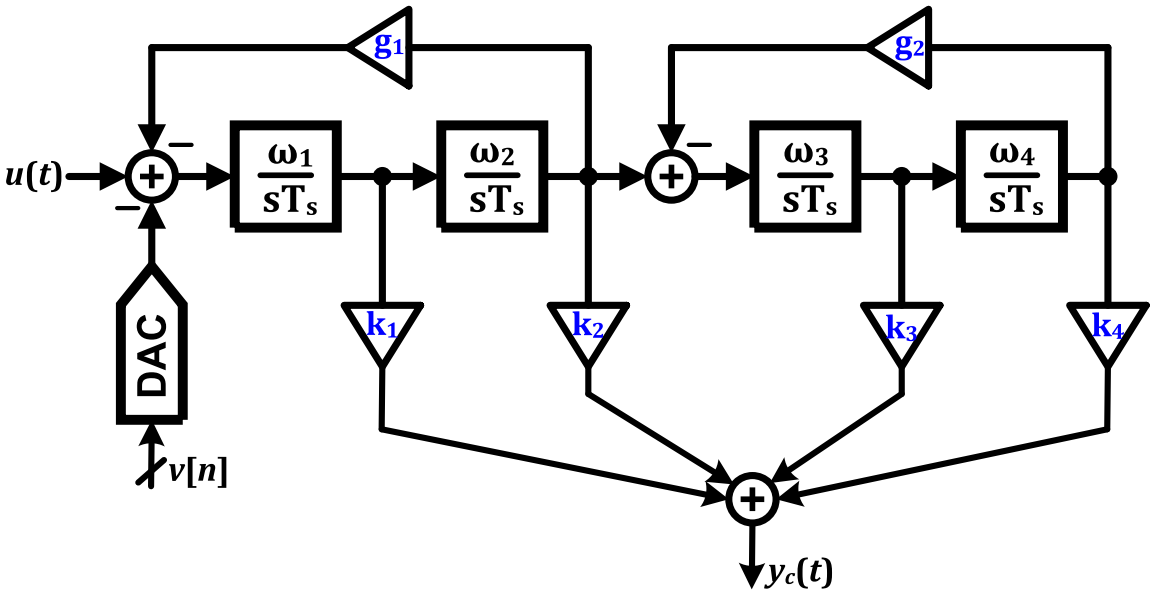

Figure 6.8: The 4^{th}- order loop-filter employed in the CT-$\triangle\Sigma$ modulator.

delayed DAC pulse and the sampled impulse response of $L(z)$. Figure 6.7 clearly shows that $l(t)|_{t=nT_s} = l[n]$ (i.e., the first sample is restored by the S/H fast path and the remaining samples are restored by the direct path, k_0, and the loop filter, $L_{new}(s)$).

A 4^{th}-order feed-forward loop-filter architecture is chosen to realize $L_{new}(s)$, as shown in Figure 6.8. The modulator architecture used in Chapters 4 and 5 avoids the usage of the power hungry summing amplifier by feeding back the differentiated value of feedback DAC k_0 to the last integrator. However, since this design employs a 5-bit quantizer, implementing three 5-bit feedback DACs may increase the circuit-design complexity. Thus, by trading the power consumption with the circuit complexity, a traditional feed-forward architecture is chosen as a reasonable compromise to demonstrate the proposed concept. Further, the loop-filter coefficients are computed by incorporating the opamp non-idealities using the systematic design procedure described in Section 6.2.1. Further, due to the use of a 5-bit quantizer, the

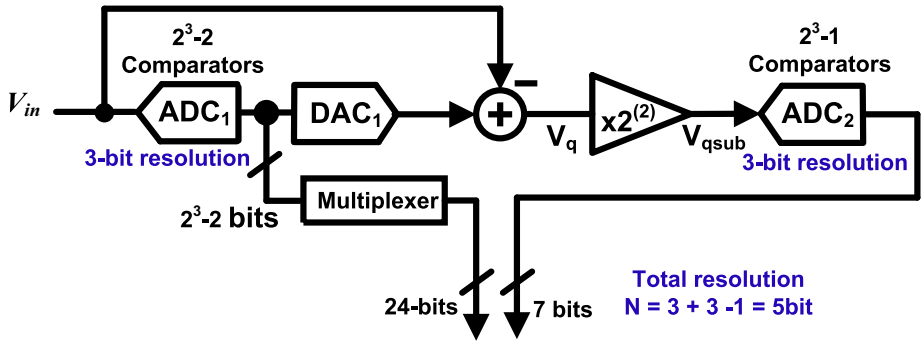

Figure 6.9: Block diagram representation of a two-step Flash quantizer.

slew rate requirements on the first opamp in the loop filter are greatly relaxed, which in turn saves power. The individual design specifications for each of the opamps were obtained through extensive behavioral simulations performed using the SIMSIDES Toolkit in Matlab/Simulink [79, 80].

6.2.2 System-Level Requirements of Two-Step Quantizer

Figure 6.9 shows the system-level block diagram representation of the 5-bit two-step Flash ADC used in the CT-$\Delta\Sigma$M. It comprises coarse and fine sub-ADCs with a Subtractor-cum-Residue amplifier for signal conditioning.The coarse sub-ADC and the residue subtractor and gain stage are together called an MDAC (multiplying DAC). The individual resolution of the coarse and fine ADCs are 3 bits each. The additional bit redundancy in the coarse sub-ADC allows the quantizer to absorb a maximum of $0.5\,LSB$ comparator offsets. To accommodate a $0.5\,LSB$ error at V_{qsub} (output of the Subtractor), an offset of $0.5\,LSB$ is added to the resistor string (i.e., to the bottom reference voltage (V_{bot}) of the Flash ADC). Similarly, to always keep V_{qsub} lesser than V_{top}, the last reference voltage from the resistor string has been removed.Thus, the resistor string reference voltages for the coarse stage are

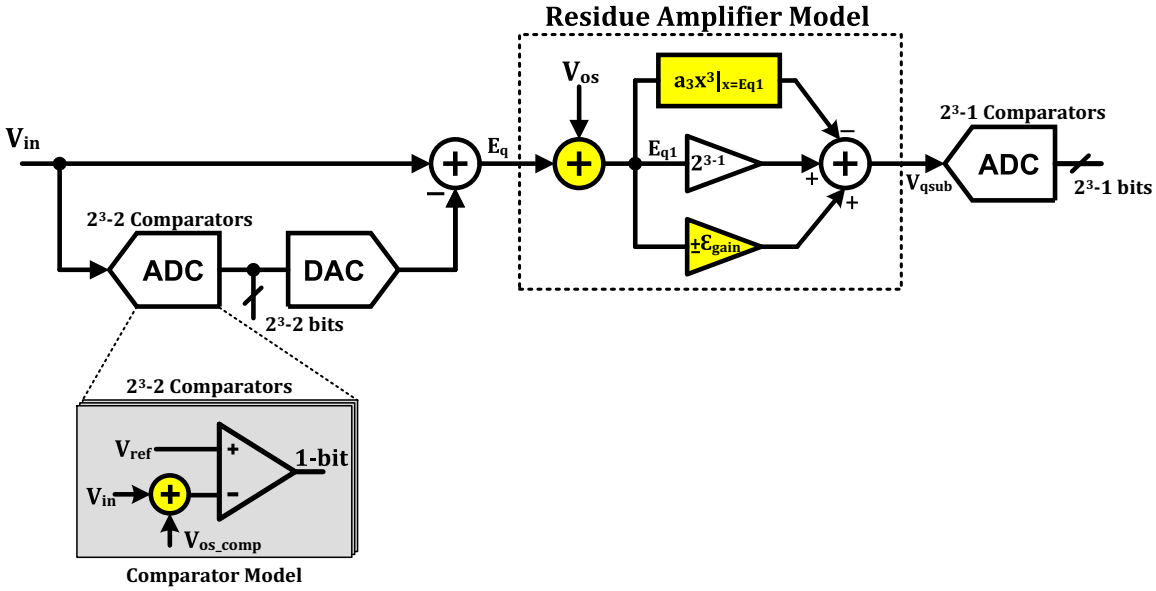

Figure 6.10: Block diagram representation of two-step Flash quantizer.

given by $V_{bot} + 1.5LSB$, $V_{bot} + 2.5LSB \ldots V_{bot} + 6.5LSB$. This results in $2^3 - 2 = 6$ comparators in the coarse stage. The coarse sub-DAC is followed by a 3-bitnary switched-capacitor DAC. The output of a DAC is directly coupled to the switch-capacitor residue amplifier, or subtractor, which subtracts and generates the amplified version of the residue V_q by a gain of 4. The residue amplifier drives the 7 comparators in the fine stage. Thus, the total resolution of the ADC is 5 *bits* as illustrated in Figure 6.9.

The key building blocks of any multi-step ADCs, such as two-step or pipelined ADC, are the sub-ADCs (i.e., coarse and fine sub-ADCs), the sub-DAC and the gain or residue amplifier that interfaces the two successive converter stages [5, 6]. In practice, these blocks are not ideal, and their imperfections have distinct effects on the overall ADC accuracy [5, 6]. Especially, in a standalone multi-step ADC, these blocks have to meet very stringent speed, offset, noise, and linearity requirements

to satisfy the overall ADC accuracy requirements. To optimize these parameters in standalone multi-step ADCs, a wide variety of techniques have been developed in the past decades, such as stage scaling, optimization of the per-stage resolution, and amplifier sharing techniques [20, 81].

However, as discussed in the previous chapter, any non-idealities introduced by the Flash converter inside the $\triangle\Sigma$ loop can be noise-shaped and hence tolerated by the loop to some extent, with marginal SNDR degradation. Thus, based on the above argument, it follows that any non-idealities introduced by the two-step ADC are also noise-shaped and accommodated by the $\triangle\Sigma$ loop. However, for overall design optimization, it is necessary to understand the maximum tolerable level of non-idealities in the $\triangle\Sigma$ loop. In the two-step ADC, the dominant non-idealities are:

- Random comparator offsets in the individual sub-ADC stages
- An error in the precise gain required from the residue amplifier, its offset and contributed non-linearity.

Figure 6.10 shows the simplified two-step ADC linear model used in *SIMULINK* to study the effects of non-ideal artifacts on the in-band SNDR of the $\triangle\Sigma$ loop. The main sources of errors in Flash ADCs include offsets and static non-linearity arising from misaligned decision levels due to comparator offsets or inaccurate reference levels. This error is modeled as a DC random variable, $V_{os,comp}$, which is added to each comparators input as shown in Figure 6.10. Similar to the sub-ADC, the main sources of errors in the sub-DAC include offset (V_{os}), gain errors (ε_{gain}) and non-linearity (for simplicity only 3^{rd}-order harmonic distortion coefficients are considered, i.e., a_3). These errors are also modeled using non-linear elements in *SIMULINK,* as shown in Figure 6.10. From Figure 6.10, the output of the residue amplifier can be written as

$$V_{qsub} = V_{os}\,(4 \pm \varepsilon_{gain}) + E_q\,(4 \pm \varepsilon_{gain}) - a_3\,(E_q + V_{os})^3 \tag{6.6}$$

The following section illustrates the individual effect of these non-ideal terms in Equation 6.6, on the in-band SNDR.

6.2.2.1 Effect of Comparator Offset of Two-Step ADC on CT-$\triangle\Sigma$M

To evaluate the influence of the random offset on in-band SNDR, Monte-Carlo analysis is performed in *SIMULINK* using the above two-step ADC model. For each run, an array of uniformly distributed error signal, $V_{os,comp}$, with fixed mean ($\mu = 0$) and standard deviation (σ_{offset}), is generated and added to each comparator of the ADCs. The results of every iteration are collected and plotted, as shown in Figure 6.11.

From Figure 5.4, it is evident that the two-step ADC can effectively tolerate a maximum offset (σ_{offset}) of $0.2\,LSB$, with marginal impact on the resulting in-band SNDR, when compared to the traditional CT-$\triangle\Sigma$ from Figure 5.4. However, for a given mean and standard deviation above $0.2\,LSB$, it is more prone to in-band SNDR degradation and may even lead to instability, because the two-step ADC becomes *non-monotonic* for extreme values of the random offset with $\sigma_{offset} > 0.2\,LSB$. Thus, to avoid the modulator instability or SNDR degradation, the comparator offset should be kept lower than $\sigma_{offset} = 0.2\,LSB = 20\,mV$.

6.2.2.2 Effect of Residue Amplifier Non-idealities on CT-$\triangle\Sigma$M

Using the model illustrated in Section 6.2.2, the closed-loop CT-$\triangle\Sigma$ is simulated in *SIMULINK* where the linear gain error, $\pm\varepsilon_{gain}$, contributed due to component or unit element mismatch and insufficient open-loop gain of the opamp, is varied from -0.5 to 0.5 for different input-refereed offsets ($0.01\,LSB$, $0.05\,LSB$, & $0.1\,LSB$) of

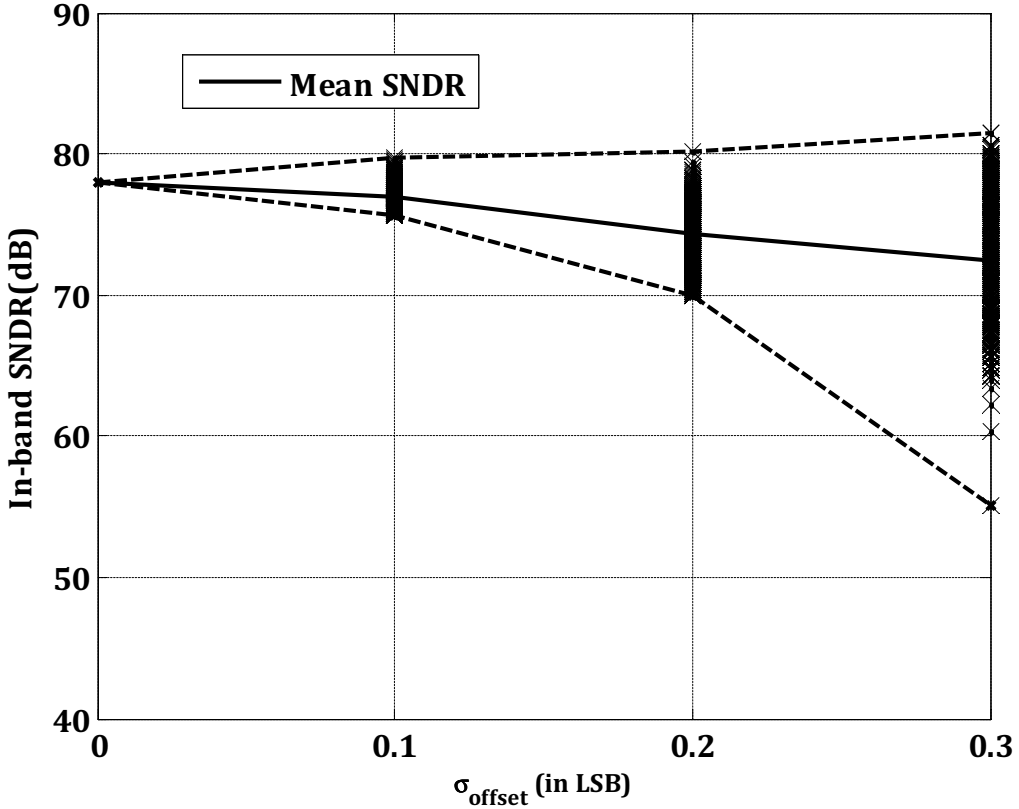

Figure 6.11: Effect of comparator random offset on in-band SNDR—for each level of offset, 500 trials were simulated. The lines show the modulators with the best 1% SNDR, mean SNDR and the worst 1% SNDR, respectively.

the opamp with a fixed 3^{rd}-order distortion gain of 0.5 (i.e., $HD_3 = 25\,dB$). The results are collected and plotted in Figure 6.12.

Figure 6.12 clearly illustrates that the $\triangle\Sigma$ feedback loop can tolerate almost $\pm 12.5\%$ gain error, $V_{os} = 0.01\,LSB$ and $a_3 = 0.5$ with marginal degradation in the in-band $SNDR$. Thus, the $\triangle\Sigma$ loop greatly relaxes the matching requirements of the sub-DAC and opamp performance requirements. Also, for the gain, $|\varepsilon_{gain}| > 0.5$, the two-step ADC becomes non-monotonic and may lead to instability in the modulator. Thus, to ensure robust operation of the modulator, the specifications obtained from

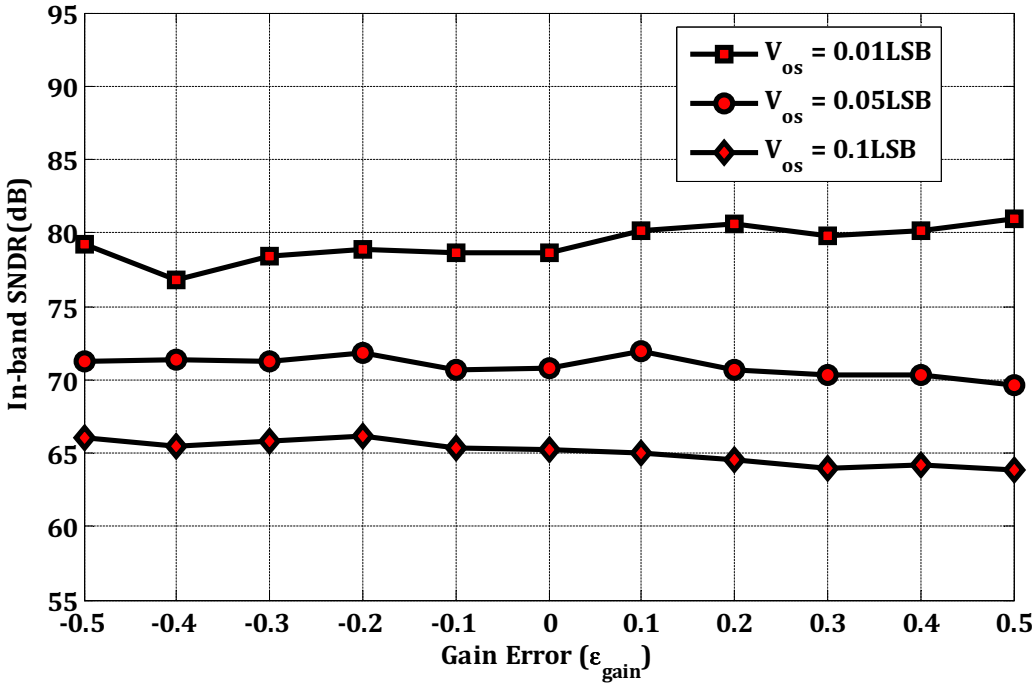

Figure 6.12: Effect of gain error (ε_{gain}), input-refereed operational amplifier offset (V_{os}) for fixed third-order linearity ($a_3 = 0.5$ or $SFDR = -21.58\,dB$)

behavioral simulation are extensively used in design and verification of the circuit-level implementation of the two-step ADC.

6.2.3 System-Level Requirements from DAC

Another important performance degradation source resulting from the two-step quantizer is the feedback DAC non-linearity. As we have seen in Chapter 5, the feedback DAC is one of the critical-design blocks in a $\Delta\Sigma$ ADC. From Figure 6.8, the illustrated modulator architecture employs two ADCs for realizing distributed feedback; DAC_1 is the main feedback DAC, and DAC_0 implements the fast feedback loop required for restoring third sample onwards on the open-loop impulse response.

With reference to Chapter 5, the k_0 DAC can tolerate a considerable amount

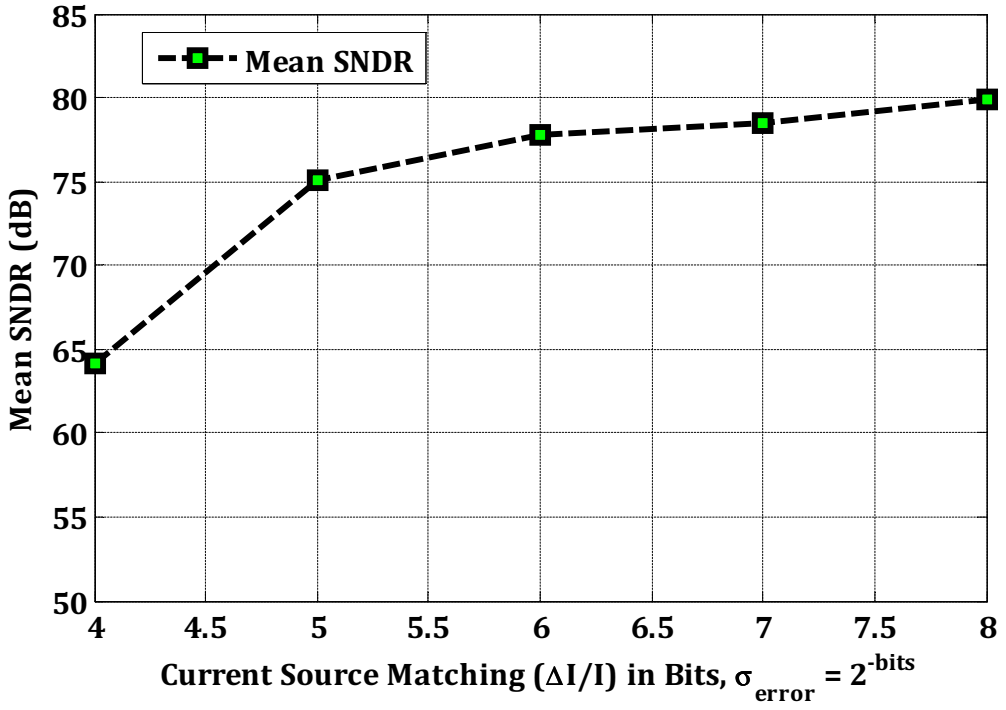

Figure 6.13: Behavioral-level simulation of modulator SNDR versus fast-loop DAC unit element mismatch−for each level of bits, 1,000 trials were simulated.

of unit-current mismatch errors. Figure 6.13 shows the behavioral-level simulation results for the modulator, where mean-SNDR is plotted against the mismatch in the fast-loop DAC unit-elements. From this result, it can be deduced that at least $6-7$ bit DAC linearity is necessary to avoid any performance degradation from the target SNDR. Similarly, Figure 6.14 shows the behavioral-level simulation of the modulator SNDR versus DAC unit-element mismatch in the main feedback path. Here, it clearly shows that the linearity of the main feedback DAC has to be at least equal to or greater than the targeted SNDR of the overall modulator. Consequently, the design of the main feedback DAC, DAC_0, is of critical importance to determine the performance of the overall $\Delta\Sigma$ ADC design.

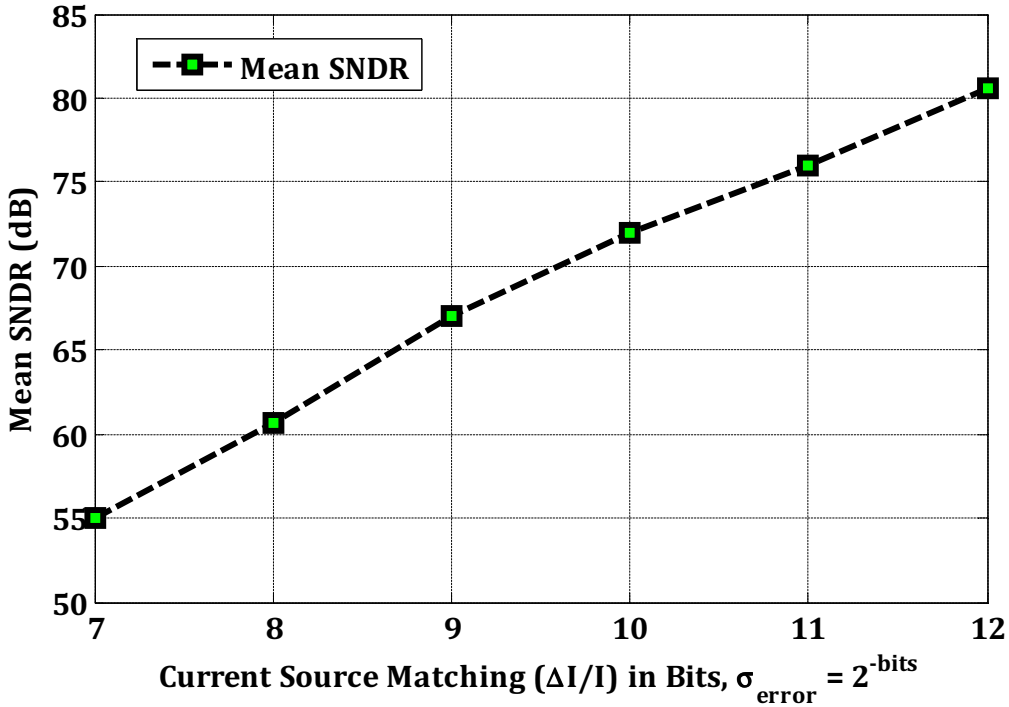

Figure 6.14: Behavioral-level simulation of modulator SNDR versus slow-loop DAC unit element mismatch−for each level of bits, 1,000 trials were simulated.

However, unlike a traditional multi-bit quantizer, in a two-step ADC, there are 6 MSB bits and 7 LSB bits, which are equivalent to a total 31 thermometer-coded bits. Here, due to the DAC segmentation, $1\,MSB = 4\,LSB$ or $I_{MSB,unit} = 4\,I_{LSB,unit}$. Thus, to achieve a linear DAC, six $I_{MSB,unit}$ and seven $I_{LSB,unit}$ current unit elements should match each other within and across the two segments. To match the unit elements themselves, analog calibrated scheme [44, 82] is employed using reference current (i.e., $I_{MSB,unit}$ and $I_{LSB,unit}$, respectively), which will be detailed in circuit-design section. However, due to process variation, generating a precise mirrored reference current, (i.e., $(I_{MSB}) : \left(\frac{I_{MSB}}{4}\right)$) is critical. Thus, it is necessary to understand any mismatch effect between $I_{MSB,unit}$ and $I_{LSB,unit}$ reference current on in-band SNDR,

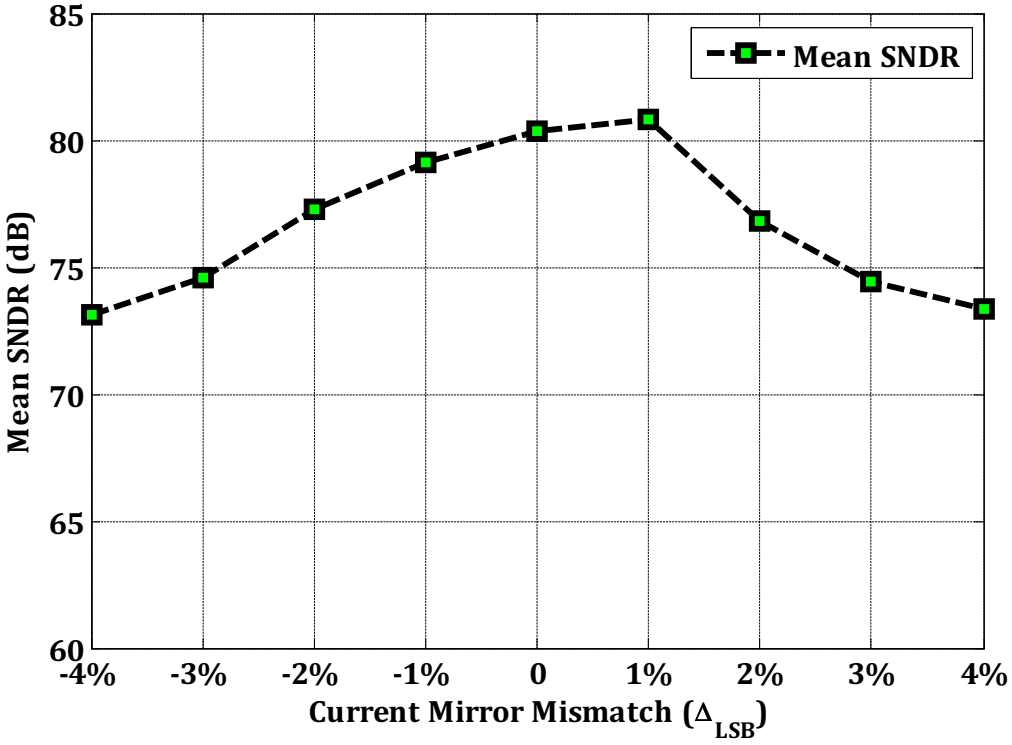

Figure 6.15: Behavioral-level simulation of modulator SNDR for current mirror mismatch factor (i.e.) $(I_{MSB}) : \left(\frac{I_{MSB}}{4} + \triangle I_{LSB}\right)$.

assuming that all the unit current elements are matched among themselves. Figure 6.15 shows that to achieve an in-band SNDR of $> 72\,dB$, the allowed mismatch is $\pm 4\%$ (i.e., $(I_{MSB}) : \left(\frac{I_{MSB}}{4}\right)(1 \pm 0.04)$). In the circuit-level design, this specification will be verified using Monte-Carlo analysis.

6.2.4 System-Level Requirement of Sample and Hold

Figure 6.16 shows the simplified block-diagram of S/H, or fast-loop implemented in the CT-$\triangle\Sigma$ loop to restore the first sample of the open-loop response and to stabilize the $\triangle\Sigma$ loop. The fast-loop comprises the sample-and-hold, and a constant gain, at the summer, seen by the S/H. It is of utmost significance to understand the non-ideal

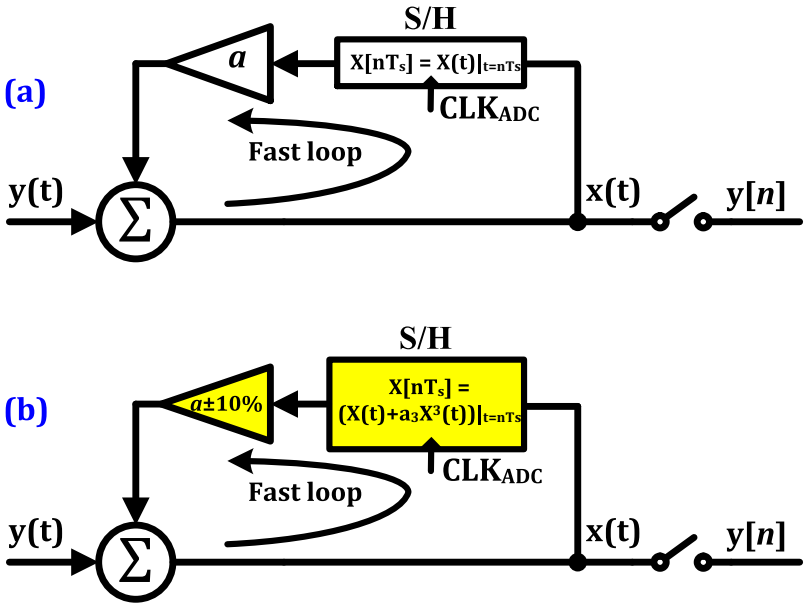

Figure 6.16: Simplified (a) ideal (b) modeled block diagram of fast-loop path.

dynamic effects of the fast-loop path on the overall in-band SNDR of the $\triangle\Sigma$M.

The predominant dynamic non-idealities introduced by S/H are switching noise, charge injection, clock-feed through, and non-linear on-resistance. Similarly, the main non-ideality of the summer is gain variation ($a \pm \triangle a$) due to PVT and circuit-level limitations such as insufficient bandwidth or peaking of the opamp. Generally, these non-ideal dynamic behaviors render the S/H more non-linear and affect its SFDR and THD. But, it is generally assumed that any non-idealities introduced at the same location in the feedback loop as that of the quantization noise, get noise-shaped (or high-pass filtered) and thus tolerated by the loop to a certain extent. However, it is important to determine the maximum allowed HD_3 for the S/H. Similarly, any change in constant gain $'a'$, changes the value of the first sample and alters the resultant $NTF\,(z)$, and thus either affects the in-band SNDR or degrades the $\triangle\Sigma$ loop stability. Thus, it is critical to know the allowable variation ($\pm\triangle a$) in the S/H

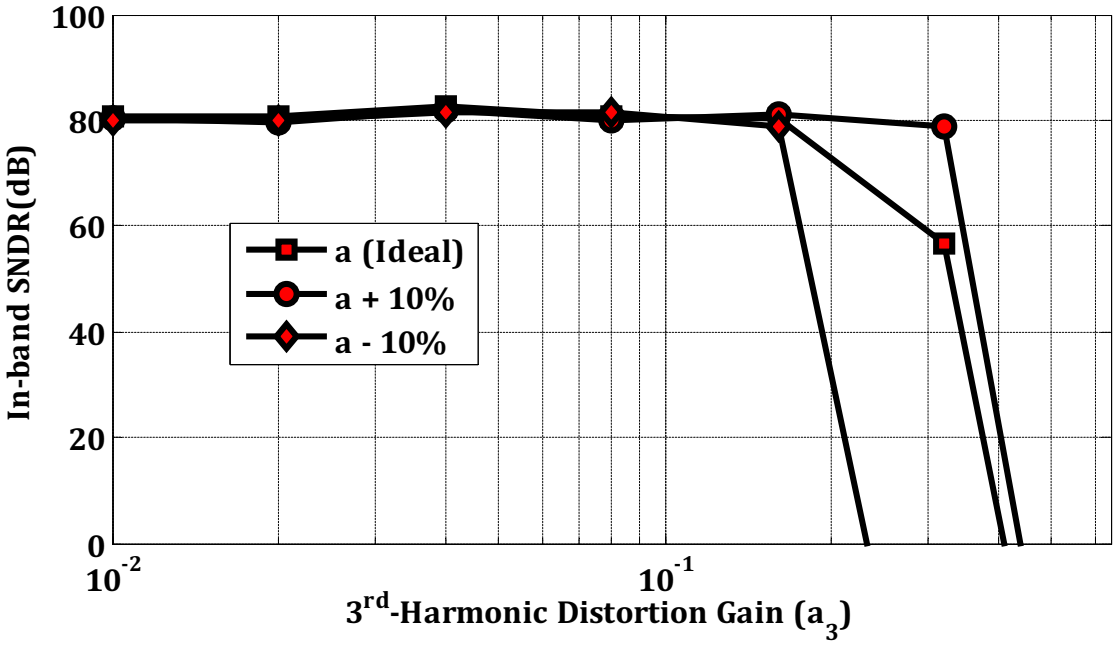

Figure 6.17: Effect of 3^{rd}- order harmonic distortion gain (a_3) of S/H with $\pm 10\%$ variation of constant gain (a) on in-band SNDR.

path gain.

Using the model shown in Figure 6.16(b), the closed-loop simulation is performed for various 3^{rd}-order harmonic distortion gains (a_3) of S/H and a gain variation of $\triangle a = \pm 10\%$. Figure 6.17 shows the results of the SIMULINK simulation that shows that the closed-loop modulator can tolerate a maximum a_3 of 0.16 or corresponding HD_3 of 25 dB from S/H and $\pm 10\%$ variation of constant gain from the summer circuit.

6.3 Circuit Design

In this section, the circuit-level blocks, used in the proposed CT-$\triangle\Sigma$ modulator, implemented in a 0.13 μm CMOS technology, are described.

6.3.1 Loop-Filter Design

Figure 6.18 shows top-level circuit diagram of the CT-$\triangle\Sigma$ modulator, which comprises of a 4^{th}- order feed-forward loop-filter architecture with an additional summing opamp, and a sample-and-hold for the fast-loop. To achieve better overall linearity and a larger signal swing, the active-RC integrators based loop filter is chosen to realize the architecture seen in Figure 6.8. The integrating capacitor, summer feedback resistor, and opamp bias currents are designed to be programmable using digital control bits to tune for the RC time-constants in the presence of process variations, and to control the unity-gain bandwidth of the opamps. Dynamic-range scaling is performed on the state-space representation of the entire loopfilter such that the feed-fordward gains (k_1, k_2, k_3, & k_4) are never greater than 5. This is done primarily to avoid peaking in the adder's closed-loop response for an optimized summing opamp design.

6.3.2 Operational Amplifier

There are five opamps used in the CT loop filter as shown in Figure 6.18, where four opamps are used for four active-RC integrators and one for an active adder. The 1^{st} integrator determines the overall input-referred noise and linearity of the modulator. Therefore, the 1^{st} golden opamp is designed for low input referred noise and a high unity-gain frequency. The opamp topology shown in Figure 4.11 is used in the 1^{st}, 3^{rd}, and 4^{th} active-RC stages with a gradual reduction in the respective bias currents (and thus their power dissipation). The detailed design description of this opamp topology is given in Section 4.3.3. However, the 2^{nd} integrator requires higher output linearity to keep the adder gain less than 5. Thus, a large-output swing

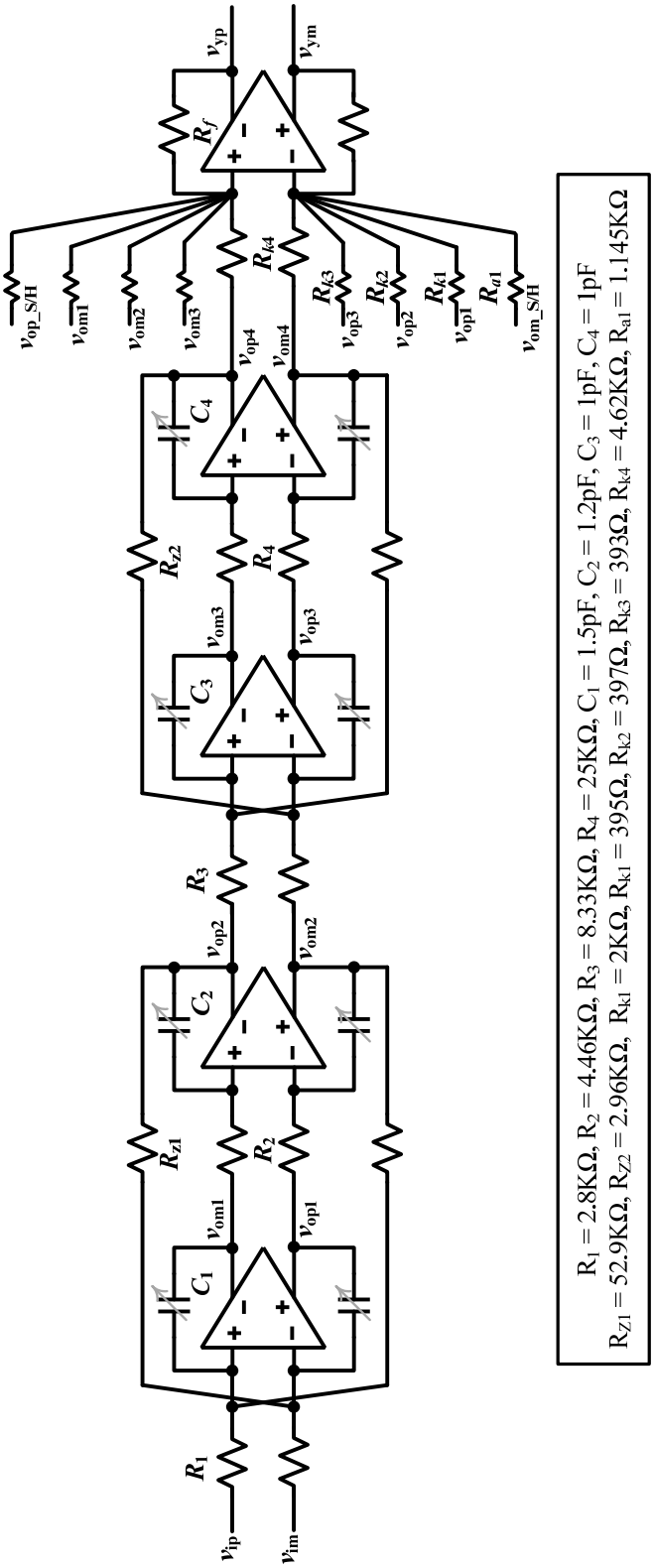

Figure 6.18: Top-level circuit diagram of the multi-bit CT-$\Delta\Sigma$ loop filter.

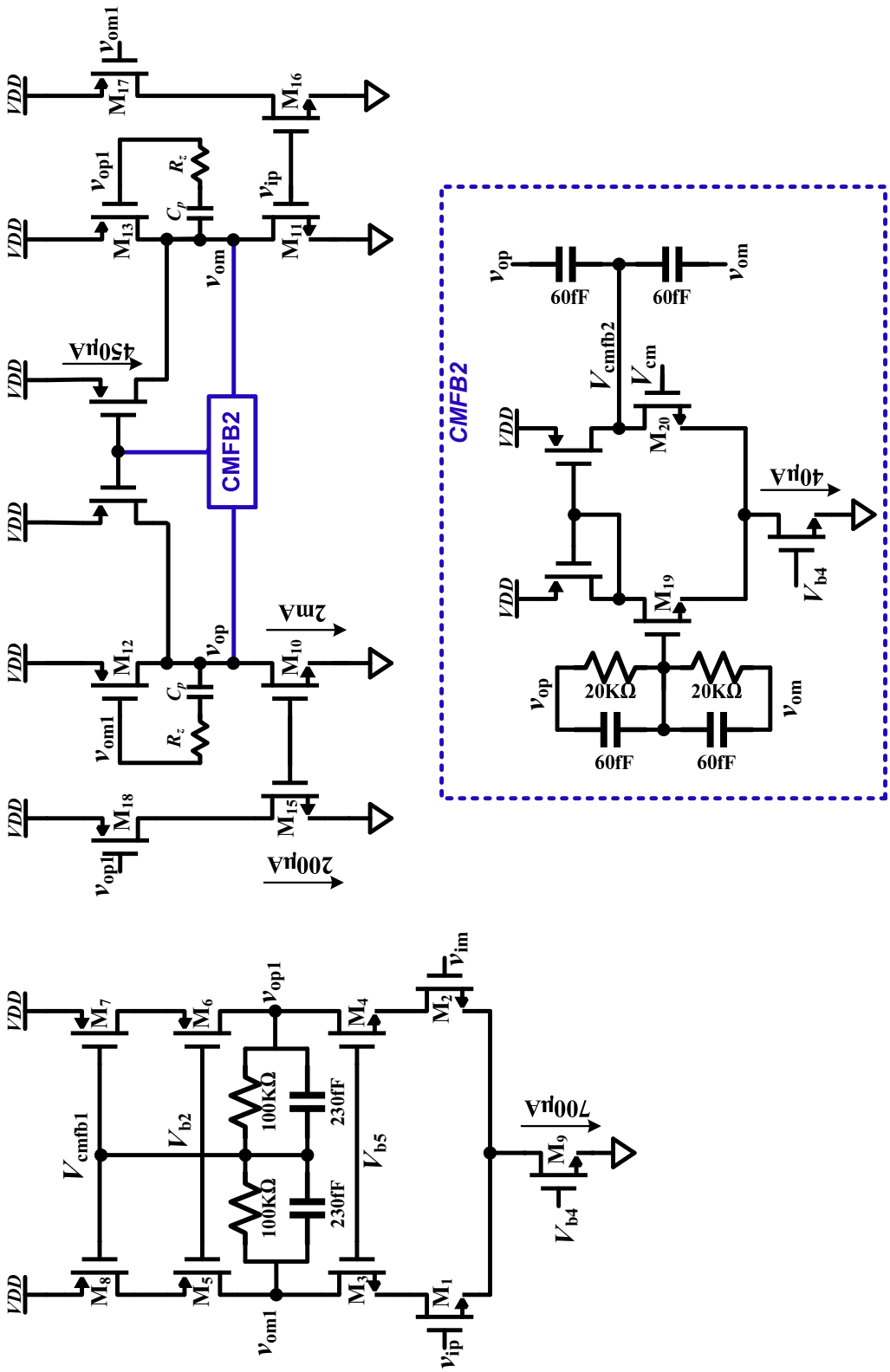

Figure 6.19: The Miller compensated two-stage opamp employed in the adder and subtractor.

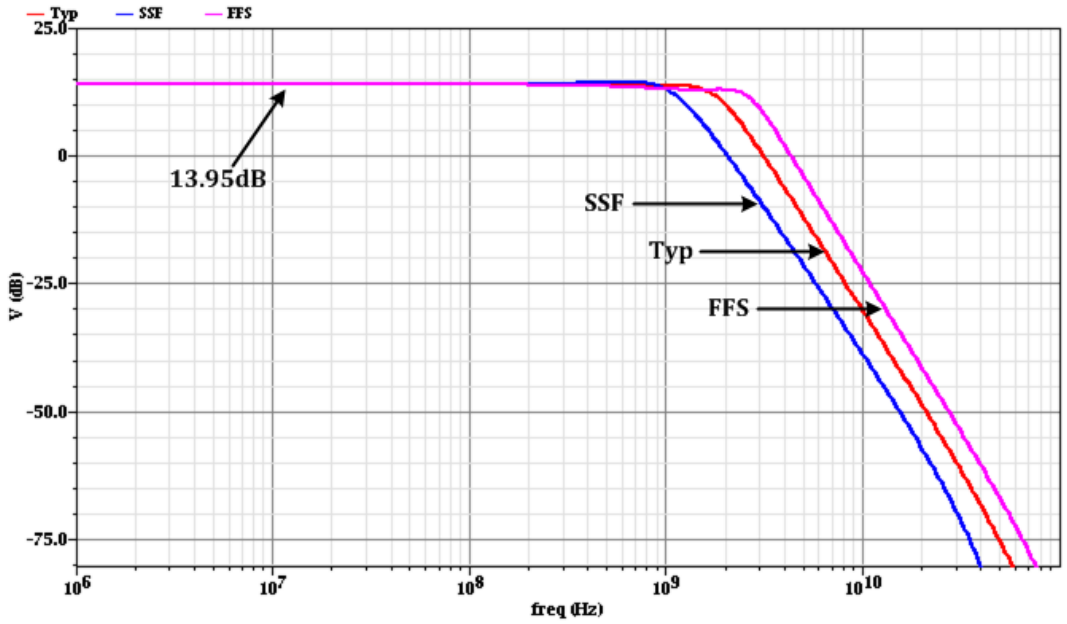

Figure 6.20: Closed-loop AC response of adder opamp when $R_f = 2K\Omega$ and $R_1 = 400\Omega$ in different corners - Typ(0σ), SF (-3σ on FETs and $+3\sigma$ on resistors and capacitors), FFS ($+3\sigma$ on FETs and -3σ on resistors and capacitors).

opamp topology shown in Figure 5.8 is employed in this design. This opamp topology was described earlier in Section 5.3.2.

Figure 6.19 shows the schematic of the Miller compensated two-stage opamps used in the CT loop-filter summation and residue amplifier. This opamp employs a telescopic first stage with a NMOS diff-pair followed by a pseudo class-AB second stage for better output linearity. Instead of using conventional common-mode feedback circuitry as in the previously described opamp topologies from Figure 4.11 and 5.8, a simple local resistive feedback is used to reduce the circuit complexity. The total current drawn by the first stage including the CMFB is $700\,\mu A$. The common-mode feedback resistor of $100\,K\Omega$ in parallel with a capacitor of $230\,fF$ is used. Similarly,

the CMFB circuit for the second stage adds extra current to M_{10} and M_{11} to hold the output node (V_{op} and V_{om}) at V_{CM}. This technique provides good CMFB loop stability and robustness [33]. For robust operation and reduced slewing, the minimum possible values for $C_p = 250\,fF$ and $R_z = 300\,\Omega$ are determined through AC simulations, such that the phase margin of the summation loop never gets below 60°. All the internal CMFB loops are simulated and stabilized using appropriate compensation capacitors. The total current drawn by second stage is $3.5\,mA$. The opamp achieves $66\,dB$ open-loop gain and f_{unity} of $3.5\,GHz$ with 53°phase margin in the SSF corner. The closed-loop bode plot of the adder with a closed loop gain of 5 (i.e., $\frac{R_f}{R_1} = 5$) is shown in Figure 6.20. The adder opamp can achieve $13.95\,dB$, which is $4.98\,\frac{V}{V}$, with bandwidth greater than $1\,GHz$ across the process corners, while driving the input capacitance of the Flash ADC and the sample-and-hold.

6.3.3 Sample-and-Hold Circuit

Figure 6.21 (a) and (b) shows the simplified block diagram and the corresponding schematic of one half of the pseudo S/H circuit used in the fast-loop. From Section 6.2.4, the S/H requires at least HD_3 of $25\,dB$ to avoid the in-band SNDR degradation. However, the output voltage swing needed from the summer opamp is $1.6\,V_{pp,d}$. Thus, to achieve a better linearity from the S/H, the input of the S/H or output of the summer is attenuated by a gain of $\frac{1}{2}$ using a capacitor divider, as shown in Figure 6.21(b). Also, by using a capacitor divider, the signal is AC-coupled and centered at V_{bias3} using R_z. The capacitor value is chosen as $250\,fF$, such that the adder opamp should able to drive the two-step ADC and and $125\,fF$ effective input capacitance from the S/H. Also, to maintain buffer gain close to unity, triple-well NMOS and body-source connected PMOS are used in all the source-follower buffer stages. The

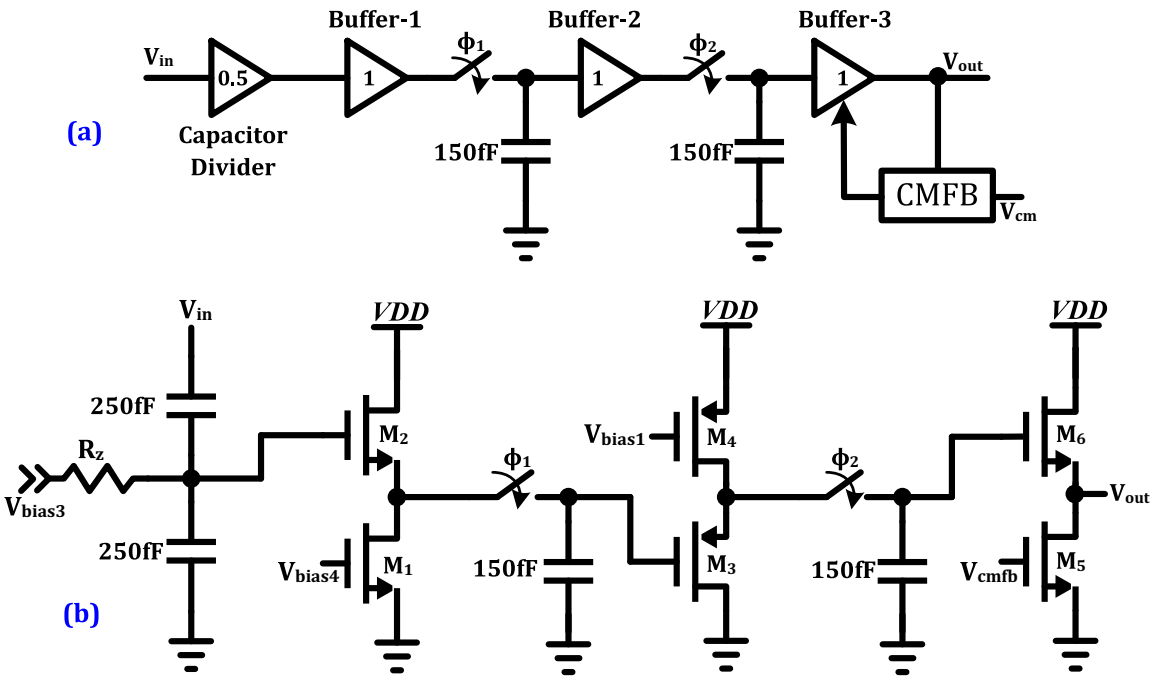

Figure 6.21: Simplified (a) block-diagram (b) schematic of one half of the pseudo-differential sample and hold.

attenuated signal from the 1^{st} stage is further buffered and sampled by two track-and-hold (T/H) stages. The final buffer current source is controlled by a feedback voltage V_{CMFB} to hold the CM of the output at V_{cm}. Also, the last buffer stage is designed in such a way that the output impedance is small, so that it doesn't affect the effective $R_{S/H}$ in Figure 6.18. Any effective gain reduction in the S/H due to the buffer stages can be compensated for by adjusting the gain $'a'$. The total power consumption of the fast path is $3.2\,mW$.

Figure 6.22 shows the simulation results of periodic AC analysis of S/H in different corners. A pseudo S/H can achieve a gain of $-7.98\,dB$ or $0.4\,\frac{V}{V}$ with a minimum bandwidth $650\,MHz$ over different corners. Also, the output signal spectrum of S/H is plotted in Figure 6.23. A pseudo S/H can achieve a HD_3 of $80\,dB$, which is significantly higher than the required system-level specification.

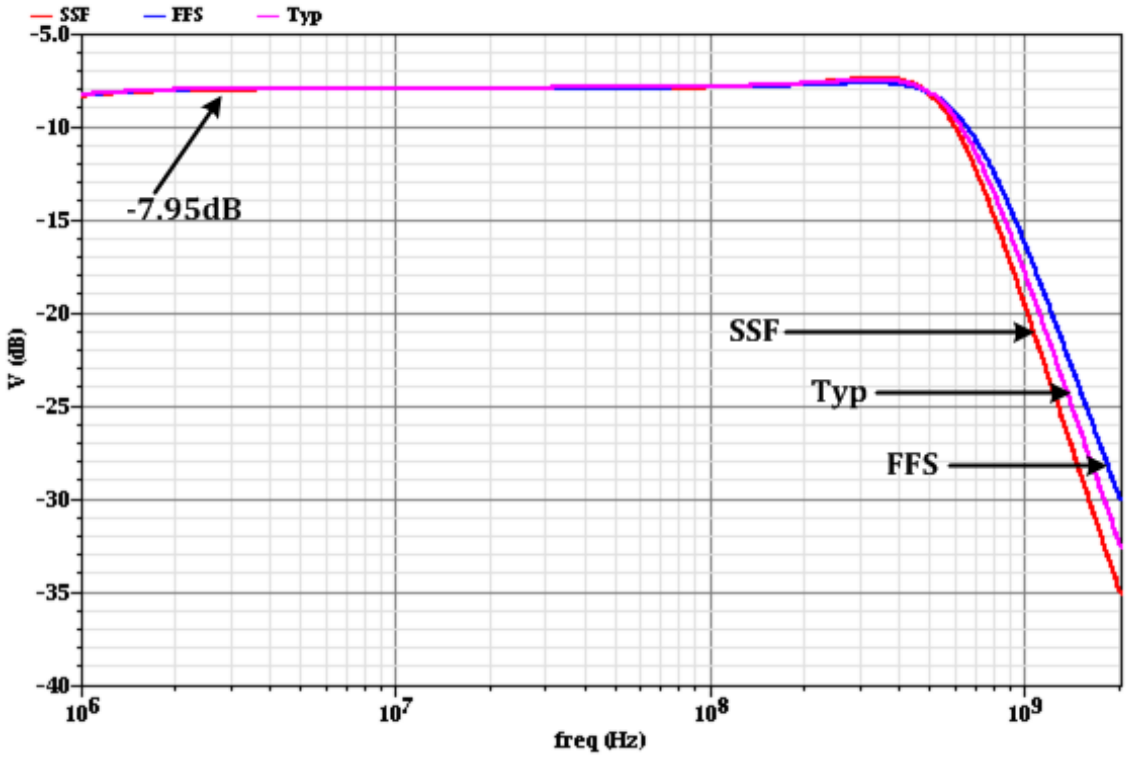

Figure 6.22: Periodic AC analysis on S/H in different corners - Typ(0σ), SF (-3σ on FETs and $+3\sigma$ on resistors and capacitors), FFS ($+3\sigma$ on FETs and -3σ on resistors and capacitors)..

6.3.4 Quantizer Design

Figure 6.24 shows the single-ended representation of the 5-bit two-step flash quantizer system-level schematic [5, 6, 40, 83]. The first stage of the quantizer comprises of 6 comparators to absorb the maximum of $0.5\,LSB$ comparator offsets, and is followed by a 3-bit segmented capacitor DAC. The output of a DAC is directly connected to the switch-capacitor residue amplifier. The residue amplifier drives the 7 comparators in the fine flash stage. V_{refn} and V_{refp} are common high and low reference voltages for the coarse and fine sub-ADC stages. The quantizer full-scale range is set to $1.6\,V_{pp}$, which results in a LSB size of 100 mV in the coarse/fine flash stage. The

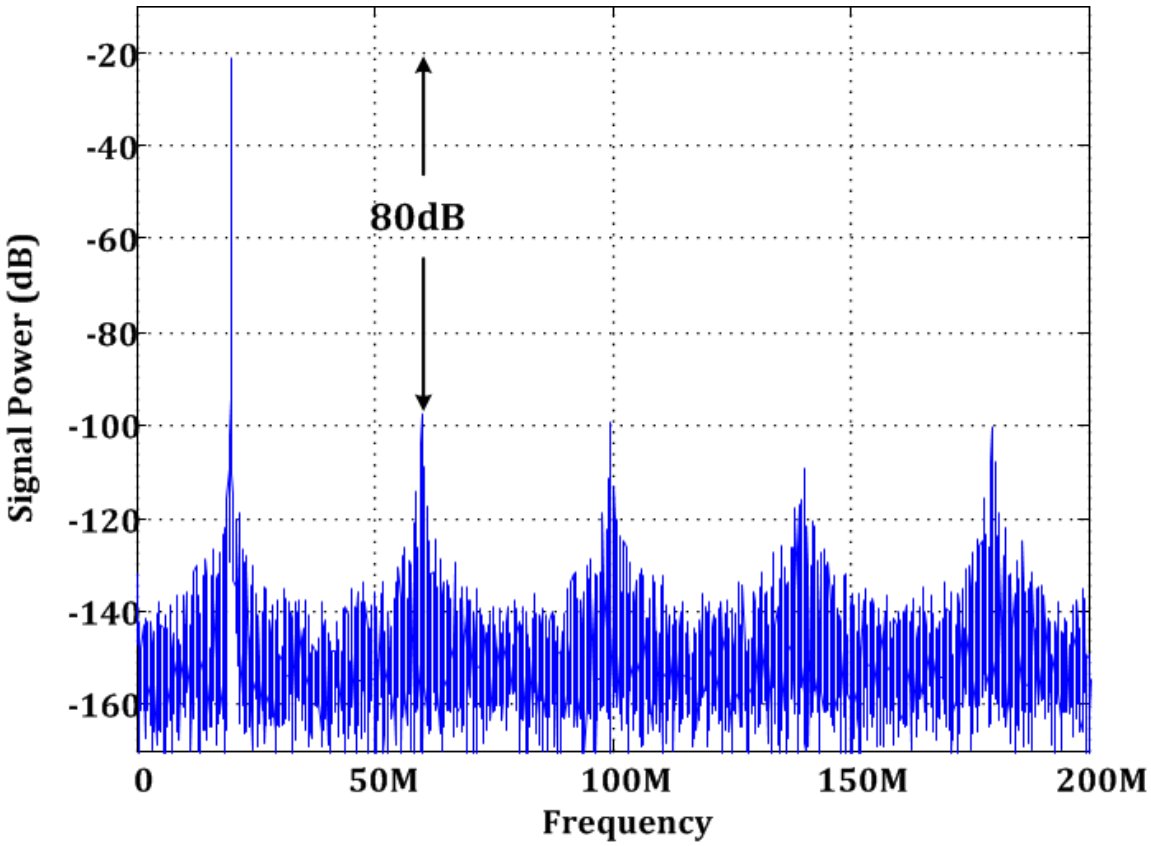

Figure 6.23: Output signal spectrum of S/H.

chosen full-scale range relaxes the random offset requirement on the comparators in the two-step flash ADC. The comparator used for this design is the same as Section 5.3.3.

During the phase ϕ_1, the coarse flash stage estimates the two MSBs of the sampled signal and provides an equivalent thermometer code output. The resultant code drives a highly linear segmented capacitive DAC to decode the signal back to a 3-bit resolution analog signal. Then, during the clock phase ϕ_2, residue V_q is estimated by the residue amplifier with a gain by subtracting V_{dac} from V_{in}. Finally, the fine stage digitizes the residue V_{sub} to encode the three least significant bits of the ADC. Further, during ϕ_1 clock phase, all the capacitors in the circuit are reset or discharged

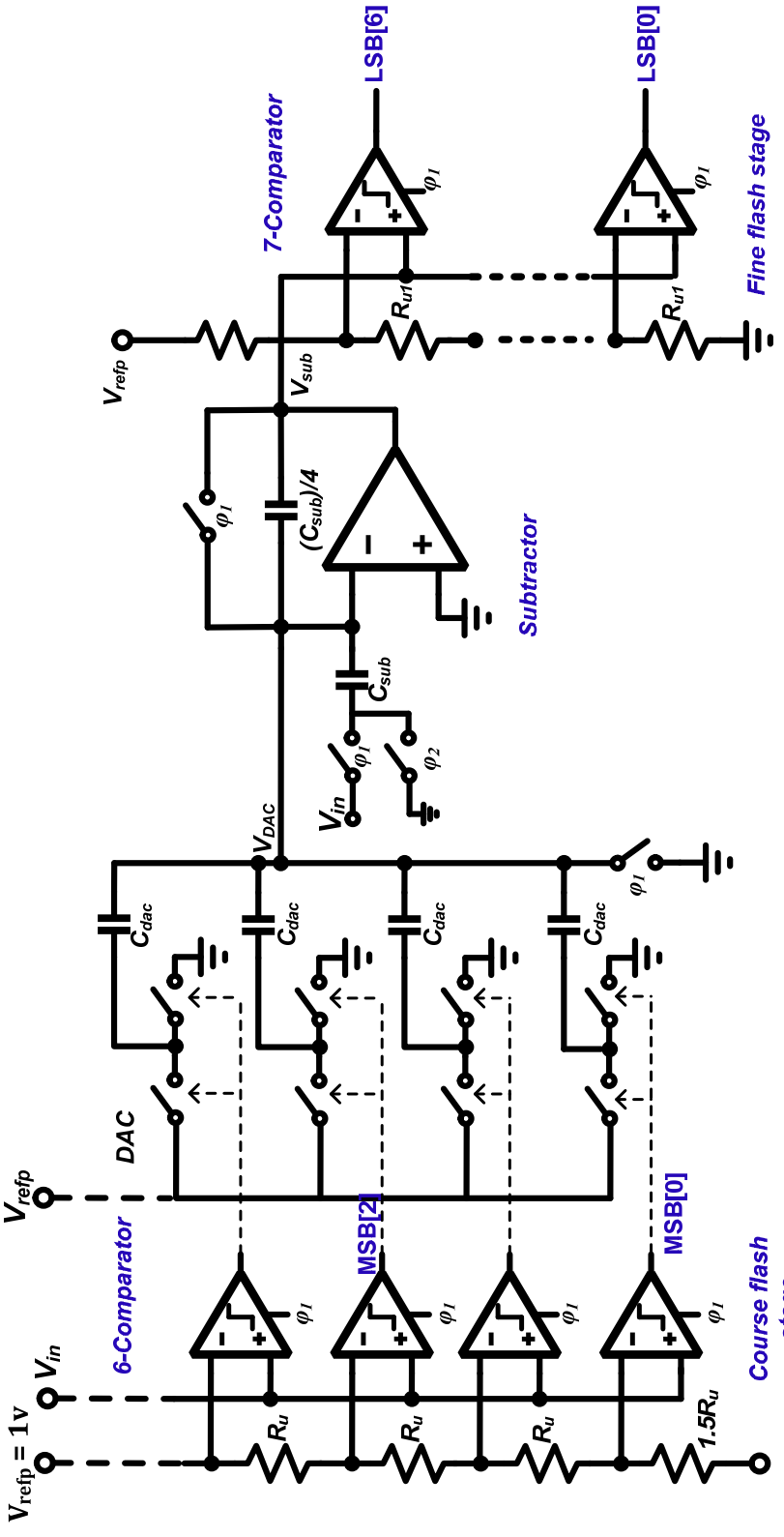

Figure 6.24: Simplified single-ended function diagram of ADC.

to ground. The time delay assigned to the first flash stage, DAC and the Subtractor combined together is $0.8\,T_s$ and, the time delay assigned to the second flash stage and current DAC combined is $0.7\,T_s$. Thus, the net delay introduced by the 5-bit quantizer is less than $1.5\,T_s$.

From Section 6.2.3, it is assumed that to achieve a linear DAC, six $I_{MSB,unit}$ and seven $I_{LSB,unit}$ current unit elements should match each other within and across the two segments and the maximum allowed mismatch between $I_{MSB,unit}$ and $I_{LSB,unit}$ is $\pm 4\%$ (i.e., $(I_{MSB}) : \left(\frac{I_{MSB}}{4}\right)(1 \pm 0.04)$). Figure 6.25 shows the feedback MSB DAC used in the modulator along with a unit current steering cell with calibration circuitry (a similar structure is used for LSB). The DAC unit cell uses fixed current references for supplying 80% of the total unit current, which is $29\,\mu A$ and a tunable current reference is used to provide 20% tunability in the DAC current. A unit DAC cell employs a redundant cell to enable online calibration. While in operation, one of the DAC pairs are selected sequentially and calibrated against reference current cells ($I_{ref,p}$ and $I_{ref,m}$) using an analog-calibration loop as shown in Figure 6.25 [44, 82]. Also, the loop bandwidth is properly stabilized using a miller capacitor.

6.3.5 Interface Circuit

The outputs of the CT-$\triangle\Sigma$M are a $7-bit$ MSB and $6-bit$ LSB thermometer coded signal at a data rate of $400\,MHz$. In order to mitigate the degrading effects of common-mode noise, capacitive coupling and EMI, it is necessary to reduce the data bus width and use a robust I/O interface technique. Thus, an interface circuit, which includes a two $3-bit$ Wallace-Tree thermometer-to-binary circuit [68] (shown in Figure 5.16), a level-shifter (from $1.2\,V$ to $2.5\,V$ IO voltage), and a LVDS driver [84, 85] are employed on-chip, as shown in Figure 6.26.

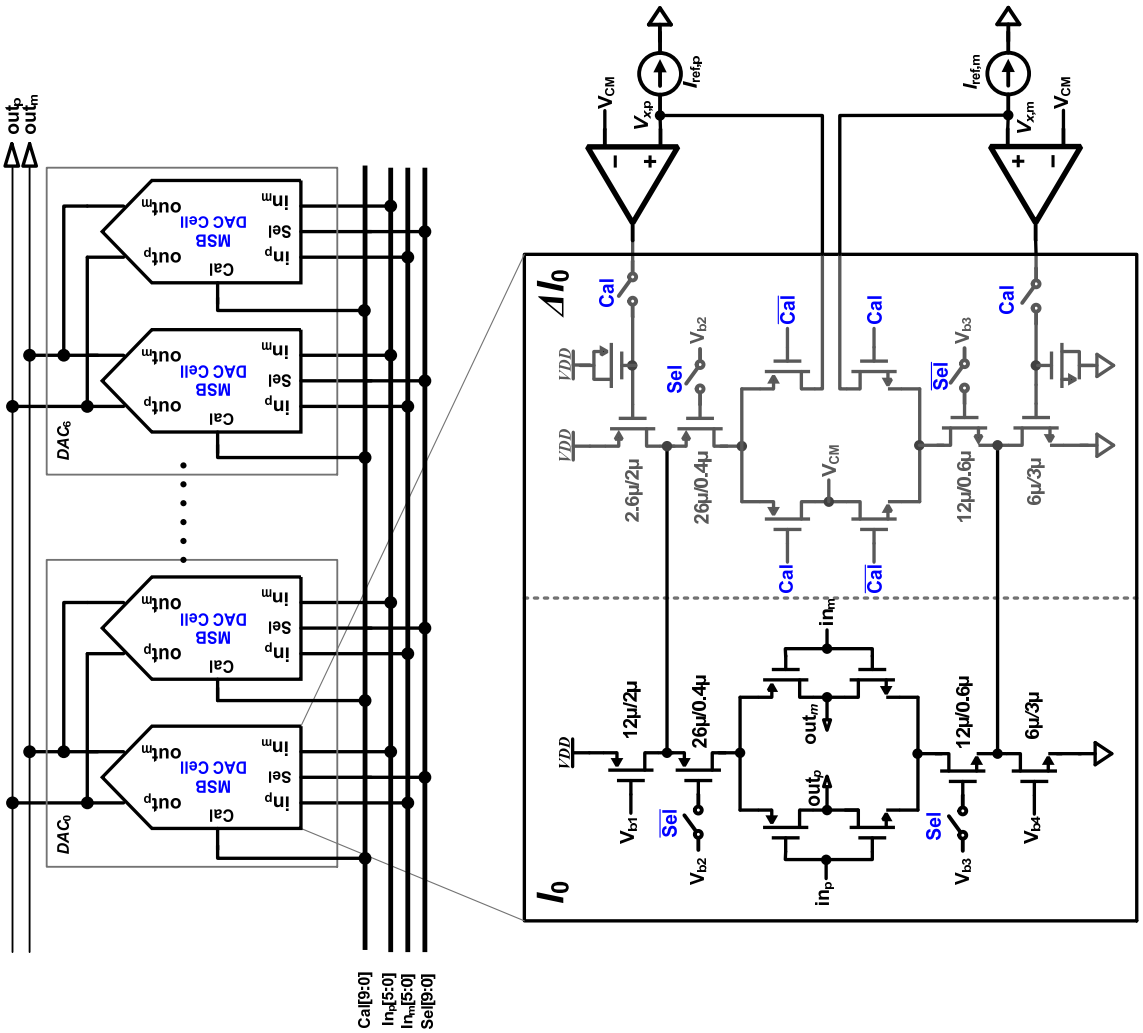

Figure 6.25: Calibration scheme of MSB/LSB current steering DAC. .

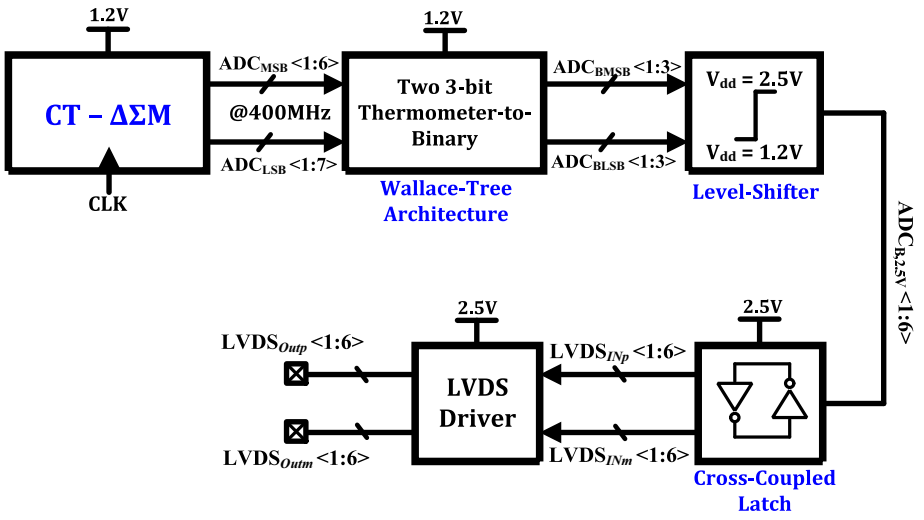

Figure 6.26: Block diagram of the interface circuit.

6.3.5.1 Low-Voltage Differential Signaling

At high-speeds (300 MHz to 1.5 GHz), the dynamic performance of a CMOS interface is primarily limited due to the impact of common-mode noise and crosstalk due to coupling between the single-ended lines in the data bus, which is further exacerbated by the large voltage swing of the transmitted signals. These single-ended data lines, with corruption due to crosstalk, result in degraded measured performance of the $\triangle\Sigma$ modulator. Further, CMOS drivers are not suitable from signal integrity considerations for higher speeds, due to reflection from the mismatch between the PCB traces (transmission lines) and impedance looking into the pad (which in turn includes bond wire inductance). Thus, to reduce crosstalk, common-mode noise, I/O power-consumption and to transcend the transmitted data speed limitations, an LVDS I/O interface is often preferred in high-speed data converters [84, 85].

Figure 6.27 shows the schematic of the LVDS transmitter and receiver used in the high-speed ADC interface. The constant current source/sink is formed by the M_1

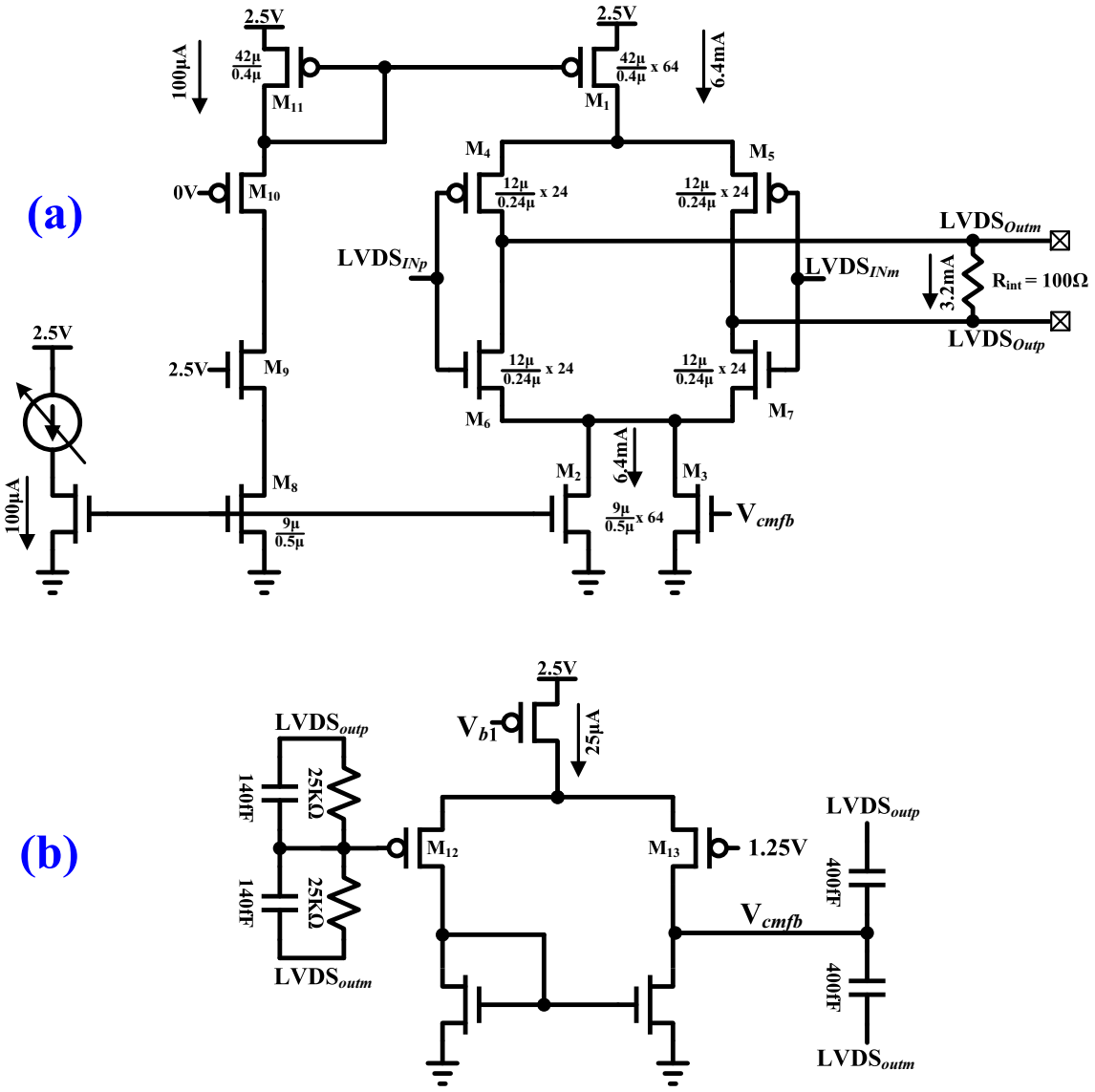

Figure 6.27: LVDS Transmitter (a) Output driver circuit and (b) Common-mode feedback circuit.

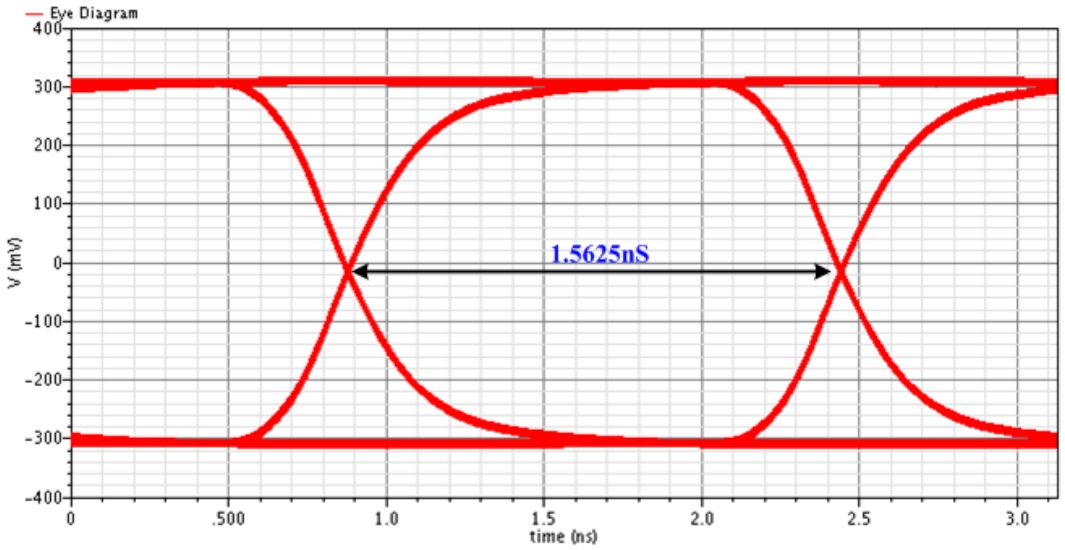

Figure 6.28: Simulated eye diagram of an LVDS buffer driving $C_{bondpad} = 150fF$, $L_{pacakge} = 1.5nH$, $C_{package} = 1pF$, $C_{load} = 5pF$ and modeled PCB transmission line with 100Ω termination.

and M_2 & M_3 transistors, respectively. The current path from current source (M_1) to sink (M_2 & M_3) via the outputs, $LVDS_{Outp}$ and $LVDS_{Outm}$, are dictated by the switches, $M_{4\,to\,7}$, which are controlled by $LVDS_{Inp}$ and $LVDS_{Inm}$. Also, a stable common-mode output voltage is required by the LVDS standards [86]. The IBM $0.13\,\mu m$ CMOS technology offers $2.5\,V$ IO power supply devices, hence the V_{cm} is chosen to be $1.2\,V$, which complies with the LVDS standard [86]. Thus, the fixed common-mode output voltage is set using the common-mode feedback loop.

Figure 6.27(b) shows that the CMFB circuit is used to set the output common-mode voltage where it uses resistors to average the output nodes ($LVDS_{Outp}$ and $LVDS_{Outm}$) and feeds it to the input transistor (M_{12}) and compares it to $V_{cm} = 1.2\,V$ to control the output common-mode feedback voltage (V_{CMFB}). The $140\,fF$ capacitors in parallel with the $25\,K\Omega$ resistor provide a fast high-frequency path,

bypassing the resistive common-mode detector and the error amplifier. The total current drawn by the CMFB circuitry and bias is $125\,\mu A$ from the $2.5\,V$ supply. The current through M_{11} and M_8 is $100\,\mu A$ with $\pm 15\%$ current tuning capability accounting for the process variation. In general, current source output impedance is required to be very high with respect to variable load impedance. But in an LVDS interface, load impedance is set as $100\,\Omega$ at the receiver side. In addition to the receiver termination of $100\,\Omega$, a transmitter termination is also used to minimize loop reflection and to obtain a wide eye opening on the link. The driver stage current is set to $6.4\,mA$ (i.e., half of the total current for the internal termination resistor $100\,\Omega$) and the other half of the current to the receiver termination resistor ($100\,\Omega$). Figure 6.28 shows the simulated eye-diagram of the LVDS buffer driving $C_{bondpad} = 150\,fF$, $L_{package} = 1.5\,nH$, $C_{package} = 1\,pF$, $C_{load} = 5\,pF$, and modeled PCB transmission line with $100\,\Omega$ termination.

6.4 Test Setup and Measurement Results

The fourth-order CT-$\triangle\Sigma$M with a two-step quantizer is designed using the IBM $0.13\,\mu m$ CMOS process as shown in Figure 6.29 and fabrication through *MOSIS*. The test setup for high-speed proposed $\Delta\Sigma$ ADC is the same as for the multi-bit $\Delta\Sigma$ ADC in Chapter 5. Figure 5.18 shows the block diagram of the complete test setup for prototype proposed two-step multi-bit $\Delta\Sigma$ ADC characterization. In order to avoid the coupling and crosstalk between the $6-bit$ data bus/reference output clock pins, the modulator outputs are brought out of the chip using on-chip differential LVDS buffer driver. Using synchronous sampling feature, data were captured using an Agilent 16851A Logic Analyzer. In this work, a $32\,K$ point Blackman-Harris

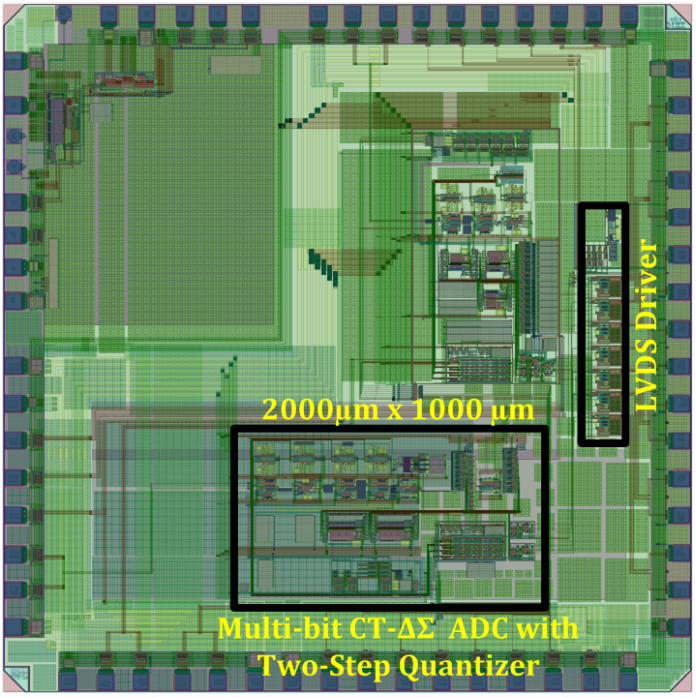

Figure 6.29: Submitted IBM 0.13μm CMOS process prototype layout.

Parameter	Measured Results
Signal Bandwidth/Clock Rate	$20\,MHz/400\,MHz$
Full Scale	$1.6\,V_{pp,diff}$
Input Swing for peak SNR	$-1.93\,dBFS$
Dynamic Range/SNDR	$76\,dB/74\,dB$
Active Area	$2\,mm^2$
Process/Supply Voltage	CMOS 0.13μm IBM
Power Dissipation	$28\,mW$
Figure of Merit	$340\,fJ/level$

Table 6.1: Summary of measured ADC performance.

window is used to evaluate the FFT on the collected data.

Figure 6.30 shows the simulation results of the power spectral density of the modulator output for a $10\,MHz$ input tone for an amplitude that results in the peak SNDR. The measured SNDR of the modulator for a $10\,MHz$ input tone are shown in Figure 6.31. The peak SNR is $66\,dB$. The measured dynamic range of the modulator

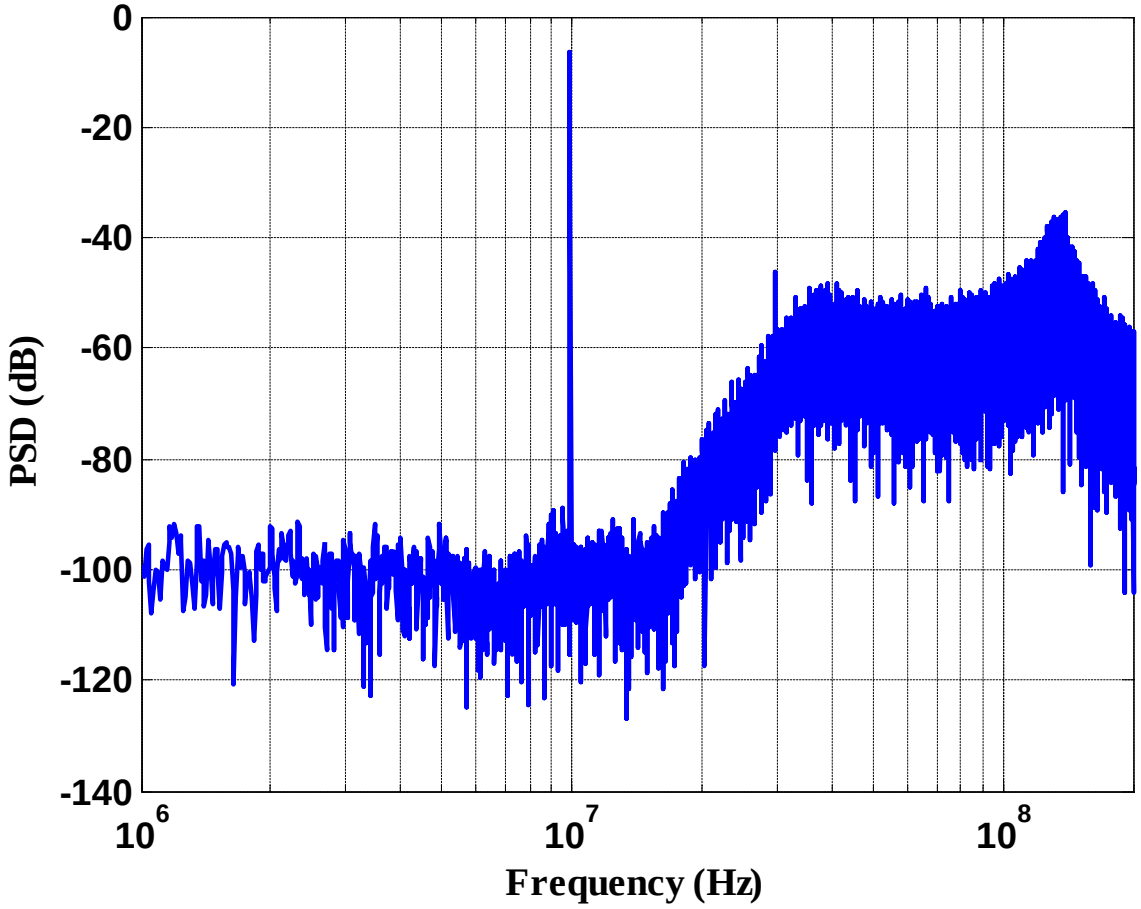

Figure 6.30: PSD for a $-2\,dBFS$ tone @ $10\,MHz$.

is $69\,dB$. The maximum stable amplitude was about $-2\,dBFS$. A summary of simulation performance of CT-$\triangle\Sigma$M with two-step quantizer is provided in Table 6.1. From Table 6.1, the designed modulator achieves a dynamic range of $690\,dB$ in $20\,MHz$ bandwidth while consuming only $28\,mW$ from the $1.2\,V$ power supply. The FoM for the designed modulator is $340\,fJ/level$. A summary of measured performance is given in Table 6.1. Also, Table 6.2 compares the performance of our design with that of state-of-the-art multi-bit high speed $\Delta\Sigma$ modulators in 130/180 nm CMOS process. The comparison shows that the proposed topology exhibits comparable

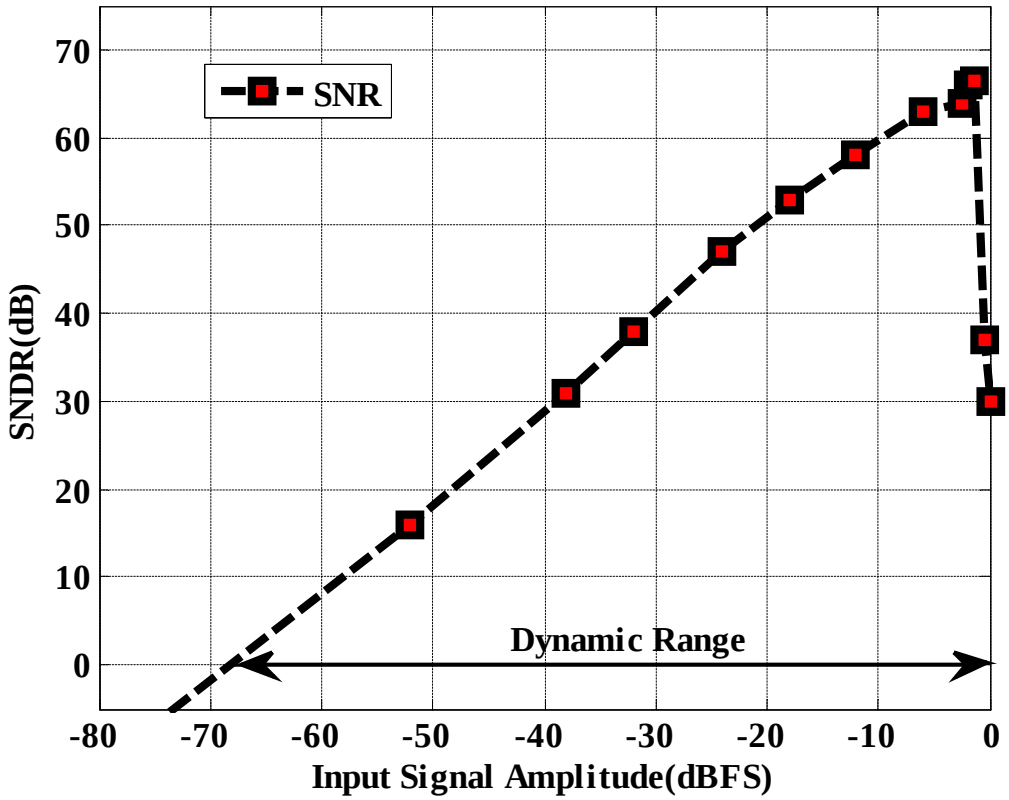

Figure 6.31: Measured SNDR - the dynamic range is $69\,dB$.

performance to the state-of-the-art designs in similar technology nodes and with the same conversion bandwidths. Since, the overarching goal of this dissertation was to demonstrate the feasibility of novel hybrid architectures with further architectural optimizations in a 64 nm CMOS or smaller technology, the proposed architecture can potentially achieve an FoM smaller than $75\,fJ/level$ with low-OSR setting.

6.5 Summary

A wideband CT-$\triangle\Sigma$M using a two-step quantizer is proposed and designed in a $0.13\,\mu m$ CMOS technology. The proposed modulator achieves a high dynamic range

Reference	Feature Size (nm)	f_s(MHz)	BW (MHz)	SNR/DR (dB)	Power (mW)	FOM (fJ/level)
[17]	130	640	20	76.0/80.0	20	97
[33]	180	300	15	67.2/70.0	20.7	368
[44]	180	800	32	57.0/64.0	47.6	152
[51]	130	900	20	81.2/80.0	87.0	231
[74]	130	950	10	86.0/90.0	40.0	122
This work	130	400	20	66.0/69.0	28	340

Table 6.2: Comparison with other $\Delta\Sigma$ modulators.

with very wide conversion bandwidth using a 5-bit two-step quantizer at very low sampling frequency. The excess loop-delay due to the two-step conversion process was successfully compensated using a fast loop around the quantizer. The CT loop-filter coefficients are systematically computed by incorporating the opamp non-idealities. The comprehensive transistor-level simulation results of the proposed CT-$\triangle\Sigma$M exhibit a peak SNR of $66\,dB$, a dynamic range of $69\,dB$ with a MSA of $-2\,dBFS$. Further, the system-level behavioral simulation is presented, to analyze the overall CT-$\triangle\Sigma$M performance degradation of quantizer non-idealities such as the offset and gain error in the two-step sub-ADC, and the current mismatch between the MSB and LSB elements in the feedback DAC. The demonstrated hybrid modulator concept paves the path for the development of CT-$\triangle\Sigma$ ADCs incorporating multi-step and pipelined quantizers. This technique could also be applied to direct-conversion bandpass CT-$\triangle\Sigma$ modulator where a high resolution quantizer could be used to achieve performance gains.

CHAPTER 7

CONCLUSION

7.1 Summary

In this dissertation, the following topics associated with the wideband continuous-time $\triangle\Sigma$ modulator were studied in detail:

- The traditional high-speed single-bit and multi-bit CT-$\triangle\Sigma$ ADC designs and their performance limitations due to circuit-level non-idealities.

- An ultra-low power 3^{rd}-order CT-$\Delta\Sigma$ modulator sampling at $1.25\,GS/s$ (highest speed in $0.13\,\mu m$ CMOS technology) was designed, fabricated and tested. The results from a test chip fabricated in a IBM $0.13\,\mu m$ CMOS technology shows that the modulator achieves $60\,dB$ dynamic range in a $15.6\,MHz$ bandwidth. The designed modulator consumes only $3.5\,mW$ and achieves a FoM of $154\,fJ/level$.

- A multi-bit CT-$\triangle\Sigma$ modulator is designed, fabricated and tested at speed comparable to state-of-the-art designs. The ADC has a measured dynamic range of $66\,B$ while dissipating $14\,mW$ from a $1.2\,V$ supply, achieving the energy consumption of $380\,fJ/level$ in a signal bandwidth of $20\,MHz$.

- A novel hybrid architecture employing two-step quantization is proposed to meet the ever increasing conversion bandwidth and performance requirements

from next-generation wireless standards. The CT loop-filter coefficients are systematically computed by incorporating the opamp and quantizer non-idealities. The complete limitations of two-step quantizer and its non-idealities such as the offset and gain error in the sub-ADCs, and the current mismatch between the MSB and LSB elements in the feedback DAC are analyzed and discussed with system-level simulations. The proposed architecture is demonstrated in IBM $0.13\,\mu m$ CMOS technology using a high-speed, wideband 4^{th}-order CT-$\triangle\Sigma$ modulator employing a $5-bit$ two-step quantizer with significantly reduced hardware complexity. The excess loop-delay due to the two-step conversion process was successfully compensated using a fast-loop around the quantizer. The proposed modulator exhibits a peak SNDR of $74\,dB$, a dynamic range of $76\,dB$ with FOM of $170\,fJ/level$.

7.2 Future Work

To improve the performance of this work (e.g., to increase the bandwidth further while keeping the sampling frequency and power consumption the same), several architectural developments and circuit techniques need to be considered:

- The successfully demonstrated concept paves the path for inclusion of higher resolution multi-step conversion or pipelined ADCs in low-pass as well as bandpass CT-$\triangle\Sigma$ ADCs.

- This technique could also be applied to direct-conversion bandpass CT-$\triangle\Sigma$ modulator where a high resolution quantizer could be used to achieve performance gains.

- Extend the Hybrid CT-$\triangle\Sigma$ ADC architecture to include pipelined and folding sub-ADCs
- Exploit noise-shaping of input-referred errors introduced by the two-step quantizer
- Residue amplifier can be optimized for low-power by using CT current-mode subtraction
- Time-domain (VCO-based) two-step quantizer for low-power implementation

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