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Communication

Simulation Modelling of Silicon Gated Field Emitter Based Electronic Circuits

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Abstract: Vacuum transistors (VTs) are promising candidates in electronics due to their fast response and ability to function in harsh environments. In this study, several oscillator and logic gate circuit simulations using VTs are demonstrated. Silicon-gated field emitter arrays (Si-GFEAs) with 1000 × 1000 arrays were used experimentally to create a VT model. First, transfer and output characteristics sweeps were measured, and based on those data, an LTspice vacuum transistor (VT) model was developed. Then, the model was used to develop Wein and Ring oscillator circuits. The circuits were analytically simulated using LTspice, where the collector bias voltage was 200 V DC, and the gate bias voltage was 30–40 V DC. The Wein oscillator circuit produced a frequency of 102 kHz with a magnitude of 26 Vpp. The Ring oscillator produced a frequency of 1.14 MHz with a magnitude of 4 Vpp. Furthermore, two logic circuits, NOR and NAND gates, were also demonstrated using LTspice modeling. These simulation results illustrate the feasibility of integrating VTs into functional integrated circuits and provide a design approach for future on-chip vacuum transistors applied in logic or radio-frequency (RF) devices.

Keywords: field emitter arrays; vacuum transistors; oscillator circuits; logic circuits

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1. Introduction

As one of the primary vital elements in electronics, vacuum electron devices have a crucial history in several areas of applications, such as communications, radars, medical, aerospace, and electronic warfare [1–4]. However, with the development of modern-day electronics, there is a requirement for a new generation of micro- and nanoscale vacuum electron device development, which can be easily integrated, has good reliability, and has substantial efficiency [5]. Currently, nano- and microscale vacuum channel devices are being fabricated to realize new generations of vacuum transistors (VT) with high-frequency response [6]. VT devices have proven to be insusceptible to high temperatures (400 °C) [7] and ionizing radiation (1 krad proton and 100 krad g radiation) [8,9]. A planar nanoscale vacuum channel transistor (NVCT) with a dimension that can be compared with a modern-day field effect transistor was demonstrated recently [10]. In these structures, electron transport takes place using quantum tunneling [11], where drift-diffusion is the primary mode of electron transportation in traditional semiconductors [12]. Recent work also suggested that these devices can be operated at a voltage as low as 15 V [13]. Also, scattering or collision loss is negligible thanks to the short vacuum channel length, which is a few hundred nm [12]. These virtues make these VTs a perfect candidate for harsh environment electronics [9]. Additionally, in the optimization of materials for electrodes such as metal and/or graphene or other low-dimensional materials, VTs are an important candidate for on-chip vacuum electron devices that can be easily integrated into circuits [14]. The reported work [3,15] shows the research interests for VTs [16].

To realize functional circuits, it is required to develop a simulation model to inspect VTs in terms of functional circuits such as oscillators [17] and high-speed logic gates [18]. In this study, the circuit modeling software LTspice XVII v17.0 was used to create an electronic model of VTs [9,18]. We also explore the possibilities of executing active circuits like oscillators and logic circuits such as NOR and NAND gates using multiple VTs. We directly employ the device characteristics from the experimental data to the device simulation module. The results presented in this work incorporate simulation models with an emphasis on functional circuit development, thus providing a crucial foundation for the subsequent development of on-chip nano- or microscale vacuum electron devices.

2. I-V Characterization Experiment

To establish a simulation model, I-V characterization experiments were carried out using a 1000 × 1000 silicon-gated field emitter array (Si-GFEAs) [14]. The gap between each tip is 1 μm, and the total number of tips are 1 million. These GFEAs include self-aligned polysilicon gates (gate aperture ≈ 300 nm), and each tip is supported by silicon nanowires at the bottom, which have a diameter of 150 nm and a height of 10 μm. These nanowires act as ballast resistors. Detailed fabrication methods and device descriptions can be found elsewhere [6]. The 1000 × 1000 arrays were able to produce a current density greater than 100 A/cm^2 [14], which made these a clear choice for the experiments. I–V characterization experiments were executed in a high vacuum environment created in a stainless-steel test chamber. The high vacuum chamber is fitted with electrical feedthroughs and a three-axis manipulator probe arm, which was used to connect to the gate pads of the GFEAs. A Keysight B2902A source measurement unit was used to carry out the experiments. Elaborated test chamber setup and experimental details can be found in our previous works [7,19].

Figure 1 shows the experimental schematic structure. For the output characteristics, the V_C was swept from 0 to 200 V, and for the transfer characteristics, the V_G was swept from 0 to 40 V. For all the tests, V_E was kept at the ground. The results were used to develop an appropriate VT model, and the details can be found in our previous work [17], where we developed, simulated, and experimentally validated a 152 kHz Colpitts oscillator. This validation provides confidence in our circuit design.

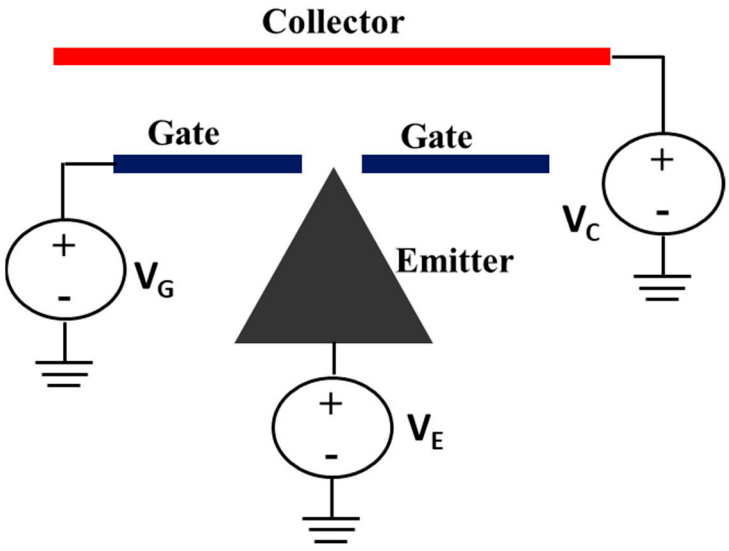

Figure 1. Experimental schematic model showing emitter (E), gate (G), and collector (C).

Figure 2a shows the transfer characteristics comparison data of experiment and model for a collector voltage of 200 V, and Figure 2b shows the output characteristics of experiment and LTspice model for a fixed gate voltage of 30 V. From Figure 2a, it can be observed that the device turns on at a gate voltage of approximately $V_{G,\,ON}$ = 24 V and reaches > 0.225 mA

of current at V_G = 30 V. From Figure 2a, it can be observed that experiment and model agree well. Figure 2a (inset) shows the Fowler–Nordheim (F–N) [11] plot for the gate sweep of 0 to 30 V. From Figure 2b, it can clearly be observed that the data of the experiment and model results match well. Please note that, for the model development, a gate voltage of 40 V was used, and the details can be found in our previous work [17].

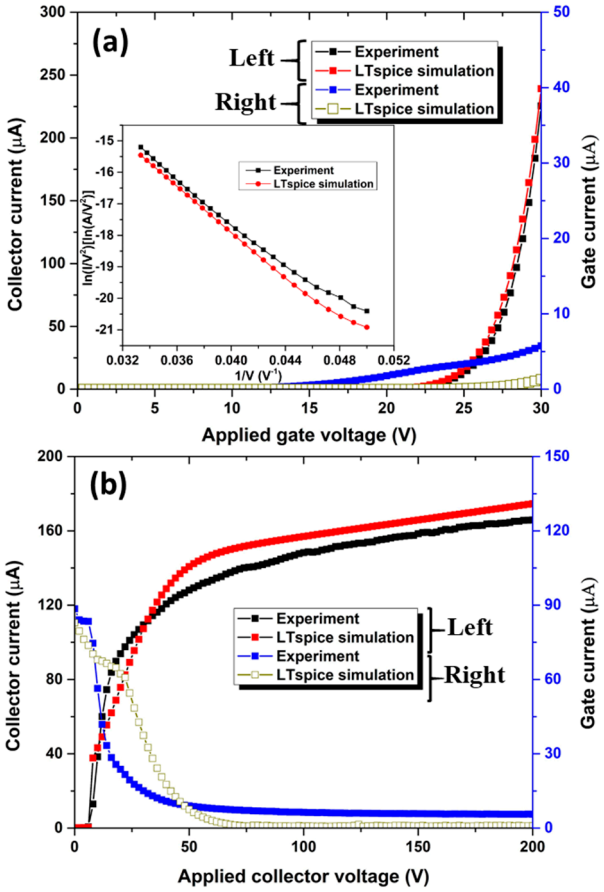

Figure 2. (**a**) Transfer characterization comparison between experiment and LTspice model (inset is the F-N plot) and gate current comparison. (**b**) Show the output characteristics and gate current comparison between experiment and model. Axis are marked with "Left" and "Right".

3. Simulation Model

The Fowler–Nordheim (F–N) model was used to establish the VT model [11,20–22]. The F–N equation is given as

$$I = a_{FN} V_G{}^2 exp\left(-\frac{b_{FN}}{V_G}\right) \quad (1)$$

Here, V_G is applied gate potential in V, a_{FN} and b_{FN} are F-N coefficients and are defined as follows:

$$ln\left(\frac{I}{V_G{}^2}\right) = ln(a_{FN}) - \frac{b_{FN}}{V_G} \quad (2)$$

$$b_{FN} = \frac{0.95 \cdot 6.83 \times 10^7 \cdot \varphi^{\frac{3}{2}}}{\beta} \quad (3)$$

where φ is the emitter work function (eV), and β is the field enhancement factor. Here, the work function is assumed to be 4.05 eV for Si. Further, to predict the model accurately, a hyperbolic tangent or tanh function was incorporated [17].

The model provides [17]

$$I_{C,Model} = I_{E,Model} \cdot \mathbf{0.5} \cdot \left(\mathbf{1} + \tanh\left(\frac{(V_C - d)}{e}\right)\right) \quad (4)$$

where the parameters d and e (two sets of coefficients for tanh) are dependent on V_G. I_C is = collector current (A), and I_E is = emitter current (A). A detailed model development method can be found in our previous work [17].

Figure 3 shows the circuit diagram and the temporal response characteristics of a VT-based Wien oscillator circuit. The Wien oscillator [23,24] is based on a frequency-selective form of the Wheatstone bridge circuit [25]. The Wien Bridge Oscillator is a two-stage RC coupled amplifier circuit that has good stability at its resonant frequency and low distortion. The Wien Bridge Oscillator uses a feedback circuit consisting of a series RC circuit connected with a parallel RC of the same component values, producing a phase delay or phase advance circuit depending upon the frequency. Figure 3a shows the Wien oscillator circuit along with the values of the passive components, where V1 = 250 V and V_{BIAS} = 37 V. Figure 3b shows the temporal response of the Wein oscillator simulation circuit. The observed oscillation frequency is ≈102 kHz with a V_{PP} of ≈26 V. The circuit includes four VTs. Among the four VTs, the rightmost one is used as a load for the simulation.

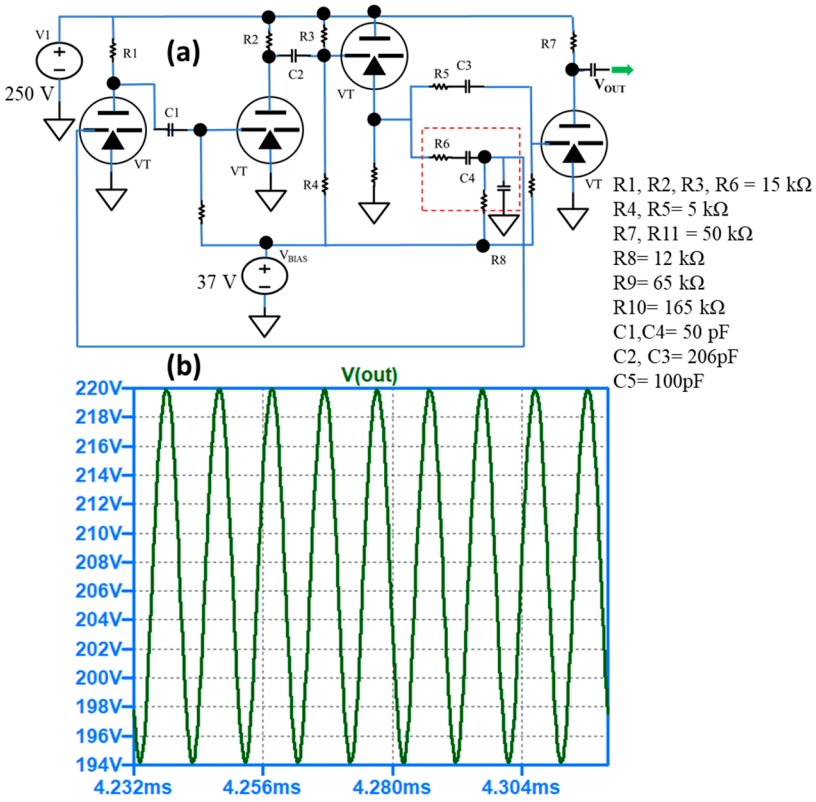

Figure 3. (**a**) LTspice model of three-device Wien oscillator circuit plus output buffer (rightmost VT) and (**b**) output waveform.

Figure 4 shows the schematic and temporal response characteristics of the VT-based Ring oscillator circuit. The Ring oscillator [26] is a combination of inverters connected in series with a feedback connection. The output of the final stage is again connected to the initial stage of the oscillator. The values for the passive components that can be seen in Figure 4a,b show the temporal response of the Ring oscillator simulation circuit. The circuit is comprised of three VTs and passive components (resistors and capacitors). The applied V_1 = 350 V and V_{BIAS} = 38 V. Observed oscillation frequency is ≈ 1.12 MHz with a V_{PP} of

≈ 4.5 V. The V_{PP} of this Ring oscillator circuit could be limited by the RC delay caused by the device capacitance [17] and biasing resistors.

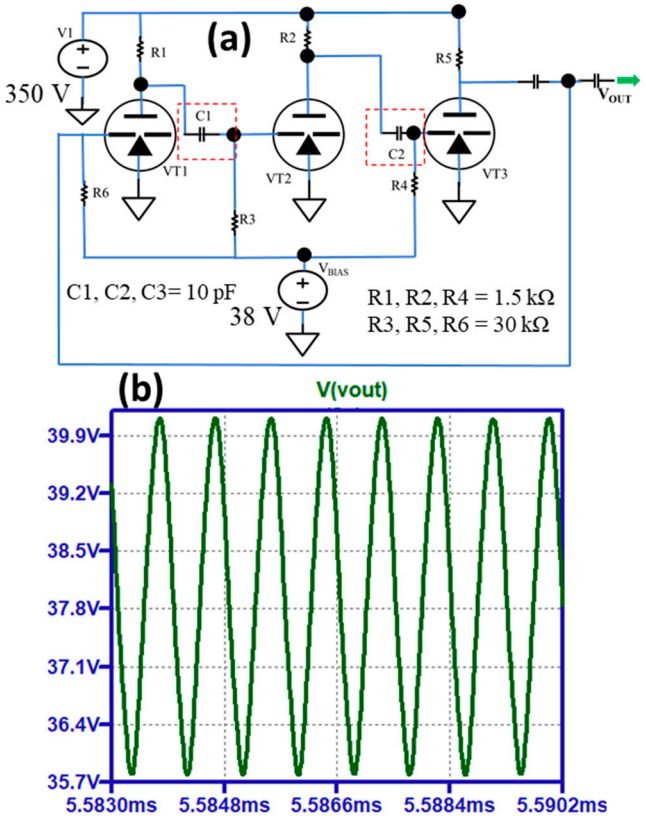

Figure 4. (**a**) LTspice model of a three VT device Ring oscillator simulation circuit and (**b**) the simulated output waveform.

A simple NOR gate [27] can be constructed using resistor–transistor logic (RTL) switches connected together with the inputs connected directly to the transistor gates. The logic NOR gate's output becomes "HIGH" only when both of its inputs are at "LOW" states, and for the rest of the states, the output will be in the "LOW" level state. A simple 2-input NOR gate was designed and simulated in LTspice using the VT model. Figure 5a shows the circuit where the inputs are connected directly to the transistor gates.

Both transistors must be cut off ("OFF") for an output. Figure 5b shows the output waveform. The circuit is comprised of three VTs and passive components (resistors). From the output, it can clearly be seen that when both the inputs are low or "false", the output is high or "true" and the output is low or "false" for all other cases, which clearly denotes the NOR operation. Here, the low-state voltage does not go to "0". However, we can still achieve the NOR operation using the high or low output.

A simple NAND gate [27,28] can be constructed using resistor–transistor logic (RTL) switches connected together with the inputs connected directly to the transistor gates. The core logic is a NOR gate formed by U1 and U2 and converted to a NAND gate through DeMorgan's Theorem [29], with the input inverters formed by U3 and U4 and an output inverter formed by U5. Figure 6a shows the circuit diagram, and Figure 6b shows the output waveform. The device is comprised of six VTs and passive components (resistors). From the output waveform, it can clearly be seen that the output is low only when both inputs are high. Otherwise, the output is always high, which clearly denotes a NAND gate operation. However, similar to the NOR gate, the "low" state does not go to "0" V. The NAND operation can still be achieved by setting the "low" and "high" threshold limits.

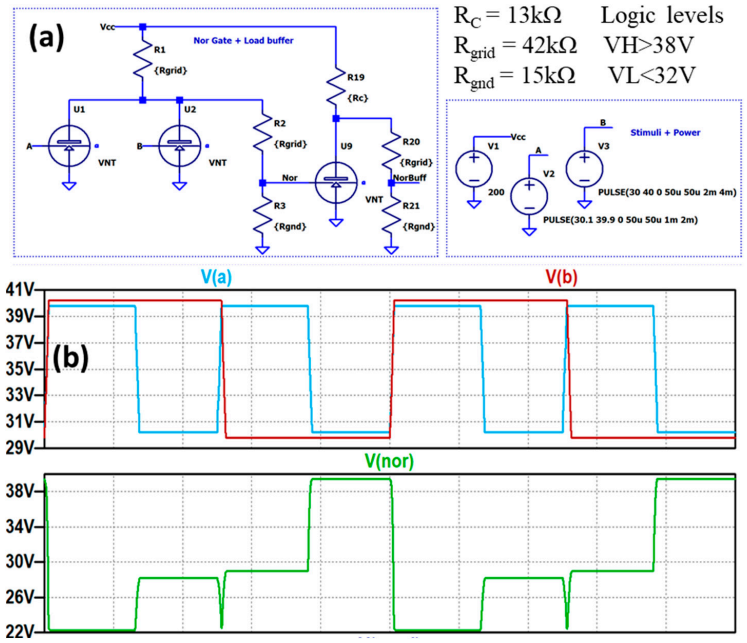

Figure 5. (**a**) Two-device NOR gate plus simulated load. (**b**) Output of the NOR gate. The output is high when both the inputs are low, and the output is low for all the other cases.

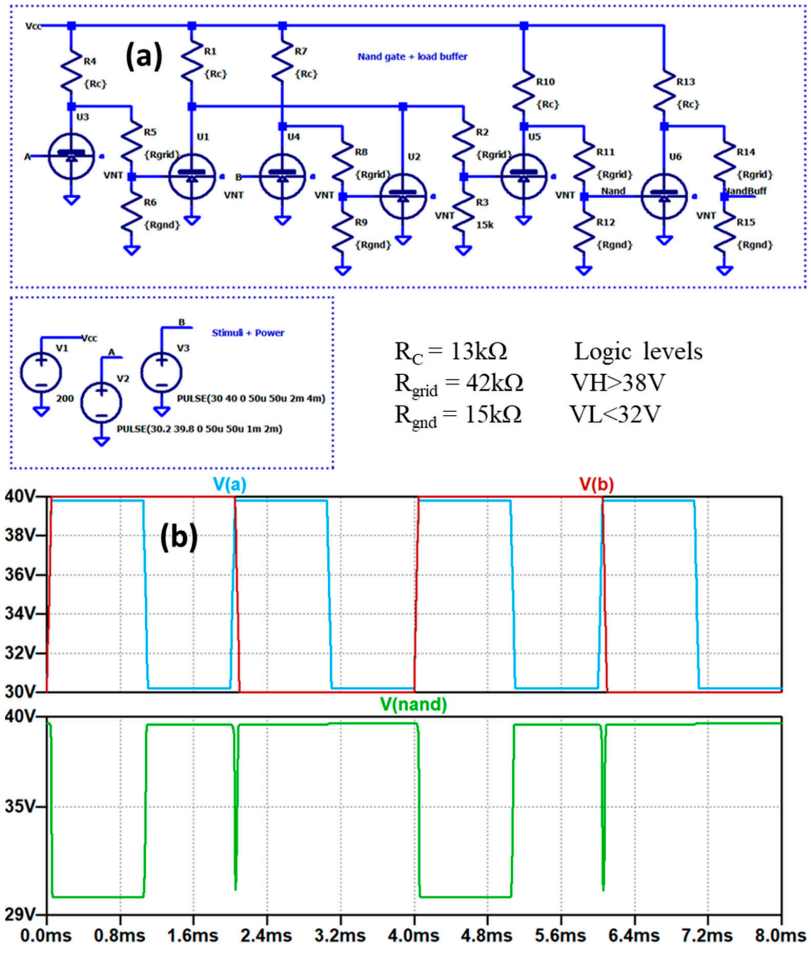

Figure 6. (**a**) Five-device NAND gate plus simulated load. (**b**) Output of the NAND gate. The output is low only when both the inputs are high; otherwise, the output is always high.

4. Conclusions

In summary, this study explores the modeling of a variety of VT-based circuits. In addition, and more importantly, we successfully simulated several oscillator and logic circuit designs based on an optimal VT. To the best of our knowledge, it is the first demonstration of a vacuum-state oscillator in the circuit simulation module in which the VT functions as a conventional triode or field-effect transistor (FET). Several circuits, a Wein oscillator, a Ring oscillator, a NOR gate, and a NAND circuit, were designed and demonstrated using LTspice simulations. The low-frequency Wein oscillator circuit has an oscillation frequency of 102 kHz with an amplitude of 26 V_{pp}. The Ring oscillator model showed a comparatively higher oscillation frequency of 1.14 MHz with a magnitude of 4 $V_{pp.}$ These oscillators and logic circuits could be used as low-frequency harsh environment temperature, pressure, and vibration sensors in nuclear reactors, satellites, and spacecraft. Future work includes the experimental validation of these circuits.

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