Temperature Effects on Gated Silicon Field Emission Array Performance

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ABSTRACT

Silicon field emitter arrays (Si FEAs) are being explored as an electron source for vacuum channel transistors for high temperature electronics. Arrays of 1000 × 1000 silicon tip based gated field emitters were studied by measuring their electrical characteristics up to 40 V of DC gate bias with a 1.3 mA emission current at different temperatures from 25 to 400 °C. At ∼350 °C, residual gas analyzer measurements show that water desorption and carbon dioxide partial pressures increase significantly, the gate to emitter leakage current decreases by more than ten times, and the collector current increases by more than ten times. These improvements remained after heat-treatment but were then lost once the device was exposed to the atmosphere for several days. The improvements could be recovered upon additional baking suggesting that adsorbates (primarily water) on the surface affected field emission and surface leakage. It was also found that after heat-treatment, the electrical characteristics of the devices exhibited <3% variation in collector current at 40 V, which (without exposure to the atmosphere) can be termed as a weak temperature dependence. These results suggest that Si FEAs could be viable as a high temperature transistor.

I. INTRODUCTION

An alternative to semiconductor devices, especially in harsh environment electronics, includes vacuum transistors1–3 that are capable of operating at high temperature and in high radiation environments.4 Transistors comprised of nanoscale vacuum channels, also known as the nanogap transistor, have been steadily gaining interest. Distinct from the early vacuum tubes,5 which had high-power consumption and were physically large, the nanogap structures with field emitters6–8 offer an alternative for modern nanoelectronics to be used for satellites, nuclear reactors, etc. Field emitters, which operate in vacuum, have several inherent advantages over semiconductors. Intrinsically, electrons could ballistically travel through the nanoscale vacuum nanodevices and could combine the advantages of ballistic transport with miniaturization and integration. Also, because the field emission mechanism9 is based on electron tunnelling into vacuum, it is inherently radiation hard like the thermionic filaments and temperature independent like the thermionic vacuum devices before it. With additional technological maturation, these vacuum transistors should have the advantages of vacuum electronics with the footprint of solid-state devices and could be a considerable device for future applications. The mechanism of field emission has been demonstrated with multiple materials: carbon nanotubes,11 graphene,12,13 molybdenum Spindt arrays,14 silicon,6,15 and diamond,16 and the concept of a nanovacuum channel transistor (NVCT)6 is not new. However, renewed interest in the device is emerging due to improved fabrication techniques17 to make nanoscale devices that can have a similar size and level of integration as modern day silicon circuits and potentially could have a similar voltage of operation. Among them, field emitters made out of silicon nanowires15 have shown encouraging possibilities.

As a result, several attempts have been made to scale the vacuum channel into nanogap, three terminal devices. As an example, the vertical structure18 was utilized in a recent vacuum nanochannel transistor.19 Researchers have proposed different types of vertical NVCTs, where the electrons could emit directly out of the plane, e.g., the slit-type20 vacuum transistor or the Spindt-type14 NVCT. However, the effects of adsorbed gas on
dielectric and emission surfaces must be studied to determine what effects such gases would have on device performance. In addition, the performance of the devices at high temperature must also be studied to understand the dependence of emission on temperature.

In this work, Si based gated field emission arrays (GFEAs)\(^{6,17,21,22}\) have been tested as a function of temperature to understand the relevance of the emitter and dielectric surface conditions\(^{23}\) on performance. First, the experimental setup and test configuration will be presented followed by results from array testing at elevated temperature.\(^{24,25}\) The results will be discussed in terms of gas desorption.

II. EXPERIMENTAL DETAILS

The field emitter arrays were fabricated on single crystal, n-type, 150 mm silicon wafers. Array sizes ranged from a single emitter to 1000 × 1000 emitters. Field emitter arrays have a 1 \(\mu\)m spacing between each emitter. These arrays consist of bare silicon nanowires with a 200 nm diameter and a 10 \(\mu\)m height with sharp tips on top. The complete emitters have annular polysilicon gate apertures \(\approx 350\) nm in diameter. Si nanowires are filled-in with a dielectric stack consisting of silicon dioxide and silicon nitride. Gate contact is made of Ni/Ti/Au, and metallization is carried out using a lift-off technique. A detailed fabrication method is described elsewhere.\(^{21}\) The tip radius distribution is log-normal with a mean of 5.6 nm and a standard deviation of 1.3 nm. Among those arrays, the 1000 × 1000 array is capable of producing a current density greater than 100 A/cm\(^2\) with a demonstrated lifetime greater than 100 h.\(^{17}\) \(I-V\) characterization measurements were carried out inside a stainless steel vacuum chamber. The chamber is equipped with electrical feedthroughs, thermocouple feedthroughs, a three-axis manipulator probe arm, and an Extorr Inc. XT100 residual gas analyzer (RGA). A turbomolecular pump backed by a roughing pump was used to maintain high vacuum \((<10^{-6} \text{Torr})\) inside the chamber. The pressure was monitored using an ionization gauge. A test setup was developed for these experiments to allow probing of the devices on a heated chuck.

As shown in Fig. 1, the test setup consists of a substrate test jig with a heater cartridge, a multi-axis probe arm containing an emitter gate probe pin and a collector rod, and the test wafer section (die). The substrate holder test jig consists of a low temperature cofired ceramic (LTCC)\(^{26}\) bottom plate, a molybdenum heating block, and an LTCC top plate for electrical isolation. The top LTCC block has a top ground plane for the backside connection of the silicon wafer section under test. The LTCC material has been tested for outgassing and has been pumped to \(5 \times 10^{-9} \text{Torr}\) in prior experiments. The silicon emitter tips are electrically connected through the wafer backside. Kapton coated metal wire connects to the LTCC ground plane and the probe structure. A stainless steel, low resistance heater cartridge is placed inside the molybdenum heating block as the heating source. The wafer test section is electrically isolated on the LTCC substrate.

The heater block also sits on an LTCC isolator to inhibit thermal conduction to the support platform and chamber. Two J-type thermocouple probes were used to measure the temperature on the heater cartridge and the die. For the room temperature experiments, the pressure was below \(7.5 \times 10^{-9} \text{Torr}\). However, for the high temperature experiments (350 °C), pressure increased to \(2 \times 10^{-6} \text{Torr}\), and the residual gas desorption was measured by an RGA.

A molybdenum pin and a stainless steel rod, mounted on the manipulator probe arm, were used as the gate connector and emission current collector, respectively. Because the collector and probe are on the same arm, it is not possible to independently control the collector to emitter gap. The collector is \(\approx 2-4\) mm above the emitter array. A Keysight B2902A source measure unit (SMU) was used as for the source voltage and to measure the gate and collector currents. The SMU has a ±210 V range, can source current up to 10 A, and can measure current with a resolution <10 pA. The gate connection is made by adjusting the manipulator while viewing through a microscope to set down on the gate electrical pad. A photograph of a wafer section under test is shown in Fig. 2. In the...
magnified view, it can be seen that the probe is attached to the gate pad.

For high temperature experiments, it was necessary to calibrate the heater chuck, to measure the actual device temperatures, and to determine the temperature ramp up time. To measure the heater cartridge temperature, a J-type thermocouple sensor built inside the cartridge was connected to the controller unit outside the chamber using a thermocouple vacuum feedthrough. A thermocouple probe wire (J-type) was also placed on the surface of a test die for calibration. The second measurement method used an

FIG. 3. (a) Reproducible $I$–$V$ characteristics of 1000 × 1000 array and (b) corresponding $F$–$N$ plot of collector current. (c) Comparison of collector and gate current with large gate current observed due to surface leakage.

FIG. 4. (a) Collector current $I$–$V$ characteristics for different temperatures. Collector current enhancement occurs at high temperature (400 °C). (b) $I$–$V$ measurements of the gate current for different temperatures.
infrared (IR) camera (FLIR A310) and a ZnSe IR transparent window. The IR camera was used to view the die through the ZnSe window at a slight angle. It was determined that 200 min was required to get to a stabilized temperature of 400 °C on the die surface with the heater temperature at 455 °C. These temperatures were confirmed using the IR camera. The emissivity correction of the IR camera is calibrated for the emissivity of the ceramic surface, and the IR camera is then used to measure the temperature on the surface of silicon wafer without the need for the in-contact thermocouple connection.

III. EXPERIMENTAL RESULTS

The experimental procedure begins with evacuation of the chamber to a base pressure of ≈7.5 × 10^{-8} Torr. Nitrogen (N2) purging was always used to reduce water vapor and other gas adsorption during chamber vent. Room temperature I–V measurements are then performed as well as RGA measurements. The heater chuck temperature is then increased up to the testing temperature in steps, and I–V and RGA measurements are carried out at each temperature. The heating test fixture is isolated from the chamber, and a ceramic insulator at the bottom of the chamber is used to avoid heating of other chamber parts. The chamber walls are not baked. For the first few tests, I–V characteristics were carried out at room temperature to determine preheat-treatment characteristics. Figure 3(a) shows the I–V characteristics for the device with 1000 × 1000 tips. The collector voltage was fixed at 100 V DC, and the gate was swept up to 40 V DC with a step size of 50 mV and a sweep time of 5 min. The sweep voltage was kept below 40 V to avoid overheating of the collector. Several measurements were carried out to ensure that the characteristics were repeatable. From the measurement, it is clear that the field emission current is extremely repeatable. However, from the I–V characteristics [Fig. 3(c)], it can be seen that there is large gate current compared to collector current. Tests with a close collector...
(0.2–1 mm) show a far lower gate current. This large gate current is partially the result of the large gap between the collector and the array resulting in field emission current collecting on the gate; however, some part of this current is the result of dielectric leakage or surface leakage from adsorbates on the insulator between the emitter silicon and the gate as will be discussed. To confirm the surface leakage, a reverse DC bias was applied to the gate, and it was observed that the gate leakage current was approximately symmetric about the origin from −20 to 20 V indicating surface leakage. Fowler–Nordheim (F–N) emission is primarily dependent on work function and the field factor (β). In general, an F–N plot is linear when the emission from the tip is due to tunneling through the surface barrier. For these devices, field emission occurs above 20 V, and Fig. 3(b) shows the roughly linear nature of the collector current in the form of an F–N plot indicating field emission.

The maximum collector current observed in the 1000 × 1000 array for a gate voltage of 40 V is not the result of current limitation of the emitter die. As has already been shown in Fig. 3(c), gate current also increased to almost 60 times the observed collector current. Thus, the low collector current is a result of emitted electron collection on the gate due to an insufficient collector field, large gate surface leakage, adsorbates on the emitter, or a combination of all of these. The gate current from the emitted electrons could be mitigated by increasing the voltage on the collector or by bringing the collector physically closer to the surface of the emitter as described here.

Experiments at high temperature were carried out to study the effects of gas adsorbates on the gate leakage and the emission current and to study the performance of emitters at high temperature. The molybdenum block, shown in Fig. 1, was heated to 400 °C in steps with I–V measurements at 50, 100, 200, 300, and 400 °C. Figure 4(a) shows the I–V curves (collector current) at each temperature including at 25 °C both before and after baking. As seen in the plot, the I–V curves are consistent until 400 °C at which point the collector current increases (more than ten times) such that the preheat-treatment room temperature collector current was ≈80 μA, and at 400 °C, the collector current was ≈1.3 mA.

After cooling the structure back down to room temperature, the increased collector current is sustained as indicated at 25 °C (after). It is not clear why the shape of the collector I–V curves is not the same at 400 and 25 °C (after), but the peak current is the same at 40 V with a difference of <3%.

The emitter to gate leakage current also greatly decreases from ≈4.8 mA to ≈460 μA (more than ten times) as observed in Fig. 4(b). Here, the I–V characteristics for the gate current are shown for a series of high temperature measurements. Once again, at 400 °C, a change in the current is observed, and this change remains when the device is cooled back down to 25 °C.

These experiments were repeated for three additional arrays. To confirm that this reduction was related to surface leakage, the reverse bias experiment was performed again, and it was observed that the leakage current under reverse bias was also greatly reduced (more than ten times) compared to preheat-treatment condition.

The collector current changes can be attributed to desorption of water vapor and possibly other adsorbates at high temperature. The adsorbates increase the emitter surface work function, thereby decreasing emission current from the tips, which is a well-known phenomenon. The surfaces along the walls between the emitters and the gate are also covered with adsorbates, which may enhance electron transport along the surface and increase gate leakage. To see the effects of the vacuum heat-treatment on field emission more clearly, Fig. 5 shows the F–N collector current plot before heat-treatment and after heat-treatment. The field emission characteristics are far less linear preheat-treatment but show a much straighter F–N plot after heat-treatment indicating a much cleaner surface. While the fraction of emitter tips that are emitting increases with increasing voltage, the shapes of the preheat-treatment and postheat-treatment F–N plots indicate that either the surface of already emitting tips has reduced work function or that additional tips have been cleaned by heat-treatment allowing those emitters to contribute additional current.

Partial pressure outgassing measurements were performed using an RGA to study the desorption versus temperature. The I–V measurements and pressure measurements required a 20 min dwell time at each temperature, but it is understood that longer dwell time at each temperature, but it is understood that longer dwell
times would affect outgassing and also passive heating of the chamber wall. Figure 6(a) shows a bar chart of the partial pressure in the chamber over the entire temperature range with smaller temperature increment steps between 300 and 400 °C.

The water partial pressure and then carbon dioxide partial pressure increase above 300 °C with the peak at 350 °C. Additional I–V characterization measurements were also carried out from 300 to 400 °C with a step value of 10 °C to clearly observe the gate and collector current transition phenomena.

At 350 °C, denoted by a dashed line, the gate and collector current transitions took place as seen in Fig. 6(b). The correlation of the transition with water vapor and carbon dioxide outgassing are very clear.

This result clearly demonstrates that water vapor desorption reduces the gate surface leakage and increases field emission from the tips, which can clearly be seen in Fig. 6. Note that a data point after heat-treatment at 25 °C is also shown at the right of the plots, denoted by a dashed vertical line. It is important to observe that the improved collector current at 400 °C is ≈1.3 mA, while after cooling down, the room temperature collector current observed is ≈1.27 mA, which clearly demonstrates a weak temperature dependence on field emission performance.

To further examine the gas desorption and the outgassing from the vacuum chamber and components, additional RGA measurements were performed.

Figure 7 shows the complete mass spectra for 25 (before heat-treatment), 400, and 25 °C (after heat-treatment) with the die in the chamber. From Fig. 7, it can clearly be seen that water vapor was the dominant desorbing gas for all three cases. However, to compare the desorption of water vapor along with other gas species for with and without the field emission array wafer section, additional temperature points were also studied and...
analyzed. Figure 8 shows a bar chart of the partial pressure for most of the gases in the chamber for the temperature points of 25 (before heat-treatment), 300, 350, 400, and 25 °C (after heat-treatment). From Fig. 8, it can be seen that the water vapor pressure at 350 °C is \( \approx 1.3 \times 10^{-6} \) Torr and the CO\(_2\) partial pressure is \( \approx 3 \times 10^{-7} \) Torr when the wafer section is present inside the chamber.

However, when the wafer section is not present inside the chamber, the water vapor partial pressure is \( \approx 1.8 \times 10^{-7} \) Torr, and the CO\(_2\) partial pressure is \( \approx 9 \times 10^{-10} \) Torr. These data confirm that the primary source of water vapor and CO\(_2\) desorption at 350 °C is from the wafer surface and not the vacuum chamber walls and system components.

To determine that this process is due to adsorption, another series of experiments were performed. After a device was heat-treated and cooled, it was removed from the vacuum chamber and allowed to sit in room air for 4–5 days. This process was repeated several times for the same device. The test set results, summarized in a bar chart in Fig. 9, show that the improved collector current and decreased gate current are not permanent.

After sitting in room air, the higher gate current and lower emission current return again to the values prior to heat-treatment. The process can be repeated each time the device is heat-treated in vacuum and removed from the chamber to sit in air.

These results confirm that heat-treatment does not create permanent changes to the emitter tip structure and that the adsorption and desorption of molecules (likely water) from the emitter tip and gate/emitter dielectric surface are the likely cause of the emission and leakage current changes. Note that these tests were repeated on 3 additional 1000 × 1000 arrays on the same wafer section with the same results.

IV. SUMMARY AND CONCLUSIONS

We have measured the \( I-V \) characteristics of several silicon-based field emission arrays including 1000 × 1000 tip arrays. Because of the large collector to gate distance, some emission current is collected on the gate. In addition, surface leakage results in a significant amount of current to the gate as well. The collector and gate currents from the arrays were studied versus temperature, and around 350 °C, the gate current decreased by more than ten times and the emission current increased by more than ten times. These results suggest that the majority of the current collected on the gate before heat-treatment was due to the surface leakage. However, even after heat retreatment, a significant emission current (\( \approx 26\% \)) is still collected at the gate, which could be the result of the long emitter-collector gap. These results were repeated for multiple devices. An RGA was used to measure the outgassing from the system during the temperature testing with small temperature increments (10 °C) from 300 to 400 °C. These measurements show very clear water desorption along with some carbon dioxide desorption. F–N plots of the \( I-V \) curves show a more linear plot after heat-treatment, which suggests either a cleaner (less water vapor) emitter tip surface or more tips emitting current after surface desorption. RGA measurements confirm that the high levels of water vapor and CO\(_2\) at 350 °C can be attributed to GFEA wafer and not the chamber walls and system components. If the devices were removed from vacuum for 4–5 days, the collector and gate currents returned to their original values, but subsequent heat-treatment returned the gate and collector current to their improved levels. These results strongly indicate that desorption from the emitter tip surface and from the dielectric between the gate and emitters affects the device performance. Hence, operation of NVCTs without heat-treatment to clean surfaces could be a concern and affect emission mechanisms. However, it is clear that these emitters are capable of operating stably from 25 to 400 °C once vacuum heat-treated as the collector current at 40 V varies by <3% over this temperature range. Future research will look at the noise figure at room temperature and at high temperature and at the effects of other gas species on emission, leakage, and noise. In addition, the effects of ultraviolet irradiation on gas desorption will also be studied.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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