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A Spatiotemporal Pattern Detector

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***Abstract*—A spatiotemporal pattern detector design is presented which can identify three fundamental spatiotemporal patterns consisting of two spikes (from different neurons or from the same neuron). These fundamental cases provide the building blocks for construction of more complicated arbitrary spatiotemporal patterns. The overall design consists of three primary subcircuits, and the operation of each is described. The detection of the three cases of spatiotemporal patterns, and the detection of a more complicated pattern by a network of Spatiotemporal Pattern Detectors, is then demonstrated through simulation using the Cadence Virtuoso platform.**

Keywords—Neuromorphic design, pattern detector, spatiotemporal pattern recognition, spiking neural network

I. Introduction

Spatiotemporal pattern recognition (STPR), within the context of spiking neural networks (SNN), is the process by which a spatiotemporal pattern is abstracted down to an output on a single neuron. STPR has been demonstrated using SNNs with synapses with spike-timing-dependent plasticity (STDP) a learning rule that updates synaptic weight according to a spike-timing-dependent learning rule [1]–[7]. In one common approach to STPR, SNNs are trained to recognize a pattern by repeatedly exposing them to the pattern embedded in noise [1], [2]. After repeated exposures, the synaptic weights adjust in accordance with an STDP learning rule so that the output neuron produces a spike which tends to coincide with the presentation of the pattern. Another approach to STPR involves knowing the pattern to be detected and designing a system to detect that particular pattern. One example of this approach uses a Spike Sequence Recognition Network with a global inhibitory neuron [7]. Another example of this approach uses a Key-Threshold based SNN which treats spikes as bits and "shifts in" spike trains to perform a bit-by-bit comparison with a key [8]. The circuit we present in this work is also an example of this approach, but unlike other approaches mentioned, which require precise timing or time steps to achieve pattern recognition, a user defined window of detection.

In this work, we present a circuit which can be used to detect simple spatiotemporal patterns and demonstrate that it can be used to detect complex spatiotemporal patterns when combined into networks without training. The goal of this circuit's design is to gain some insight into how digital SNNs perform STPR by reducing the number of variables involved. To do this, a network, composed of modified digital spiking leaky-integrate-and-fire (LIF) neurons and simple logic gates, was designed that is capable of detecting three simple spatiotemporal patterns: Na-Nb-Δt, Na-Na-Δt, and Na-Nb-coincidence, where Na and Nb are the first and second neurons to spike, respectively [9]. The three cases are depicted in Fig. 1. All synaptic weights are maximized and leakiness is minimized (leakiness is set by off-current). Section II of this paper discusses the circuit operation with detailed description of each subcircuit block. Section III demonstrates simulations of the circuit detecting spatiotemporal patterns. Conclusions are presented in Section IV.

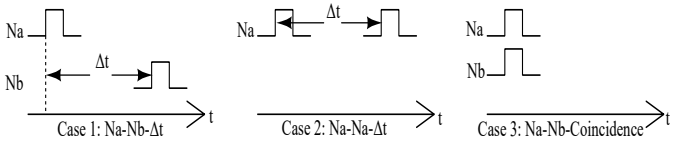

Fig. 1. The three fundamental spatiotemporal patterns that the circuit can detect. Case 1 illustrates the case where two outputs of two different neurons, Na and Nb, occur with some time, Δt, between them. Case 2 is a temporal pattern where a single neuron, Na, spikes twice with some time, Δt, between the spikes. Case 3 is a special case of Case 1 where Δt is reduced to zero so that the two spikes coincide.

II. Circuit Operation

The circuit presented in this work is a spiking network consisting of modified leaky integrate-and-fire neurons and simple logic gates designed for the TSMC 0.18 µm process and simulated in industry standard software Cadence Virtuoso using the NCSU PDK [10].

A. Spatiotemporal Pattern Detector Subcircuit

The Spatiotemporal Pattern Detector subcircuit shown in Fig. 2a is all that is strictly necessary to detect the three spatiotemporal patterns of Fig. 1. It consists of a window circuit and an AND gate. It produces a pattern detected signal (Vpatterndetected=Vdd) when an input spike from Vin2 occurs during a digital window (Vwindow=Vdd) produced by the window circuit. However, the resulting pattern detected signal may not have a full spike pulse width due to either a very short window ("large" Vwinwidth chosen by the user) or due to the input spike from Vin2 occurring at the edge of a window (see Fig. 2b)

B. Window Circuit

The Window circuit consists of two modified LIF neurons which act as analog timing circuits. The window circuit can operate in two modes: non-coincidence and coincidence detection modes which correspond to the state of Vcoin. Vcoin

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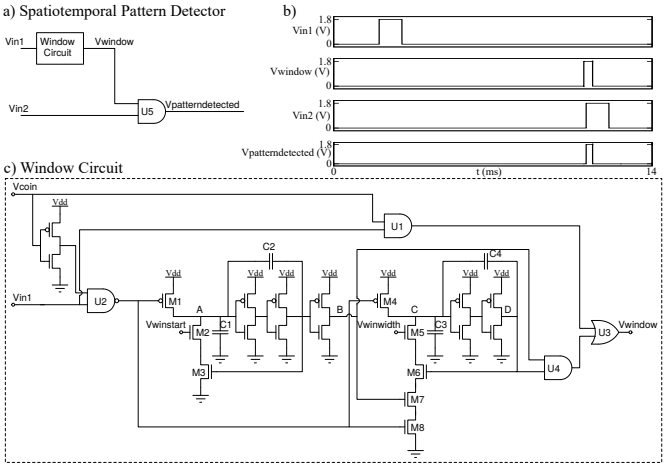

Fig. 2. a) A block diagram of the Spatiotemporal Pattern Detector. b) The response of the spatiotemporal pattern detector to stimulus with Vcoin tied to gnd. The pulses applied to Vin1 and Vin2 are 1.8 V for duration 1 ms. c) Schematic of the window circuit.

is a voltage set by the user to either gnd or Vdd for non-coincidence and coincidence modes, respectively. In the non-coincidence mode of operation, meaning that Vcoin is tied to gnd, a simple digital pulse at Vin1 charges C1, C2, C3, and C4. Initially, V_A and V_C are at logical 0. When a digital pulse arrives at Vin1, V_A quickly rises to logical 1 due to a combination of M1 being saturated and feedback from C2 after V_B rises to Vdd. Similarly, V_C quickly rises to logical 1 due to a combination of M4 being saturated and feedback from C4 after V_D rises to Vdd. This, in turn, raises the potential at nodes B and D to raise to Vdd and quickly saturate M3 and M6. This causes C1 and C2 to discharge at a rate controlled by M2 and, the user selected potential, Vwinstart. When a sufficient amount of time has passed (determined by the user's choice of Vwinstart) enough charge will have passed to ground from C1 and C2 via M2 and M3 that Node A will have dropped below the inverter threshold (θ), causing node B to fall to gnd. This places a logical 1 on U4 and causes M7 to quickly saturate. The logical 1 due to node B being at gnd, combined with the logical 1 due to node D being at Vdd, causes the window circuit to output a logical 1 (Vwindow=Vdd). With M7 saturated, C3 and C4 discharge through M5, M6, M7, and M8 at a rate controlled by M5 and, the user selected potential, Vwinwidth. When a sufficient amount of time has passed (determined by the user's choice of Vwinwidth) enough charge will have passed to ground from C3 and C4 via M5, M6, M7, and M8 that node C will have dropped below θ, causing node D to fall to gnd and the window circuit to output a logical 0. The result is that Vwinstart and Vwinwidth control the start and duration, respectively, of a digital window initiated by an input spike at Vin1.

In the coincidence mode of operation, meaning that Vcoin is tied to Vdd, U2 prevents input spikes from reaching the LIF neurons. Instead, Vwindow is created through simple logic (Vin1 AND Vcoin).

C. Pulse Formatter and Refractory Circuits

To address the issue of shortened pattern detected pulses, a pulse formatter subcircuit has been created that is attached to the output. It consists of a single LIF circuit that produces a pulse, the width of which is set by Vpw, for an input from the Spatiotemporal Pattern Detector subcircuit. This ensures that the Spatiotemporal Pattern Detector produces pulses of a consistent width. The refractory subcircuit consists of a single LIF circuit that produces a pulse, the width of which is set by Vrefrac. The refractory subcircuit prevents the pulse formatter circuit from producing any pulses during a refractory period set by Vrefrac. Fig. 3 depicts the pulse formatter and refractory subcircuits.

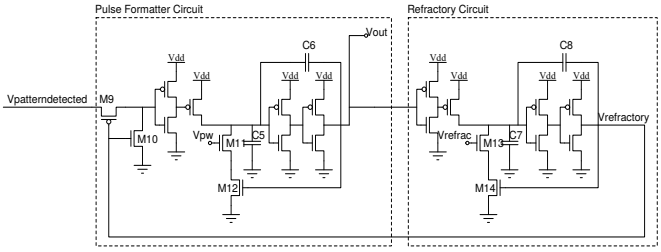

Fig. 3. The Pulse Formatter and Refractory circuits. The pulse Formatter takes Vpatterndetected signals and produces an output pulse of a width determined by the user set Vpw. The Refractory circuit produces a signal, Vrefractory, which prevents Vpatterndetected signals from reaching the Pulse Formatter Circuit.

III. Spatiotemporal Pattern Detection Demonstration

A. Case 1: Na-Nb-Δt

In Case 1, the pattern consists of two input pulses, one from each of two different neurons, separated by some time Δt. To detect a Case 1 pattern, the circuit is placed in non-coincidence mode (Vcoin=gnd) and the user sets the start and duration of the desired digital window and the output pulse width and refractory period via Vwinstart, Vwinwidth, Vpw, and Vrefrac respectively. Fig. 4 depicts the circuit detecting a Case 1 pattern.

Initially, V_A and V_C are at logical 0. When a digital pulse arrives at Vin1, V_A quickly rises to logical 1 due to a combination of M1 being saturated and feedback from C2 after V_B rises to Vdd. Similarly, V_C quickly rises to logical 1 due to a combination of M4 being saturated and feedback from C4 after V_D rises to Vdd.

When the digital pulse ends, V_A and V_C start lowering at rates determined by Vwinstart and the off current of M7 respectively ($|d/dt\ V_A| >> |d/dt\ V_C|$). When V_A falls below θ, V_B is pulled down quickly to gnd. This places a logical 1 on U4, resulting in Vwindow quickly rising to Vdd, and causing M7 to quickly saturate, which causes V_C to lower more rapidly as the discharge rates of C3 and C4 are now limited by Vwinwidth instead of the off current of M7 (since M7 is no longer "off").

If a digital pulse arrives at Vin2 while Vwindow is a logical 1, then Vpatterndetected quickly rises to logical 1. This is detected by the Pulse Formatter circuit. As the Pulse Formatter circuit is simply a LIF circuit with a maximum synaptic connection strength, it fires immediately causing Vout to rise quickly. This in turn causes the refractory circuit to fire immediately (it is also a LIF circuit with a maximum synaptic connection strength) causing Vrefractory to rise to Vdd and C7 and C8 to start discharging through M13 and M14 at a rate

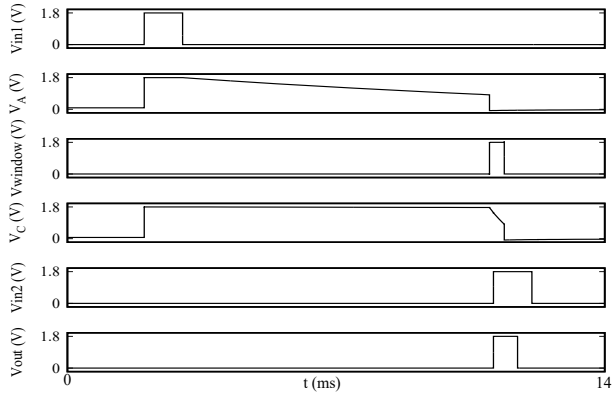

Fig. 4. Case 1:Na-Nb-Δt. Initially, the circuit is in non-coincidence mode (Vcoin=gnd) and V_A and V_C are at logical 0. When a digital pulse arrives at Vin1, V_A and V_C rise as C1, C2, C3, and C4 charge up. When the pulse ends, V_A lowers as C1 and C2 begin to discharge at a rate determined by the user (Vwinstart) and V_C lowers as C3 and C4 begin to discharge at a rate determined by the off current of NMOS M7 (very small). When V_A crosses θ, it drops quickly to logical zero, Vwindow goes high, and V_C starts to lower more quickly as the discharge rate of C3 and C4 are now limited by Vwinwidth (which is chosen by the user.) If a second digital pulse arrives at Vin2 while Vwindow is high, Vpatterndetected goes high and causes the pulse formatter circuit to generate a pulse on Vout and the refractory circuit to initiate a refractory period.

determined by Vrefrac. Vrefractory at Vdd turns M9 off, preventing Vpatterndetected from influencing the output while Vrefractory is high, and turns M10 on creating a path to discharge charge trapped by M9. Another thing that happens when Vout rises to Vdd is that C5 and C6 begin discharging through M11 and M12 at a rate controlled by Vpw. When the voltage across C5 drops below θ, Vout is pulled to gnd. After V_C falls below θ, V_D is pulled down quickly to gnd. This places a logical 0 on U4, which in turn quickly pulls down Vwindow to gnd.

B. Case 2: Na-Na-Δt

In Case 2, the pattern consists of two input pulses, each from the same neuron, separated by some time Δt. To detect a Case 2 pattern, the circuit is placed in non-coincidence mode (Vcoin=gnd), the circuit inputs Vin1 and Vin2 are tied together, and the user sets the start and duration of the desired digital window and the output pulse width and refractory period via Vwinstart, Vwinwidth, Vpw, and Vrefrac respectively. Fig. 5 depicts the circuit detecting a Case 2 pattern.

Initially, V_A and V_C are at logical 0. When a digital pulse arrives at Vin1 and Vin2 (they are tied together), V_A quickly rises to logical 1 due to a combination of M1 being saturated and feedback from C2 after V_B rises to Vdd. Similarly, V_C quickly rises to logical 1 due to a combination of M4 being saturated and feedback from C4 after V_D rises to Vdd.

When the digital pulse ends, V_A and V_C start lowering at rates determined by Vwinstart and the off current of M7 respectively ($|d/dt\ V_A| >> |d/dt\ V_C|$). When V_A falls below θ, V_B is pulled down quickly to gnd. This places a logical 1 on U4, resulting in Vwindow quickly rising to Vdd, and causing M7 to quickly saturate, which causes V_C to lower more rapidly as the discharge rates of C3 and C4 are now limited by M5 and Vwinwidth instead of the off current of M7 (since M7 is no longer "off").

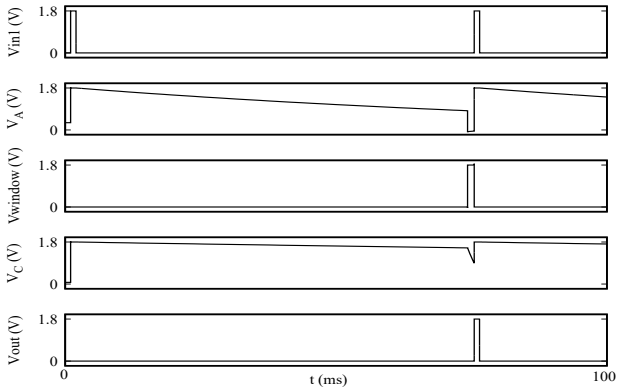

Fig. 5. Case 2:Na-Na-Δt. Initially, the circuit is in non-coincidence mode (Vcoin=gnd), Vin1 and Vin2 are tied together, and V_A and V_C are at logical 0. When a digital pulse arrives at Vin1, V_A and V_C rise as C1, C2, C3, and C4 charge up. When the pulse ends, V_A lowers as C1 and C2 begin to discharge at a rate determined by the user (Vwinstart) and V_C lowers as C3 and C4 begin to discharge at a rate determined by the off current of NMOS M7 (very small). When V_A crosses θ, it drops quickly to logical zero, Vwindow goes high, and V_C starts to lower more quickly as the discharge rate of C3 and C4 are now limited by Vwinwidth (which is chosen by the user.) If a second digital pulse arrives at Vin1 while Vwindow is high, Vpatterndetected goes high and causes the pulse formatter circuit to generate a pulse on Vout and the refractory circuit to initiate a refractory period. Also, V_A and V_C rise as C1, C2, C3, and C4 are recharged by the new pulse, cutting the window off and setting up the circuit to detect another Na-Na-Δt pattern.

If another digital pulse arrives at Vin1 and Vin2 while Vwindow is a logical 1, then Vpatterndetected quickly rises to logical 1. This causes V_A and V_C to rise as C1, C2, C3, and C4 are recharged by the new pulse, cutting the window off and setting up the circuit to detect another Na-Na-Δt pattern, while Vpatterndetected is detected by the pulse formatter circuit. As the pulse formatter circuit is simply a LIF circuit with a maximum synaptic connection strength, it fires immediately causing Vout to rise quickly. This, in turn, causes the refractory circuit to fire immediately (it is also a LIF circuit with a maximum synaptic connection strength) causing Vrefractory to rise to Vdd and C7 and C8 to start discharging through M13 and M14 at a rate determined by Vrefrac. Vrefractory at Vdd

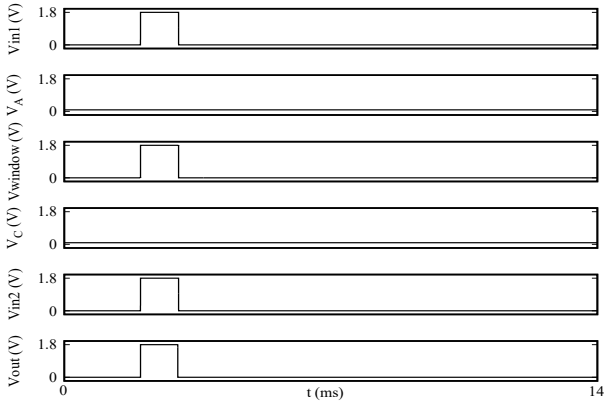

Fig. 6. Case 3: Na-Nb-coincidence. Initially, the circuit is in coincidence mode (Vcoin=Vdd) and V_A and V_C are at logical 0. When a digital pulse arrives at Vin1, V_A and V_C remain unchanged as the output of U2 is held at logical 1 by Vcoin. When a digital pulse arrives at Vin1, Vwindow goes high through U1 and U3. If a second digital pulse arrives at Vin2 while Vwindow is high, Vpatterndetected goes high and causes the pulse formatter circuit to generate a pulse on Vout and the refractory circuit to initiate a refractory period.

turns M9 "off", preventing Vpatterndetected from influencing the output while Vrefractory is high, and turns M10 "on" creating a path to discharge charge trapped by M9. Another thing that happens when Vout rises to Vdd is that C5 and C6 begin discharging through M11 and M12 at a rate controlled by Vpw. When the voltage across C5 drops below θ, Vout is pulled to gnd. After V_C falls below θ, V_D is pulled down quickly to gnd. This places a logical 0 on U4, which in turn quickly pulls down Vwindow to gnd.

C. Case 3: Na-Nb-Coincidence

In Case 3, the pattern consists of two input pulses, each from one of two different neurons, occurring at the same time. This is a special case of Case 1 where Δt=0. It should be noted that overlapping input pulses will cause a detection and not just coincidental pulses. However, in this mode of operation coincidental pulses will be detected. Fig. 6 depicts the circuit detecting a Case 3 pattern.

D. Larger Spatiotemporal Patterns

Larger spatiotemporal patterns can be detected by networks of Spatiotemporal Pattern Detector circuits. Fig. 7a shows a network of Spatiotemporal Pattern Detector circuits. Each Spatiotemporal Pattern Detector is depicted as an AND gate with the start time of its window written in its body and Vin1 above Vin2. Simulation of a network with 25 spiking input neurons is provided in Fig. 7b. The input consists of a pattern, highlighted in grey, embedded within random activity. The network of Fig. 7a is identifying a sub-pattern generated by neurons 1, 3, 7, 10, 11, and 20 as indicated by the "Pattern Detected" signal. If detecting a sub-pattern is insufficient, then a larger detector can be used to detect the entire pattern.

IV. Conclusion

A Spatiotemporal Pattern Detecting circuit was presented capable of detecting three fundamental spatiotemporal spike patterns. A network of Spatiotemporal Pattern Detectors was then created to detect a more complicated spatiotemporal pattern. Future work will continue to explore these pattern detectors and attempt to bridge the gap between them and more traditional spiking neural networks.

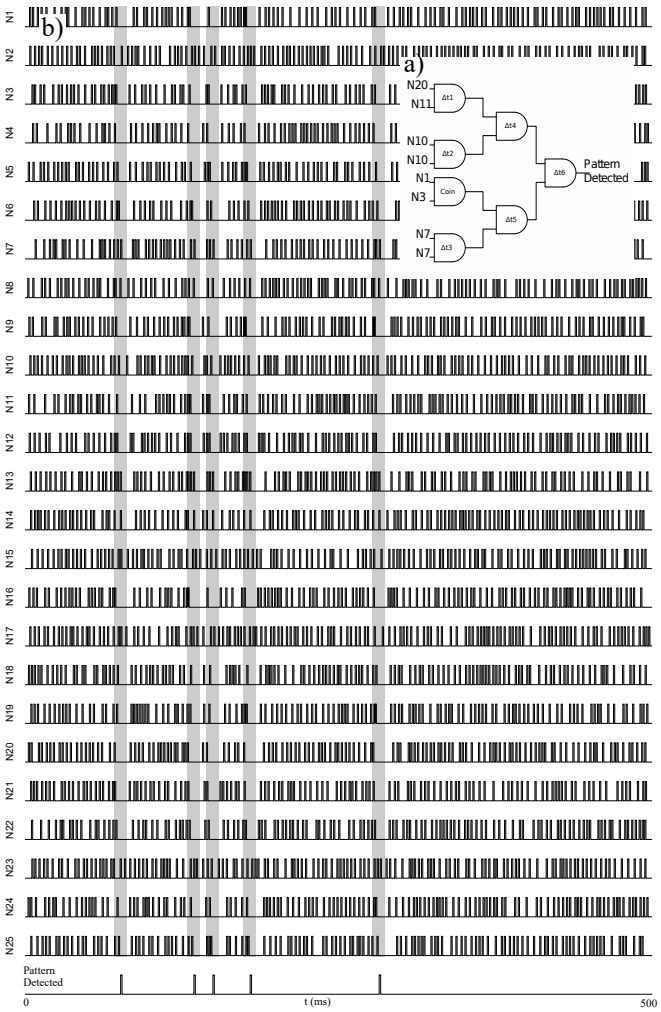

Fig. 7. a) A block diagram of a network of Spatiotemporal Pattern Detectors, where each Spatiotemporal Pattern Detector is depicted as an AND gate with the start time of the window written in the body and Vin1 above Vin2. Each Δt indicates the amount of time between the appropriate pattern spikes. For example Δt1 is the time between the pattern spikes from N20 and N11. This network was designed to detect the pattern highlighted in grey. b) The simulation results of the network depicted in Fig. 7a. A combination of pattern and noise input spikes from neurons N1 through N25 results in a pattern detection signal that coincides with the presentation of the pattern (highlighted in grey) indicating that the desired pattern was detected.

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