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Electrical Characteristics of Nanocrystalline Silicon Resistive Memory Devices

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Introduction: Resistive memory devices have been studied and fabricated using a wide variety of materials including chalcogenides [1], metal oxides [2], and hydrogenated amorphous silicon (a-Si:H) [3]. The most promising materials seem to be amorphous in nature, with the properties of the atomic lattices being conducive to the physical mechanisms that underlie the subsequent resistive switching. The devices are also finding applications beyond high-density digital memory, such as for electronic synapses in neuromorphic systems [4], [5]. However, a different set of properties is required in the latter case compared to devices that must only store binary values. In addition, it is well known that biological synapses are extremely unreliable and noisy, and yet the brain is still able to perform high-level cognitive functions [6]–[8]. This work uses pulse-based electrical characterization techniques to demonstrate the stochastic nature of resistive switching in nanocrystalline silicon (nc-Si) Conductive Bridge Resistive Memory (CBRAM) Devices. We chose nc-Si active layers so these devices could potentially be co-fabricated in the same process as nc-Si TFTs [9]–[11]. Our subsequent findings indicate the device properties may be particularly useful for some non-von Neumann computing paradigms. Though much research has been done using a-Si:H, results from nc-Si CBRAM devices have not been published. In this study, we showed that the switching of the device depends on the history of current passing through it, and not only the voltage applied. Further, the resistance switching in the devices is stochastic, making them ideal candidates for a biologically realistic synapse.

Device Fabrication: Devices were fabricated on a p⁺ Si wafer with 0.01–0.02 Ω -cm resistivity. The 20 nm thick nc-Si active layer is deposited immediately after HF dip using PECVD with 1:100 SiH₄ diluted in H₂. Deposition temperature was 250 °C with RF power 150 W, gas flow of 600 sccm, and chamber pressure 900 mTorr. Using XRD (Fig. 1) and TEM (not shown), the crystallite size was found to be approximately 7 nm, with a volume fraction relative to amorphous material approaching 70%. Following nc-Si deposition, 100 nm of SiO₂ was deposited in-situ as an insulation layer into which vias of area 25 μ m² were etched using 1% HF. Vias were sputtered with silver and Si mixed layer followed by pure a silver and gold top contact pad resulting in the structure of Fig. 2. The bottom electrode was formed by sputtering a layer of Al.

Results and Discussion: All device measurements were performed using a Keithley 4200-SCS. Individual devices presented very consistent hysteresis in the quasi-DC hysteresis curves (not shown). However, variation in turn ON and OFF voltages was observed across the die. This may be due to the resistance noise coming from the device, which is still under analysis, or non-uniform depositions in either the PECVD or sputtered layers. With a Ag and Si mixed layer, no forming step was required as observed by other groups [12]. A mix layer seems to provide better mobility and directionality to the Ag filament in the active layer. Fig. 4a depicts the behavior of the device when it is pulse cycled; current is read after every pulse using different read voltages. It is observed that device turns ON and OFF very randomly, especially at lower read voltages. Similarly, Fig. 4c depicts the nature of the device at varying pulse width. Increasing variability in current is noticed at lower pulse widths. Fig. 4b represents the input voltage pulses used for these measurements. Fig. 5 represents the behavior of the device when multiple varying voltage and frequency pulses are provided in effort to turn the device ON. In Fig. 5a, 5 V pulses provided at 10 ms and 1 ms turn the device on but with large resistance fluctuation. In Fig. 5b, 6 V, 10 ms pulses decrease device resistance early on but at 1 ms/100 μ s resistance still fluctuate between high and low until 4000/16000 pulses. As voltage increases to 7V in Fig. 5(c) switch is attained very early on by 10ms and 1ms pulse and within 5000 pulses at 100 μ s. Input voltage pulses as represent in Fig. 3a. As no switching was observed in Fig. 5 at higher frequencies of 10 μ s/1 μ s ON time even after 20000 pulses were applied, this range was increased up to 10⁸ pulses in Fig. 6, input represented by Fig. 3b. The device eventually turned on even at higher frequency of 10 μ s (Fig. 6b) and 1 μ s ON time (Fig. 6c). However, more pulses are required to turn on the device at lower voltages and this spread increases with increase in frequency.

Conclusions: This research highlights the potential use of nc-Si active layers as a viable candidate for CBRAMs for synaptic memory devices. The demonstrated stochastic nature of resistive switching between high and low resistance states before stabilizing may be a desirable feature in neuromorphic design.

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Fig. 1. XRD spectrum of nc-Si used as the active layer.

Fig. 2. Cross-sectional illustration of resistive memory device.

Fig. 3. Input Pulse trains (a) and (b) are used to obtain data in Figs. 4 and 5, respectively.

Fig. 4. (a) Maximum current changes with change in read voltage and device turns ON and OFF very stochastically specifically at lower read voltages. (b) Pulse train applied for the measurements. (c) Maximum current changes with frequency with noticeable variation in turns ON and OFF current at lower frequencies.

Fig. 5. 200 write pulses applied followed with a read pulse as shown in Fig. 3a. (a) at 5 V, 10 ms and 1 ms pulses switches device between high and low resistance before device turns ON steadily after 12000 pulses. (b) at 6 V, 10 ms and 1 ms pulses switch device state early on but 100 μ s pulses switch device stably to low resistance after 16000 pulses. (c) at 7 V, 10 ms, 1 ms and 100 μ s pulses bring device to low resistance state quicker. 10us and 1us, high frequency pulses never turned ON the device even after 20,000 pulses were applied. This shows stochastic behavior of the device.

Fig. 6. Logarithmically increasing number of write pulses were applied followed with a read pulse as shown in Fig. 3b. It can be noted that device eventually turned on even at lower frequencies of 100 μ s, 10 μ s and 1 μ s though higher number of pulses need to be applied for higher frequencies and lower voltages.