ELECTRICAL SWITCHING STUDIES OF CHALCOGENIDE-BASED

ION-CONDUCTING VARIABLE RESISTANCE DEVICES

by

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ABSTRACT

In this work, ion-conducting devices using layers of chalcogenide materials are explored as potential non-volatile memory devices. This technology is also known in the literature as conductively bridged RAM (CBRAM), programmable metallization cell (PMC), and programmable conductor RAM (PCRAM; not to be confused with the acronym PCRAM as used to denote phase-change memory).

Electrical measurements with five different programming currents at four temperatures have been performed on two-terminal devices comprised of silver with a metal-selenide and germanium-chalcogenide layer. The metal-selenide layer is Sb_2Se_3, SnSe, PbSe, In_2Se_3, or Ag_2Se. The germanium-chalcogenide layer is either Ge_2Se_3 or GeTe. Total ionizing dose radiation effects are also investigated for GeTe/SnSe/Ag and Ge_2Se_3/SnSe/Ag devices.

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CHAPTER 1: INTRODUCTION

1.1 Introduction and Motivation

There is an assemblage of personal media devices that use non-volatile electronic memory (NVM) that are increasingly in demand, such as digital cameras, music players, and cell phones. NVM is distinguished from volatile memory (such as Dynamic Random Access Memory) in that it retains its data state in the absence of power to the memory.

The leading NVM device is Flash. A Flash device uses a charge storage mechanism that requires a high voltage, 5 to 8 V or more, to operate. Flash has a few disadvantages for many applications, however. First, it is damaged by radiation. Flash memory can, thus, lose its data state or be rendered nonfunctional if exposed to radiation. Second, the high voltage requirements of Flash make it unattractive in applications for which low power operation is necessary. Third, because of the way Flash stores the data state, a scaling limit is close to being reached, which will prevent higher density memory arrays from being realized. For these reasons, new types of NVM are under investigation in the hopes that Flash can be replaced with a memory device that is not prone to any of the disadvantages of Flash.

The ideal NVM should be low cost, have fast write and read access times, low energy consumption, high cycling endurance greater than 10^7 cycles (1), and reliable data retention in standard conditions and conditions of radiation exposure. Devices that are

currently being explored include resistive variable devices, such as phase change

memory, resistive oxide memory, and ion-conducting memory devices.

In this work, ion-conducting devices using layers of chalcogenide materials are

explored as potential non-volatile memory devices. This technology is also known in the

literature as conductively bridged RAM (CBRAM), programmable metallization cell

(PMC), and programmable conductor RAM (PCRAM; not to be confused with the

acronym PCRAM as used to denote phase change memory).

1.2 Overview of Ion-Conducting Variable Resistance Devices

Ion-conducting devices are composed of a medium that is amorphous and that

acts as an insulator and a metal ion storage medium, as well as a source of metal ions.

The source of metal ions is an electrochemically active material that is enclosed next to

the amorphous medium between two electrode pads, forming a simple metal-insulator-

metal (MIM) structure. The most common electrochemically active metals used are Ag

or Cu. Common amorphous materials used include oxides and chalcogenides.

The devices are commonly fabricated in a high resistance state. When a voltage

bias is applied to the anode, the active metal will oxidize and become a positive ion. The

positively charged metal ion will drift due to the induced electric field through the

amorphous layer. When the positively charged metal ion reaches the cathode, it will be

reduced and become neutral; this process is referred to as electro-deposition. Additional

positively charged metal ions will then reach the now neutral metal and be reduced. This

sequence continues until the active metal creates a conductive channel between the two

electrodes. The conductive channel will be thicker in shape at the cathode because the bulk of electro-deposition occurs there (2). When a bias voltage of opposite polarity is applied, the cathode becomes the anode and vice versa. The neutral metal in the conductive channel will be oxidized once again and drift with the electric field, which is in the opposite direction from before. Because of the lack of an active metal source on the cathode side of the device, the conductive channel will be severed, and the device will be in a high resistance state. These devices exhibit bipolar switching, meaning that reversed voltage polarities are required to change the state of the devices. The ion-conducting devices are read by applying a potential across the device and measuring the resistance. The state of the ion-conducting device is defined by the resistance value.

The research in this thesis investigates the effects on device operating parameters of Ag in various chalcogenide glasses as the medium with an additional metal-selenide layer.

1.2.1 <u>Operation of Silver Ion Migration Through Chalcogenide Glasses</u>

The exact mechanism by which the Ag (or Cu) forms and dissolves as a conductive channel is not fully understood. One theory is that the amorphous chalcogenide films provide pathways for fast transport of cations like silver in a reduction-oxidation (redox) reaction when a potential is applied to the electrodes (3; 4). This theory assumes that the silver is electroplated on the bottom electrode when reduced from a cation to a neutral atom and that the silver cations continue to electro-deposit until they reach the top electrode. The ease with which this happens not only depends on the

applied potential but also on the structure of the amorphous chalcogenide. Another theory is that Ag will form a bond with Se, which provides a shorter pathway for the silver cations to drift in an electric field before being reduced (1; 5). Recently, a model using density functional theory of Ag in Ge_2Se_3 has hypothesizes that Ag will displace the germanium (Ge) from Ge-Ge bonds to form strong Ag-Ge bonds, also creating shorter pathways for subsequent reformations of a silver conductive pathway (6).

The ion-conducting two-terminal devices fabricated in this study consist of layers from top to bottom: tungsten top electrode, silver layer, metal-selenide layer, germanium-chalcogenide layer, and a tungsten bottom electrode. The varying metal in the metal-selenide layer are lead (Pb), antimony (Sb), tin (Sn), indium (In), or silver (Ag). The chalcogenide in the germanium-chalcogenide layer is either selenium (Se) or tellurium (Te). In addition to those layers, there are adhesion Ge_2Se_3 layers that are described further in Chapter 2. The device is considered 'ON' when in a low resistance state and 'OFF' when in a high resistance state. The ion-conducting device will be in a high resistance state when fabricated due to the chalcogenide amorphous layers behaving as an insulator between two metal electrodes. The silver is easily oxidized and releases an electron to the adjoining chalcogenide layer or to the anode (top electrode) when a very small potential is applied in order to form the ion Ag^+. To write to a low resistance state, the device requires a positive voltage bias sweep to the top electrode, which produces an electric field in which the Ag^+ ions drift through the chalcogenide layers and reduce at the bottom electrode. When the silver eventually spans the top and bottom electrodes,

forming a conductive channel, the device will be in a low resistance state. A negative

potential applied to the top electrode will sever the silver conductive channel, and the

device will be in a high resistance state again.

A voltage versus current (IV) curve from a DC sweep of an ion-conducting device

shows a distinct 'ON' and 'OFF' resistance state. An example IV curve for an ion-

conducting device is shown in Figure 1.1. The two-terminal device in the figure had a

positive double DC sweep from 0 V to 1 V and back to 0 V applied to the top electrode.

Then, a subsequent negative double DC sweep from 0 V to -1 V and back to 0 V was

administered to the top electrode. The two separate measurements are combined into one

graph in Figure 1.1. The positive DC sweep had a compliance current of 10 µA in order

to prevent excess current through the device when it switched rapidly to a low resistance

state.
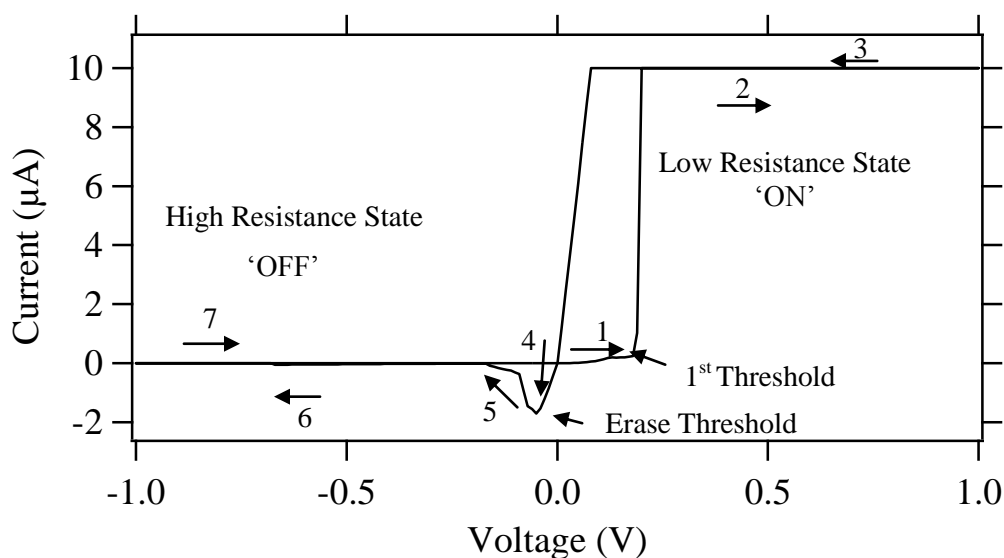
Figure 0.1: IV Curve for Ge$_2$Se$_3$/SnSe/Ag device.

The DC sweep of Figure 1.1 is somewhat misleading because it looks as if the voltage increases to 1V; that, however, is not the case. When the sweep reaches the critical voltage labeled as the 1st threshold in Figure 1.1 and referred in this study as V_{T1}, the current increases to the compliance current set by the parameter analyzer. The positive DC sweep measurement still continues through the number of steps set up in the procedure, but the actual applied potential clamps at the voltage at which the compliance current is maintained, which is less than the threshold voltage. This effect is seen in the number 3 trace in Figure 1.1, which has a lower voltage than the V_{T1} when it returns to 0 V. The positive DC sweep is considered the Write Sweep because you are 'writing' or programming the device into a low resistance.

At the erase threshold, the device goes from a low resistance state to higher resistance state when the conductive silver channel has been disrupted during the application of a negative potential. This negative DC sweep is considered the Erase Sweep because you have 'erased' the device's programmed low resistance and returned it to a high resistance state. The erase sweep is asymmetric to the write sweep as evident in Figure 1.1 and has 1 mA compliance current to restrict current flow. Commonly, the resistance at the erase threshold is not the highest resistance of the device; there is still some conductivity as seen in the number 5 trace in Figure 1.1.

The threshold voltage of an ion-conducting device will be dependent on the ease of the ion movement through the medium with an applied electric field. Within the same material system, the greater the film thickness results in a greater threshold voltage. It

has been modeled that within the Ge_2Se_3 system, Ag readily releases an electron to become Ag^+ (6). With an increased distance for the Ag^+ ion to drift, a larger potential is needed to create the adequate electric field.

The ion-conducting device can be programmed into variable resistance states during the write sweep by limiting the amount of current allowed through the device. The 'ON' resistance is inversely proportional to the magnitude of the compliance current; e.g., a higher compliance current will create a lower 'ON' resistance.

The 'ON' state is dependent on the silver conductive channel, which is assumed to be much smaller than the device area and hence independent of electrode size contact (7). The high resistance 'OFF' state can be increased by reducing the contact electrode area (8). This effect is explained by the classic equation for resistance, $R = \rho \frac{l}{A}$. Where ρ is the electrical resistivity of the material, l is the length or thickness, and A is the cross-sectional area.

1.3 Summary of Thesis

To achieve the role as a universal memory, there are certain guideline values that need to be achieved. The NVM should achieve a high ('OFF') and low ('ON') resistance value difference greater than an order of magnitude with data retention of greater than ten years, and it should utilize write/erase voltages of a few hundred mV and pulse times less than 10 μs to compete with Flash. Ion-conducting devices are a contender in the race for a universal memory.

The characteristics of ion-conducting devices can be modified by the choice of chalcogenide glass and metal-chalcogenide material. In this research, the electrical switching characteristics of devices comprised of metal chalcogenide layers consisting of various metal-selenides (with the metal either being Pb, Sn, Sb, Ag, or In) and a Ge_2Se_3-chalcogenide layer are compared. Additionally, a comparison of the $SnSe:Ge_2Se_3$-based device and the $SnSe:GeTe$-based device is performed.

Chapter 2 provides a description of the devices studied and the electrical tests performed in this work. Chapters 3 and 4 present electrical measurement results for the devices under study and discuss trends in electrical switching properties with respect to the metal chalcogenide layer and the chalcogenide glass layer. Chapter 5 presents electrical characterization results during and after total ionizing dose radiation testing. Lastly, Chapter 6 provides of summary of the key results of this research.

CHAPTER 2: ION-CONDUCTING DEVICES: MATERIALS AND ELECTRICAL

CHARACTERIZATION METHODOLOGY

2.1 Introduction

In this chapter, the description of the germanium-chalcogenide/metal-selenide/Ag

ion-conducting device layout, fabrication, materials, and electrical characterization

measurements are discussed.

2.2 Ion-Conducting Two-Terminal Device Layout

All devices tested in this work had the same two-terminal device layout consisting

of tungsten electrodes with varying stacked layers in a 0.25 μm contact. A pictorial

representation of the device is shown in Figure 2.1. A SEM top-down image of a

fabricated two-terminal device used in this work is shown in Figure 2.2.
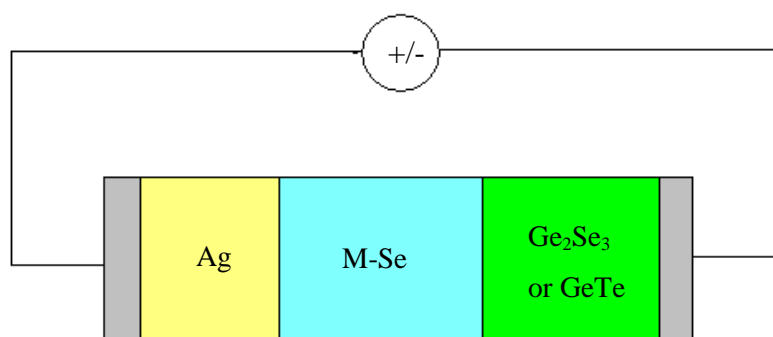
Figure 2.1: Cartoon of the Two-Terminal Device Showing the Sandwiched Layers Between Two Tungsten Electrodes. Layer Thicknesses Are Not Drawn to Scale. M Represents: Pb, Sb, Ag, Sn, and In
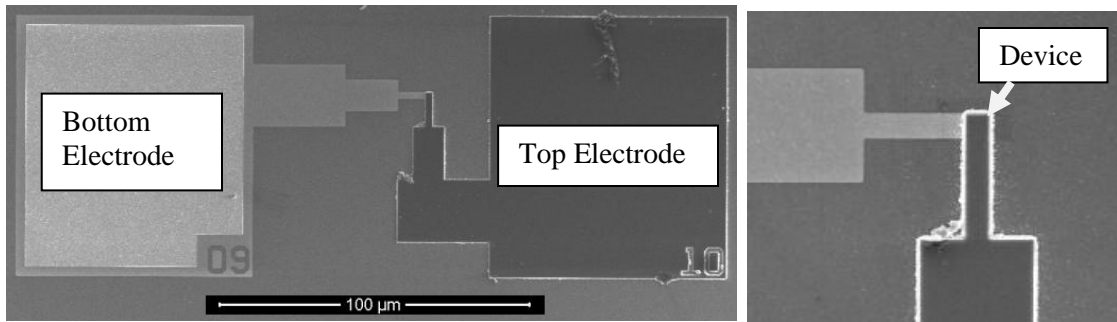
Figure 2.2: Top-Down SEM Image of a Two-Terminal Device Showing Top and Bottom Electrodes a) Low Magnification and b) High Magnification Image of Device Contact. Images Are Courtesy of Micron Technology.

Figure 2.2 is a top-down SEM image of an untested two-terminal device. The two terminals are labeled as bottom electrode and top electrode. The large electrodes are needed for proper probe tip placement to perform electrical testing. The magnified image of the two metal lines from the electrodes intersection points out the location of the 0.25 μm contact where the device actually resides. The metal lines provide the path from the electrodes to the device. Note the residue on the top electrode. The residue is un-removed photoresist. The unaltered photoresist on the top electrode acts as an indicator for untested (virgin) devices. The probe tip will leave a scratch in the photoresist when performing electrical testing on the devices and provides a marker that the device has been previously tested.

A cross-section of the device's film layers as deposited is shown in Figure 2.3. The layer thicknesses are not drawn to scale and act as a reference. The target film thicknesses are provided in Table 2.1. The Ge_2Se_3 adhesion layers (shown in Figure 2.3) are not listed in Table 2.1 since they are not key layers for device operation but are

necessary only for electrode adhesion. In all devices, the adhesion layers include 150 Å

and 100 Å Ge_2Se_3 between the M-Se/Ag films and Ag/W films, respectively.
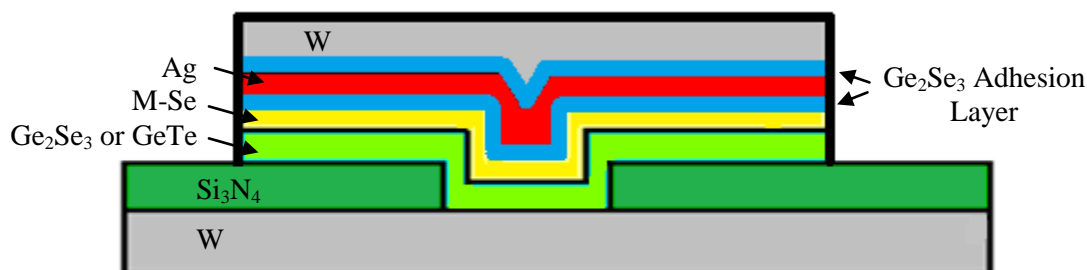
Figure 2.3: Cross-Sectional Representation of Device Including Ge_2Se_3 Adhesion Layer Films.

Table 2.1: Table of the Devices Tested in This Work and Corresponding Target Film Thicknesses.

Device #	Bottom Electrode	Germanium-Chalcogenide	Metal-Selenide	Ag	Top Electrode
1	W	Ge_2Se_3	Sb_2Se_3	Ag	W
	350Å	300 Å	500 Å	500 Å	350 Å
2	W	Ge_2Se_3	SnSe	Ag	W
	350 Å	300 Å	500 Å	500 Å	350 Å
3	W	Ge_2Se_3	PbSe	Ag	W
	350 Å	300 Å	1000 Å	500 Å	350 Å
4	W	Ge_2Se_3	Ag_2Se	Ag	W
	350 Å	300 Å	500 Å	500 Å	350 Å
5	W	Ge_2Se_3	In_2Se_3	Ag	W
	350 Å	300 Å	500 Å	500 Å	350 Å
6	W	GeTe	SnSe	Ag	W
	350 Å	300 Å	500 Å	500 Å	350 Å

A cross-sectional SEM image of a device of type 2 with Ge_2Se_3/SnSe (see Table

2.1) is shown in Figure 2.4. The corresponding STEM mapping of the device is also

provided.
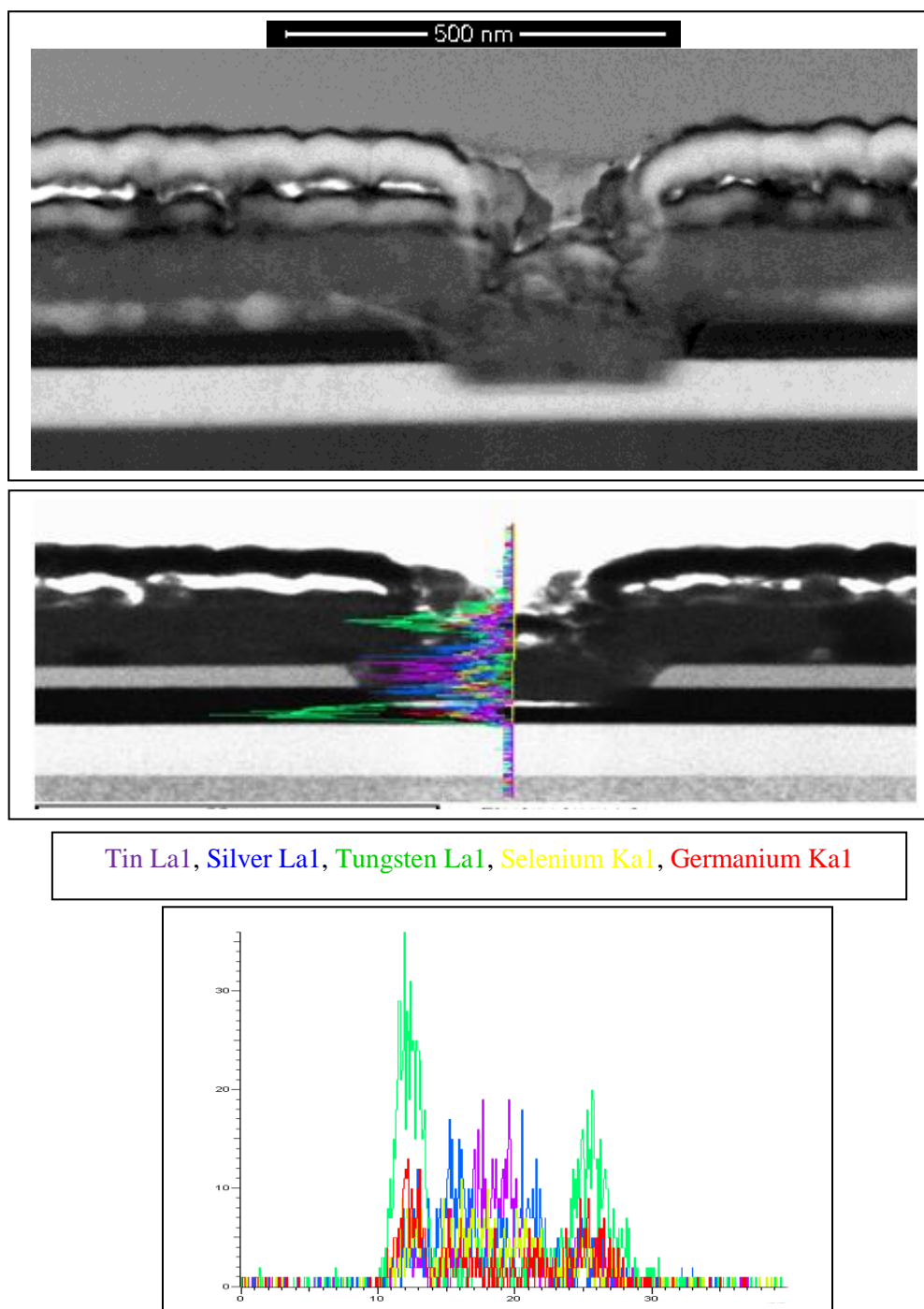
Figure 2.4: SEM and STEM Elemental Mapping of Contact Between the Top and Bottom Electrodes of a Virgin Ge_2Se_3/SnSe/Ag Device. Data Collected at Micron Technology.

The STEM mapping demonstrates the difficulty of using SEM and STEM techniques to investigate structure of ion-conducting devices that use Ag. In all cases, Ag moves easily under the influence of an electron beam. Samples are always compromised during sample prep, as the Ag will move between layers during preparation of a sample with a focused ion beam as well as during imaging. Figure 2.4 shows clearly that silver has migrated throughout the chalcogenide device during imaging in an untested device.

2.3 Fabrication of Ion-Conducting Two-Terminal Devices

The two-terminal devices were fabricated on 200 mm p-type Si wafers. The bottom and top W electrodes and Ag were deposited by sputtering. The bottom electrode received an argon sputter etch prior to chalcogenide deposition to remove any native oxide growth. The Ge_2Se_3 layers were deposited by sputtering with an Ulvac ZX-1000 RF sputtering tool. The remaining materials were purchased from Alfa Aesar with 99.999% purity: GeTe, SnSe, PbSe, Sb_2Se_3, Ag_2Se, and In_2Se_3. These materials were all thermally evaporated using a CHA Industries SE-600-RAP thermal evaporator with a base system pressure of 1×10^{-7} torr. A summary of film compounds and target thicknesses are shown in Table 2.1.

2.4 Chalcogenide Film Choices

Chalcogenide refers to the elements and the materials containing those elements in column six of the periodic table: sulfur (S), selenium (Se), and tellurium (Te). In 1968, Ovshinsky discovered the phase-change resistive switching in the chalcogenide film $Te_{48}As_{30}Si_{12}Ge_{10}$ (9). The switching resistance states of chalcogenide compounds

discovery led to phase-change memory and the compact disk (CD) technology. In 1976, Hirose and Hirose found a reversible resistance switching effect in Ag-photodoped As_2S_3 films (10). This discovery was the catalyst for the later work on ion-conducting resistance-variable devices and ultimately on the device studies in this work.

2.4.1 Metal-Selenide Layer Choices

The metals used for the metal selenide layer were Sb, Sn, Pb, Ag, and In. These metal-selenide materials are readily commercially available and can be thermally evaporated. Under study in this work is an investigation of the involvement, if any, of the metal-ion species in the metal-selenide layer, including whether the metal-ion species affects the formation of a conducting pathway through the chalcogenide glass layer. Any effects would be realized in variations of threshold voltages, resistances, and power requirements for switching between high and low resistance states. Possible methods by which the metal-ion could influence the device's electrical properties include the metal ion assisting in formation of the conductive channel during the first write operation, the metal-ion participating in a redox reaction with the Ag, the metal-ion species drifting with Ag^+ in the electric field, or the steric effects of the metal-selenide species hindering the motion of Ag^+ through the layer.

The theory of a redox reaction involves the transfer of electrons between two different atoms or molecules. A species is reduced when it gains an electron and acts as an oxidizing agent. A species is oxidized when it loses an electron and acts as a reducing agent. A reduction potential is a value that gives the tendency of a species to be reduced.

A species with a higher (more positive) reduction potential will have a tendency to gain

an electron from a species with a lower reduction potential. Table 2.2 lists the standard

reduction potentials of the metals used in an aqueous environment at 25 °C, excluding the

metal Sb (11). The chosen reduction reaction for Sb in an acidic environment at 25 °C is

used due to the lack of a reduction potential of Sb^{3+} in an aqueous environment.

Table 2.2: Table of Standard Reduction Potentials of Metals from Metal-Selenide Layer (11).

Metal	Cathode (Reduction)	Half Reaction Standard Potential E^0 (V)
Ag	$Ag^+ + e^- \leftrightarrow Ag\,(s)$	+0.799
Sb	$Sb_2O_3(s) + 6H^+ + 6e^- \leftrightarrow 2Sb(s) + 3H_2O$	+0.147
Sn^{4+}	$Sn^{4+} + 2e^- \leftrightarrow Sn^{2+}$	+0.139
Pb	$Pb^{2+} + 2e^- \leftrightarrow Pb(s)$	-0.126
Sn^{2+}	$Sn^{2+} + 2e^- \leftrightarrow Sn(s)$	-0.141
In	$In^{3+} + 3e^- \leftrightarrow In(s)$	-0.338

Table 2.2 lists the metals with decreasing reduction potentials from top to bottom.

Since silver has the most positive reduction potential from all of the other metals, silver at

the interface of the two layers will be reduced by each of the metals from the metal-

selenide layer without an applied voltage bias.

The metal ions have the possibility of also drifting with the electric field, just as

Ag^+ does, and of being reduced at the bottom electrode.   It has been shown that Sn from

SnSe migrates into Ge_2Se_3 and GeTe layers with an applied potential bias (12; 13). The oxidized metals could perhaps assist in the formation of the conductive channel.

2.4.2 Germanium-Chalcogenide Layer Choices

The two varying germanium chalcogenides used are GeTe and Ge_2Se_3. The Ge_2Se_3 film was sputtered with a physical vapor deposition target composed of pressed Ge_2Se_3 powder and film is amorphous as deposited. The GeTe was thermally evaporated and is amorphous as deposited. An air break was performed between the GeTe deposition and the subsequent SnSe thermal evaporation deposition to mimic the Ge_2Se_3 exposure to air during transportation from the sputter tool to the thermal evaporator. These two compounds are chosen to compare the role of the chalcogenides (Se vs. Te) and their glass structures and properties on the device switching properties. Both compounds contain homopolar Ge-Ge bonds (6; 14). The Ge-Ge bonds are predicted through models by Edwards and Campbell to break and form new bonds with Ag in a Ge_2Se_3 system (6). Both selenium and tellurium are in the chalcogen family and exhibit similar properties. But they are different in size and that difference influences the electronegativity, bonding, and sterics; and they have different amorphous glass structures and properties. For example, the glass transition temperature of Ge_2Se_3 is greater than 613 K but only 423 K for GeTe thin films (12).

2.5 Electrical Testing Description

DC sweeps using a parameter analyzer to apply a potential across a device and during application of the potential the current through the device was measured. The DC

sweeps were performed using an HP 4156A Semiconductor Parameter Analyzer to provide the DC sweep and resultant IV curve. The compliance currents on the measurement were varied to 'set' the maximum device programming current during testing. Electrical contact was made to the devices by using micromanipulators with W Micromanipulator 7B probe tips to contact the top and bottom electrodes.

An initial programming DC sweep on a virgin device is performed by first applying a positive double sweep, followed by a negative double sweep, followed by a final positive double sweep. This test sequence is referred to as the write/erase/write (W/E/W) cycle. The positive double sweeps were from 0 V to 1 V and back to 0 V with varying compliance currents of 100 nA, 1 µA, 10 µA, 100 µA, and 1 mA, with the bottom electrode grounded. This test is referred to as the 1st write cycle. Immediately following the first positive double sweep, a double sweep from 0 V to -1V and back to 0 V with 1 mA compliance current was performed. The negative sweep is known as the erase cycle. A subsequent positive double sweep with same parameters as the first positive sweep then follows. The second positive DC sweep is referred as the 2nd write cycle. Each W/E/W cycle was performed on virgin devices with a minimum of three to five devices per temperature and compliance current. An example I-V plot showing data for an actual W/E/W cycle is shown in Figure 2.5.
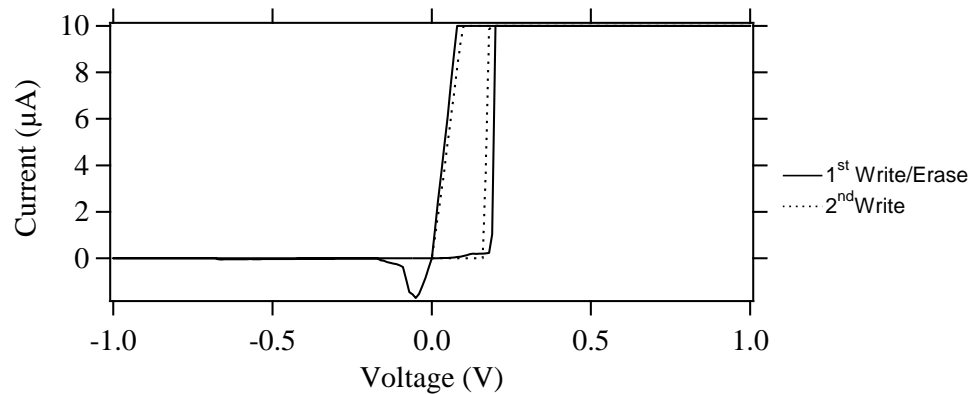
Figure 2.5: Example of Ge₂Se₃/SnSe/Ag Two-Terminal Device Representing a Write/Erase/Write Cycle.

Temperature studies were performed on a temperature controlled wafer stage with an accuracy of ±1 °C on the backside of the wafer; the top of the wafer (the device side) was exposed to ambient. The electrical measurements were taken at temperatures of 23 °C, 50 °C, 100 °C, and 150 °C. The cleaved wafer was placed on the stage, and room temperature (23 °C) measurements were first performed on the two-terminal devices. The wafer remained on the stage while it was heated to the desired temperature, and then the wafer was allowed to equilibrate for a minimum of 15 minutes. After equilibration, the W/E/W cycle was performed on three to five virgin devices for each of the five compliance currents at that temperature. Attempts were made to prevent air cooling on the wafer surface from any air movement in the room.

2.6 Conclusion

In this chapter, the layout and cross-section of the layered chalcogenide two-terminal devices are provided. The choice of materials and fabrication methods were introduced. Lastly, the electrical measurement methodology was provided.

CHAPTER 3: WRITE THRESHOLD VOLTAGE CHARACTERISTICS

3.1 Introduction

This chapter discusses the measured threshold voltages of each of the

chalcogenide ion-conducting devices listed in Table 2.1, as a function of temperature and

programming current (compliance current on the semiconducting parameter analyzer).

The electrical measurements performed are described in Chapter 2. The device threshold

voltages are compared to determine trends due to the various metal-chalcogenide and

germanium-chalcogenide layers. The bars above and below the average values in graphs

are high and low, respectively. The erase thresholds are discussed as power requirements

to erase in Chapter 4.

The activation energies are calculated from the Arrhenius equation and by solving

for activation energy, $E_A = -R \frac{\partial V_{T1}}{\partial \frac{1}{T}}$, where R is Boltzmann's Constant, $k_B = 8.617 \times 10^{-5}$

eV K^{-1}. This approach assumes a first order reaction. The 150 °C V_{T1} value is not used

in this calculation due to the unusual behavior exhibited with these devices at the elevated

temperature (as will be discussed), which is beyond the operating specification

requirements for IC devices. An example plot to obtain the activation energy is seen in

Figure 3.1.
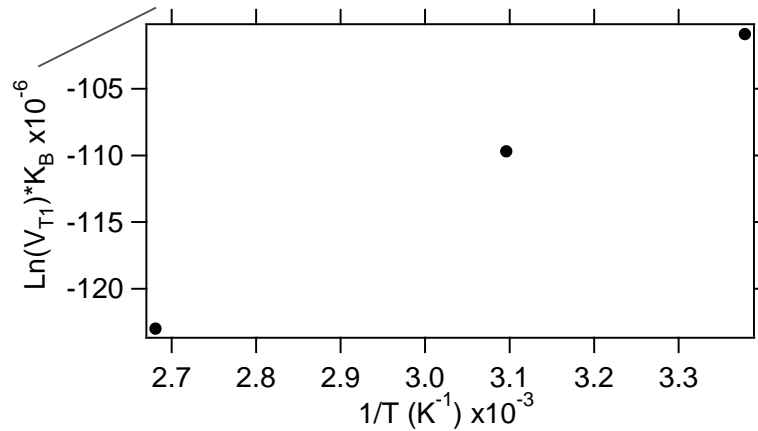
Figure 3.1: Sample Arrhenius Equation Plot for Ge$_2$Se$_3$/Sb$_2$Se$_3$/Ag Device Used in Determining Activation Energy.

The Arrhenius equation plot of Figure 3.1 has a y-axis that is $\ln(V_{T1})*k_B$ and the

x-axis is inverse temperature in Kelvin. The slope of this plot will provide the activation

energy for the electro-deposition of silver through the medium.

For outlier statistical data points, a q-test was performed to determine if the data

point is random or relevant to the data set. The q

value$= \frac{difference\ of\ outlier\ and\ nearest\ data\ point}{range\ of\ data\ set}$ is compared to a critical Q table easily

viewed on the internet or in literature (15). If q is greater than Q$_{critical}$, the suspect

measurement can be rejected; otherwise, it is retained. The q-test is often used for fast

evaluation of small data sets, commonly three to ten measurements (15).

3.2 Compliance Current and Temperature Effects

We begin this section by exploring the compliance current and temperature

effects on the threshold voltage of the write sweeps. When the first programming sweep

is performed on a virgin device and the device is then erased, the threshold voltage of the

second and subsequent writes will differ from the threshold voltage of the first write.

This is likely due to the ease at which the Ag^+ ion can migrate along the conduction pathway that was formed during the first write sweep. The DC sweeps used for the measurements discussed in this section were described in Chapter 2. The DC sweeps performed had compliance currents of 100 nA, 1 µA, 10 µA, 100 µA, and 1mA. The temperatures at which testing was administered were 23 °C, 50 °C, 100 °C, and 150 °C and retested at 23 °C post thermal exposure.

3.2.1 $Ge_2Se_3/Sb_2Se_3/Ag$

The Sb_2Se_3-layered device threshold voltages at each temperature and programming compliance current for the first write (on a virgin device) and the second write (post a single write/erase cycle) are shown in Figure 3.2. Typical values are listed in Table 3.1. Five to six virgin devices were tested at each compliance current and temperature. Post 150 °C, devices remained on the probe station and were allowed to cool over night. The devices were tested approximately 17 hours post 150 °C thermal exposure. Bars above and below the average points provided in Figure 3.2 are the high and low threshold voltage values, not error bars.
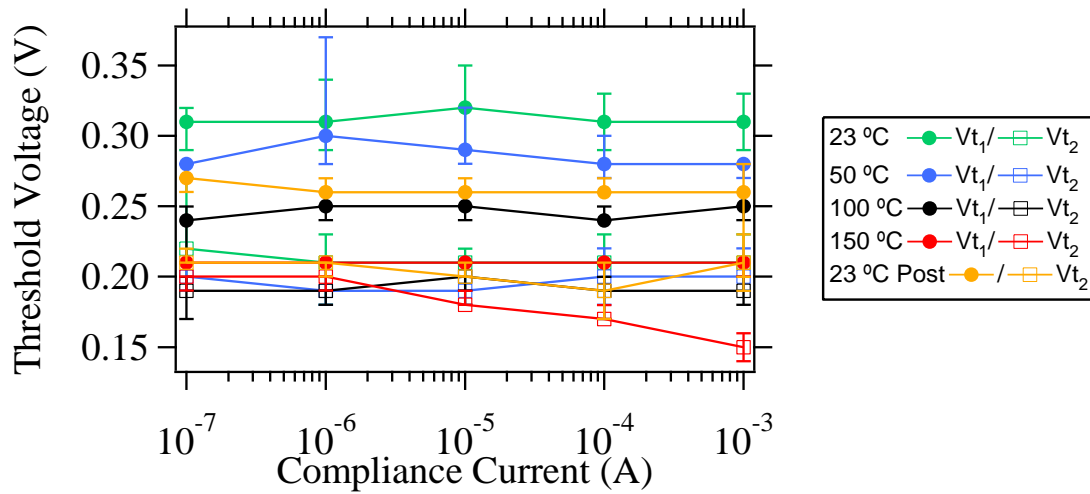
Figure 3.2: Average Write Threshold Voltages of Ge₂Se₃/Sb₂Se₃/Ag Stack Devices versus the Programming Compliance Current at Four Different Temperatures.

Table 3.1: Average Threshold Voltage Values for Ge₂Se₃/Sb₂Se₃/Ag Device at Five Different Programming Currents and Four Different Temperatures.

Programming Current	23 °C V_{T1}/V_{T2} (V)	50 °C V_{T1}/V_{T2} (V)	100 °C V_{T1}/V_{T2} (V)	150 °C V_{T1}/V_{T2} (V)	23 °C Post V_{T1}/V_{T2} (V)
100 nA	0.31/0.22	0.28/0.20	0.24/0.19	0.21/0.20	0.27/0.21
1 µA	0.31/0.21	0.30/0.19	0.25/0.19	0.21/0.20	0.26/0.21
10 µA	0.32/0.21	0.29/0.19	0.25/0.20	0.21/0.18	0.26/0.20
100 µA	0.31/0.21	0.28/0.20	0.24/0.19	0.21/0.17	0.26/0.19
1 mA	0.31/0.21	0.28/0.20	0.25/0.19	0.21/0.15	0.26/0.21

The compliance current had no effect on the threshold voltage as seen by the horizontal lines of Figure 3.2. However, the devices programmed at 150 °C have a slight decrease in V_{T2} after 1 µA programming current whereas V_{T1} remains constant.

The first and second threshold voltages versus temperature are shown in Figure

3.3 and Figure 3.4, respectively.
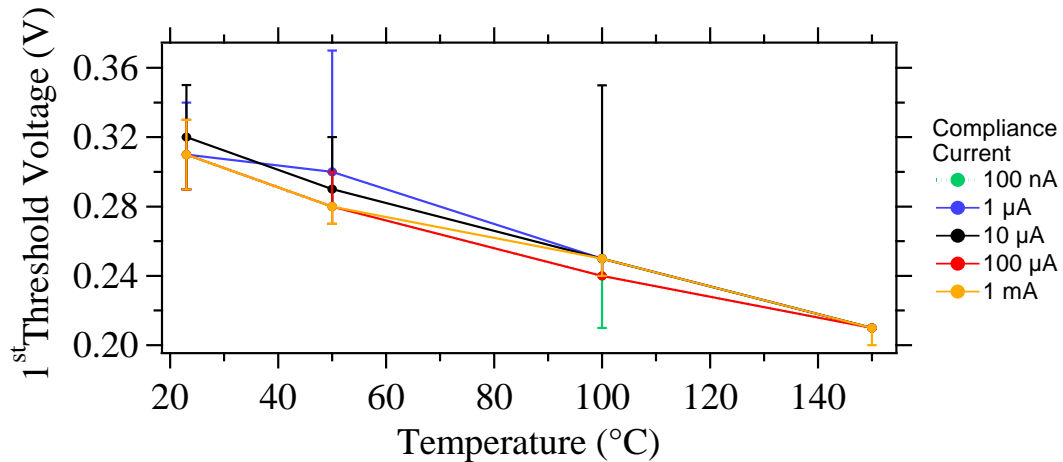
Figure 3.3: First Threshold Voltages of Ge$_2$Se$_3$/Sb$_2$Se$_3$/Ag Stack Devices versus Temperature for Five Different Programming Compliance Currents.
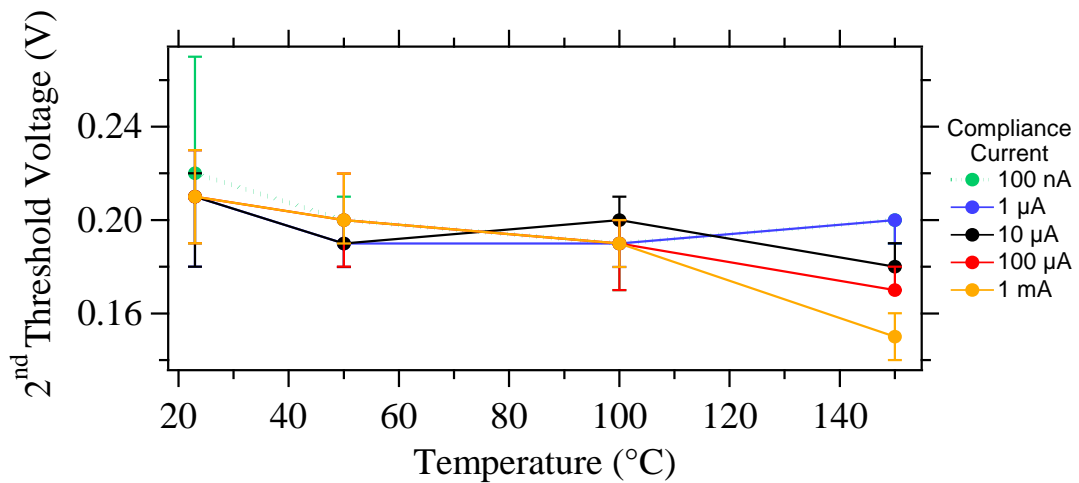
Figure 3.4: Second Threshold Voltages for Ge$_2$Se$_3$/Sb$_2$Se$_3$/Ag Stack Devices versus Temperature for Five Different Programming Compliance Currents.

The V_{T1} of the Sb$_2$Se$_3$ devices decrease with increase in temperature as seen in

Figure 3.3. This is consistent for thermal energy entering the system and yields an

activation energy of 0.032 eV. Within each temperature regime, all programming

currents yielded V_{T1} values within 20 mV of each other as seen in Table 3.1. At 150 °C,

the V_{T1} values differ by up to 50 mV, which indicates some other phenomena is

happening at the elevated temperature.

The V_{T2} seen in Figure 3.4 are much less affected by temperature than the V_{T1}.

However, at 150 °C, the temperature appears to have a greater effect on the V_{T2}, as seen

by the slope of the line from 100 °C to 150 °C. Overall, the V_{T2} are less than the V_{T1}.

The V_{T2} being less than the V_{T1} suggests that the channel was formed on the first write

and on subsequent writes the Ag moves in the same pathway as formed in the first write

cycle (6). The electric field at the threshold voltage at 23 °C is 2 x 10^4 Vcm^{-1}.

The 23 °C post thermal exposure threshold voltages are listed in Table 3.1.

Thermal exposure at 150 °C for 90 minutes lowered V_{T1} by 40-60 mV. This could be

due to structural relaxation of the Ge_2Se_3 (16). V_{T2} was virtually unaffected by the

thermal exposure with most devices having a 23 °C post thermal value of 0.21 V, the

same V_{T2} for pre thermal exposure 23 °C.

3.2.2 Ge_2Se_3/SnSe/Ag

The SnSe-layered device threshold voltages at each temperature and

programming compliance current for the first write (on a virgin device) and the second

write (post a single write/erase cycle) of the same device are shown in Figure 3.5. Three

to five virgin devices were tested at each temperature and compliance current. The

typical threshold voltages are shown in Table 3.2. The devices were exposed at each

temperature for 20 minutes prior to testing to allow time to equilibrate. The devices were

exposed to 150 °C for a total of 45 minutes. Post 150 °C, devices remained on the probe

station, were allowed to slowly cool to 23 °C, and were tested after approximately 4

hours. For each graph provided, bars above and below the average values are high and

low, respectively, not error bars.
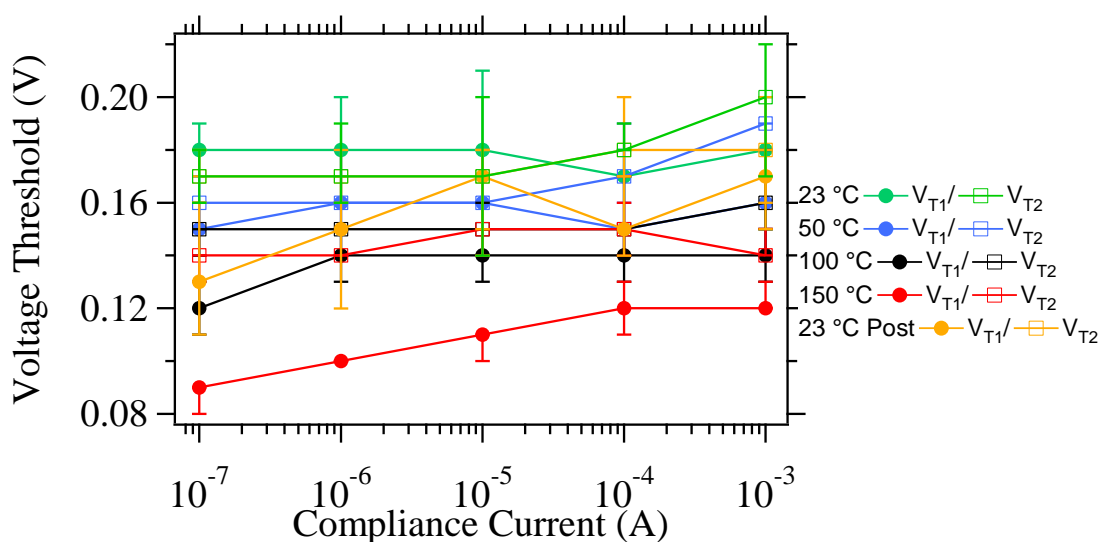
Figure 3.5: Threshold Voltages of Ge$_2$Se$_3$/SnSe/Ag Stack Device versus Compliance Current at Four Temperatures.

The first and second threshold voltages for all five compliance currents are all

very similar in value, centered about 150 mV, as seen in Figure 3.5. The 100 nA

compliance current was reached before a high enough potential could create an electric

field that would write the device into a lower resistance state. The 100 nA programmed

device appears to be 'ON' already during the first write sweep in Figure 3.6. The

subsequent negative sweep erased the device, and the second write sweep has a distinct

V_{T2}. The first and second threshold voltages versus temperature are shown in Figure 3.7

and Figure 3.8, respectively.
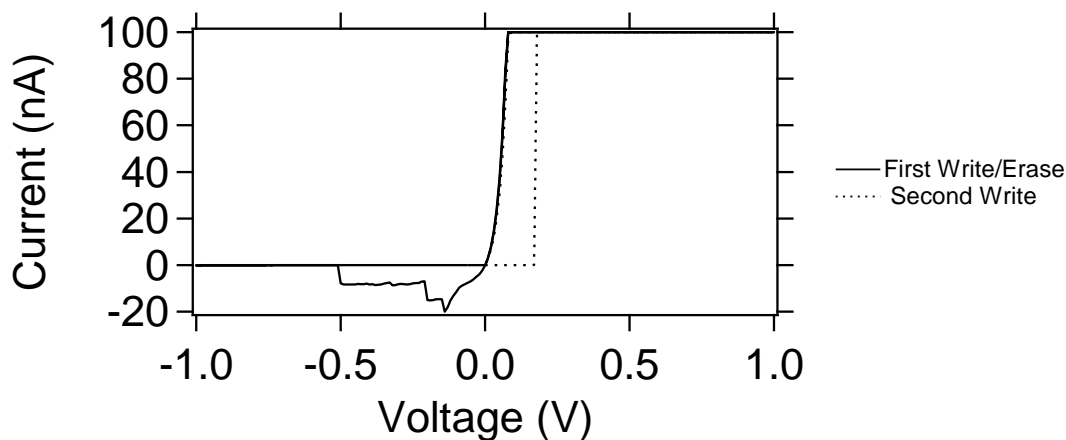
Figure 3.6: Example of Ge$_2$Se$_3$/SnSe/Ag Device Programmed with 100 nA Compliance Current at 23 °C.
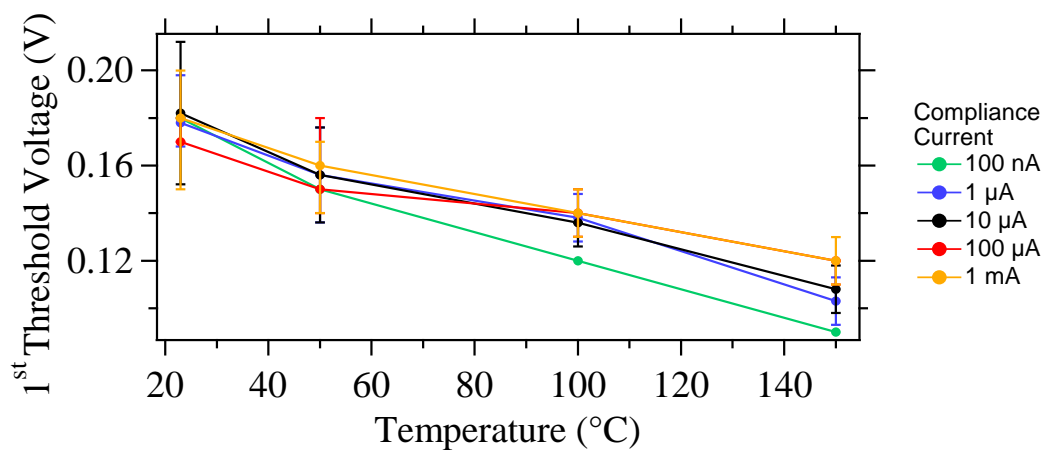
Figure 3.7: First Threshold Voltages of Ge$_2$Se$_3$/SnSe/Ag Stack Devices versus Temperature for Five Different Programming Compliance Currents.
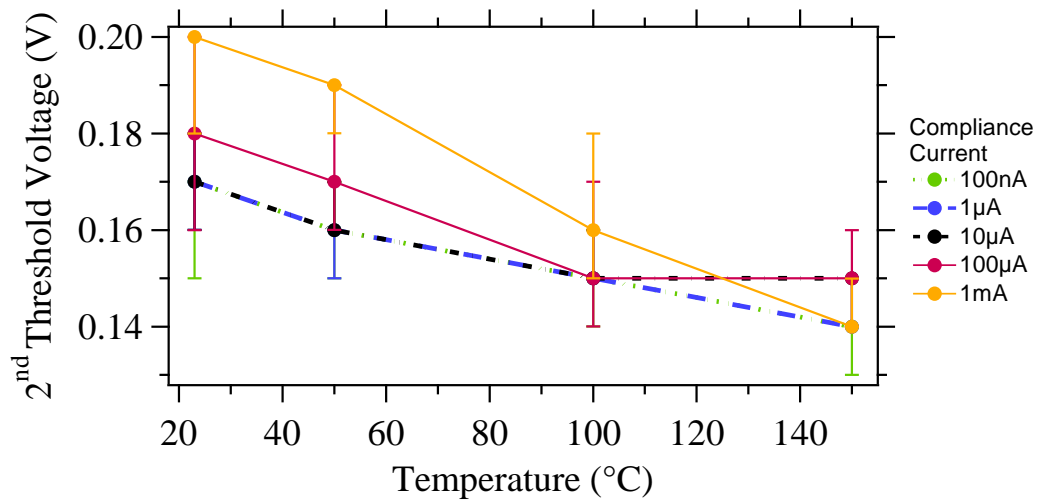
Figure 3.8: Second Threshold Voltages of Ge$_2$Se$_3$/SnSe/Ag Stack Devices versus Temperature for Five Different Programming Compliance Currents.

The V_{T1} decreases with increase in temperature as seen in Figure 3.7 and yields an activation energy of 0.031 eV. When the device achieves the formation of the silver conductive pathway at 23 °C, the electric field is 1.16 x 10^4 Vcm^{-1}. The 23 °C 100 nA compliance current point in Figure 3.7 is the voltage when the compliance current was reached not an actual threshold voltage. The V_{T1} values are within 20 mV of each other among all compliance currents for each temperature regime except at 150 °C. At the higher temperature, the V_{T1} varies up to 40 mV across all compliance currents. The V_{T2} are also affected by temperature as seen in Figure 3.8. As shown in Table 3.2, there is a slight decrease in V_{T2} with an increase in temperature.

Table 3.2: Typical Voltage Threshold Values for Ge$_2$Se$_3$/SnSe/Ag Devices at Five Different Programming Currents and Four Different Temperatures. (-) Represents There Is No Measurable Threshold Voltage

Programming Current	23 °C V_{T1}/V_{T2} (V)	50 °C V_{T1}/V_{T2} (V)	100 °C V_{T1}/V_{T2} (V)	150 °C V_{T1}/V_{T2} (V)	23 °C Post V_{T1}/V_{T2} (V)
100 nA	-/0.17	0.15/0.16	0.12/0.15	0.09/0.14	0.13/0.17
1 µA	0.18/0.17	0.16/0.16	0.14/0.15	0.10/0.14	0.15/0.17
10 µA	0.18/0.17	0.16/0.16	0.14/0.15	0.11/0.15	0.17/0.17
100 µA	0.17/0.18	0.15/0.17	0.14/0.15	0.12/0.15	0.15/0.18
1 mA	0.18/0.2	0.16/0.19	0.14/0.16	0.12/0.14	0.17/0.18

The pre and post thermal exposure average threshold voltages are given in Table 3.2. The thermal exposure during temperature testing appears to have had a small effect on the V_{T1}. The post thermal exposed device had a V_{T1} that was typically 10 mV less than the pre-thermal value. The post 23 °C V_{T2} is same as the 23 °C pre-thermal exposure devices for all compliance currents, so it was unaffected by the thermal exposure.

3.2.3 Ge$_2$Se$_3$/ PbSe/Ag

The PbSe-layered device threshold voltages at each temperature and programming compliance current for the first write (on a virgin device) and the second write (post a single write/erase cycle) of the same device are shown in Figure 3.9. The devices were exposed at each temperature for 20 minutes prior to testing to allow time to equilibrate. The devices were exposed to 150 °C for a total of 47 minutes. Post 150 °C, devices remained on the probe station over night. The devices were allowed to slowly

cool to 23 °C and tested approximately 16 hours after the temperature was reduced from

150 °C. For each graph provided, bars above and below the average values are high and

low, respectively, not error bars.

The first and second threshold voltages are shown in Figures 3.12 and 3.13.   The

voltage when the device reached the compliance current is shown as the threshold voltage

for 100 nA and 1 µA programmed devices in Figures 3.9, 3.12, and 3.13. Those values

are shown on the graph to visually demonstrate that the bias applied was slightly under

that of the other threshold voltages for higher programming currents. Figures 3.10 and

3.11 show the representative device sweeps with 100 nA programming current to

demonstrate the ineffectiveness of programming at such a low compliance current.
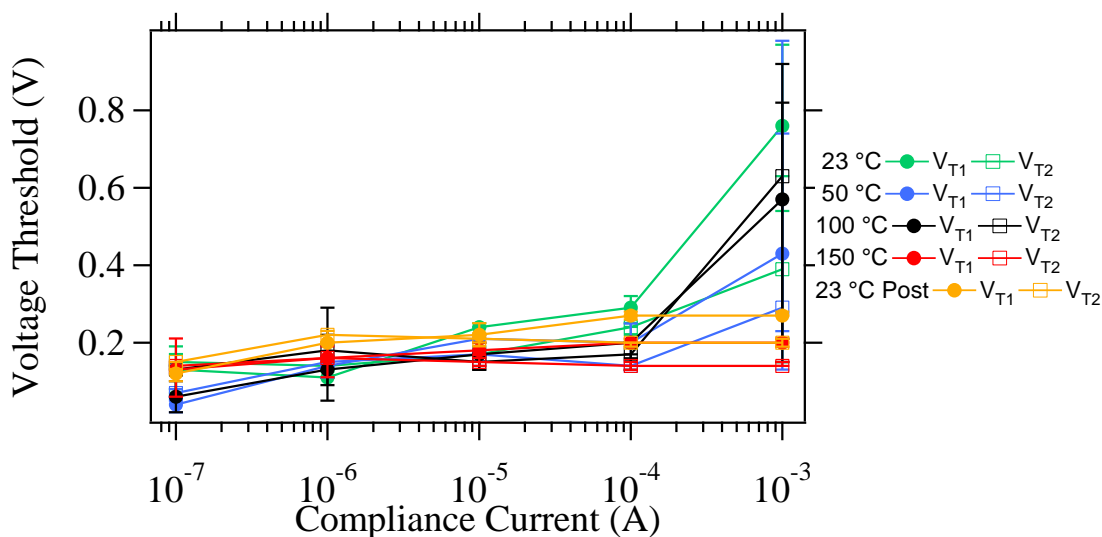
Figure 3.9: Threshold Voltages of Ge$_2$Se$_3$/PbSe/Ag Stack Devices versus Compliance Current at Four Different Temperatures.
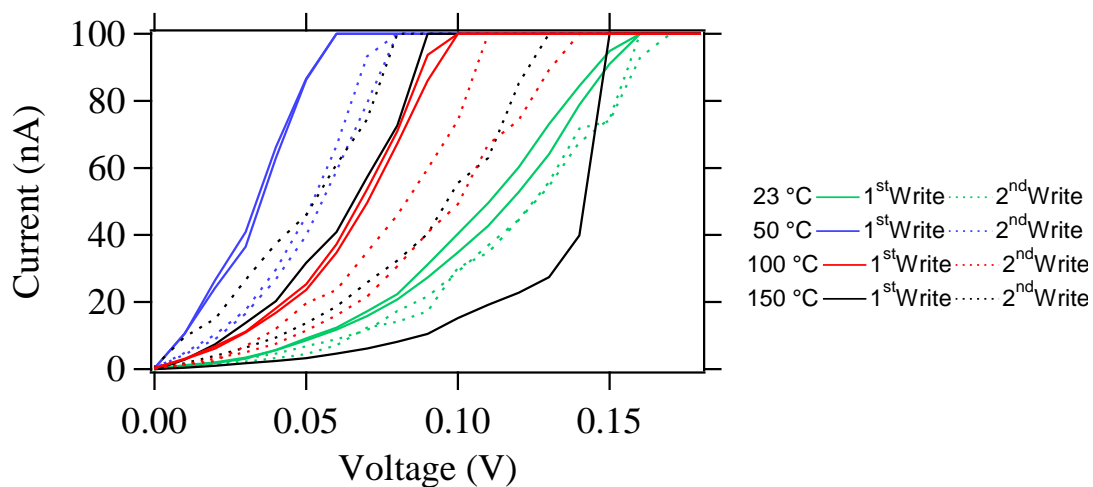
Figure 3.10: Representative IV Write Sweeps of Ge$_2$Se$_3$/PbSe/Ag Virgin Devices Programmed at 100 nA Compliance Current at Four Different Temperatures.
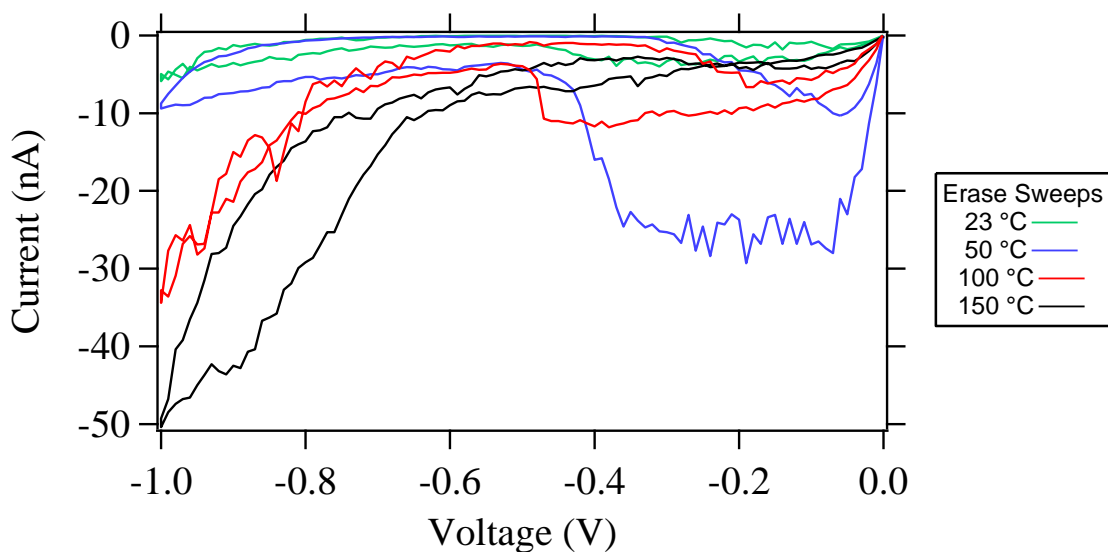
Figure 3.11: Representative IV Erase Sweeps of Ge$_2$Se$_3$/PbSe/Ag Virgin Devices Programmed at 100 nA Compliance Current at Four Different Temperatures.

The 100 nA compliance current was reached before a high enough potential could create an electric field that would write the device into a lower resistance as seen in Figure 3.10. For the higher programming currents that achieved a threshold voltage, the

applied electric field at 23 °C when the silver conductive pathway was formed is 1.27 x

10^4 Vcm^{-1}. The subsequent negative sweep in Figure 3.11 failed to erase the device,

which then created no V_{T2}. The 1 µA programming IV sweeps on virgin devices at 23 °C

are similar to 100 nA programmed devices.

The temperature effects on the first and second threshold voltages are shown in

Figure 3.12 and 3.13, respectively.
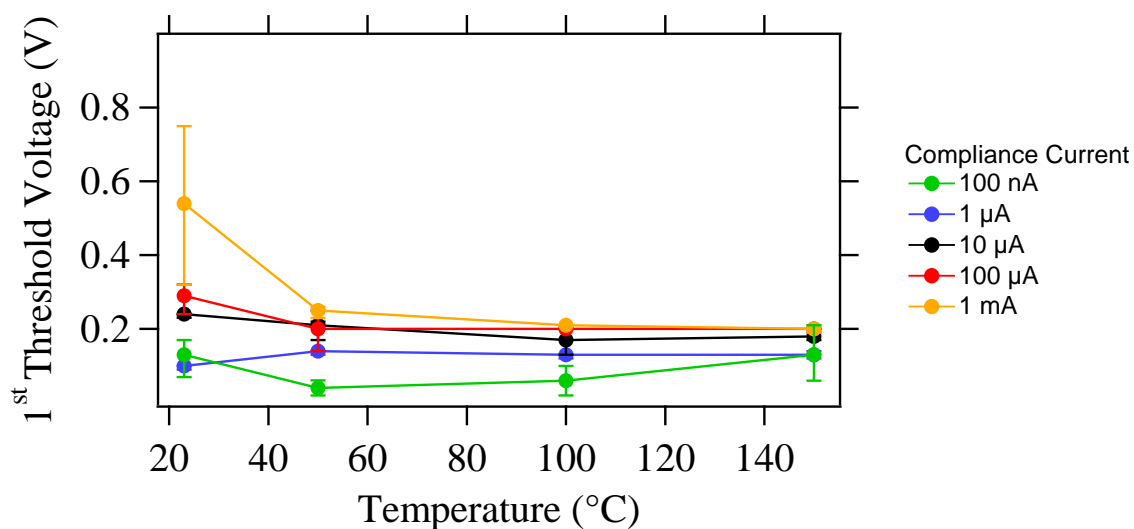
Figure 3.12: First Threshold Voltages of Ge₂Se₃/PbSe/Ag Stack Devices Versus Temperature for Five Different Programming Compliance Currents.
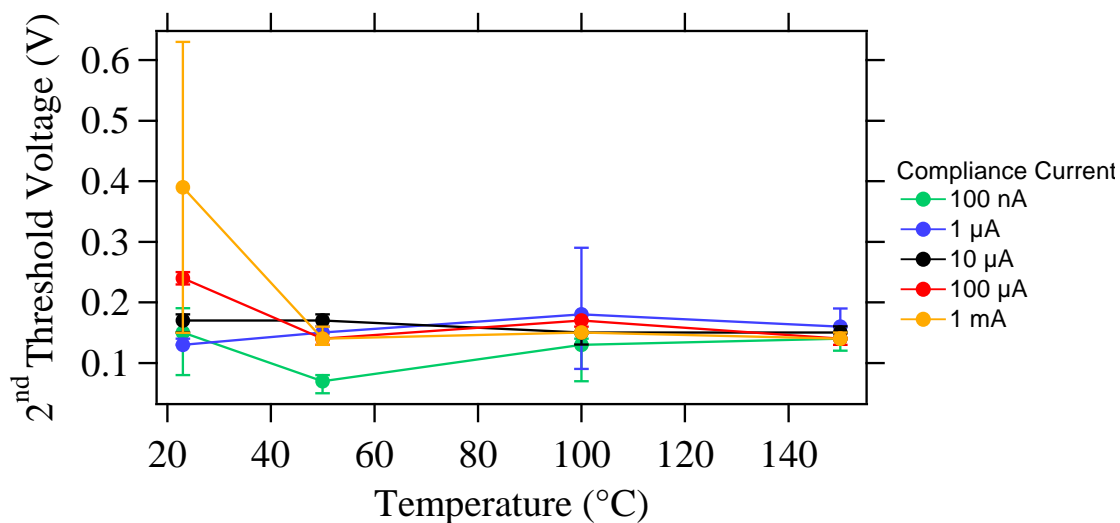
Figure 3.13: Second Threshold Voltages of Ge$_2$Se$_3$/PbSe/Ag Stack Devices Versus Temperature for Five Different Programming Compliance Currents.

The threshold voltages do not significantly decrease from the introduction of thermal energy. There is, however, a variation in threshold values for the 1 mA programmed devices at 23 °C, which is possibly due to contact issues between the probe tip and the remaining photoresist on the top electrode. The second threshold voltages, shown in Figure 3.13, are similar to the first thresholds of Figure 3.12.

The 10 µA, 100 µA, and 1 mA compliance current threshold voltages are consistent across all temperatures as seen in Table 3.3 except for the skewed 1 mA at 23 °C data point. There is an overall decrease in V$_{T1}$ values with increased temperature for 10 µA , 100 µA, and 1 mA devices that yield an activation energy of 0.044 eV.

Table 3.3: Typical Voltage Threshold Values for Ge$_2$Se$_3$/PbSe/Ag Device at Five Different Programming Currents and Four Different Temperatures. (-) Signifies There Was No Threshold Voltage. (*) Signifies Voltage When Compliance Current Was Reached.

Programming Current	23 °C V_{T1}/V_{T2} (V)	50 °C V_{T1}/V_{T2} (V)	100 °C V_{T1}/V_{T2} (V)	150 °C V_{T1}/V_{T2} (V)	23 °C Post V_{T1}/V_{T2} (V)
100 nA	-/-	-/-	-/-	-/-	-/-
1 µA	-/-	0.14*/0.15*	0.13*/0.18*	0.16*/0.16*	0.20*/0.22*
10 µA	0.24/0.17	0.21/0.17	0.17/0.15	0.18/0.15	0.22/0.21
100 µA	0.29/0.24	0.20/0.14	0.20/0.17	0.20/0.14	0.27/0.20
1 mA	0.54/0.39	0.25/0.14	0.21/0.15	0.20/0.14	0.27/0.20

The pre and post thermal exposure threshold voltage values are listed in Table 3.3. The thermal exposure did not significantly affect V_{T1} or V_{T2} of virgin devices. The lower V_T's of the 1 mA post thermal exposure suggests that the high threshold value seen at 23 °C is potentially not normal device behavior.

3.2.4 Ge$_2$Se$_3$/Ag$_2$Se/Ag

The Ag$_2$Se layered device threshold voltages at each temperature and programming compliance current for the first write (on a virgin device) and the second write (post a single write/erase cycle) of the same device are discussed in this section and shown in Figure 3.14. Three to five virgin devices were tested at each temperature and compliance current. The devices were exposed at each temperature for 20 minutes prior to testing to allow time to equilibrate. The devices were exposed to 150 °C for a total of 45 minutes. Post 150 °C, devices remained on the probe station and were allowed to cool

to 23 °C, and were tested approximately 4 hours later. For each graph provided, bars

above and below the average values are high and low, respectively, not error bars.
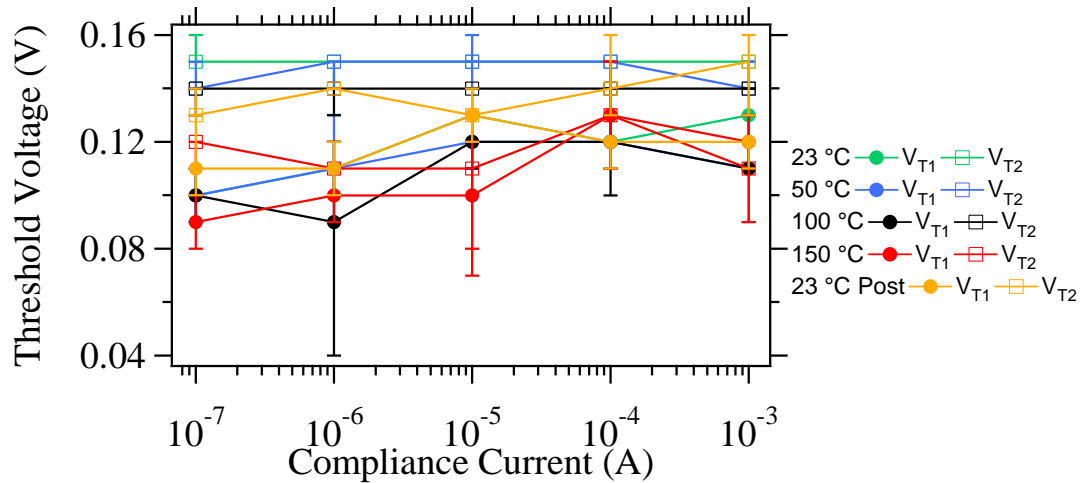
**Figure 3.14: Threshold Voltages of Ge₂Se₃/Ag₂Se/Ag Stack Devices Versus
Temperature for Five Different Compliance Currents.**

The threshold voltages are fairly constant across all compliance currents as seen

in Figure 3.14. There is one extreme low V_{T1} outlier at 100 °C of 0.04 V for a 1 μA

programmed device also seen in Figure 3.14. The single bit devices are very sensitive to

electrostatic discharge and possibly the outlier had received a surge of charge from

placement of the probe tips onto to the electrodes.

The first and second threshold voltages are compared at four different

temperatures in Figure 3.15 and Figure 3.16, respectively.
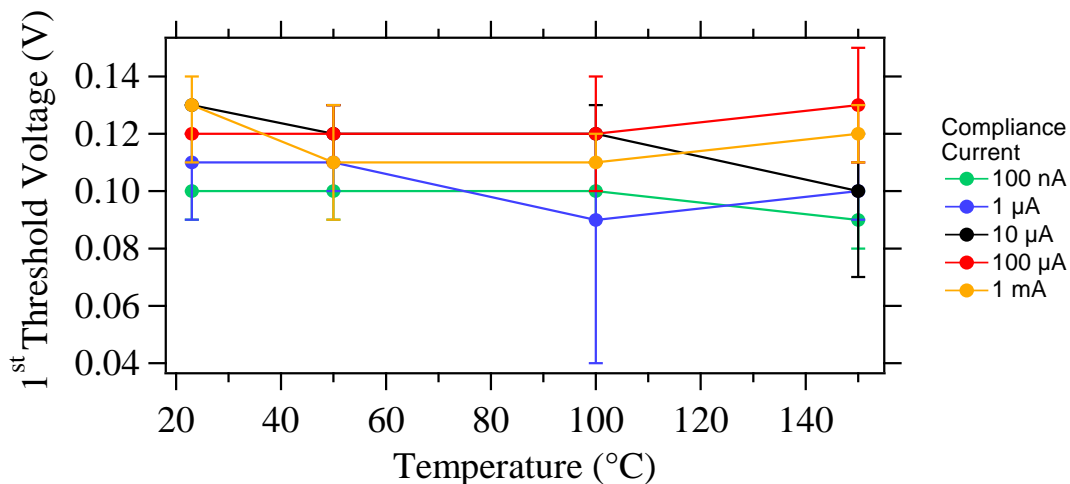
Figure 3.15: First Threshold Voltages of Ge₂Se₃/Ag₂Se/Ag Stack Devices Versus Temperature for Five Different Compliance Currents.
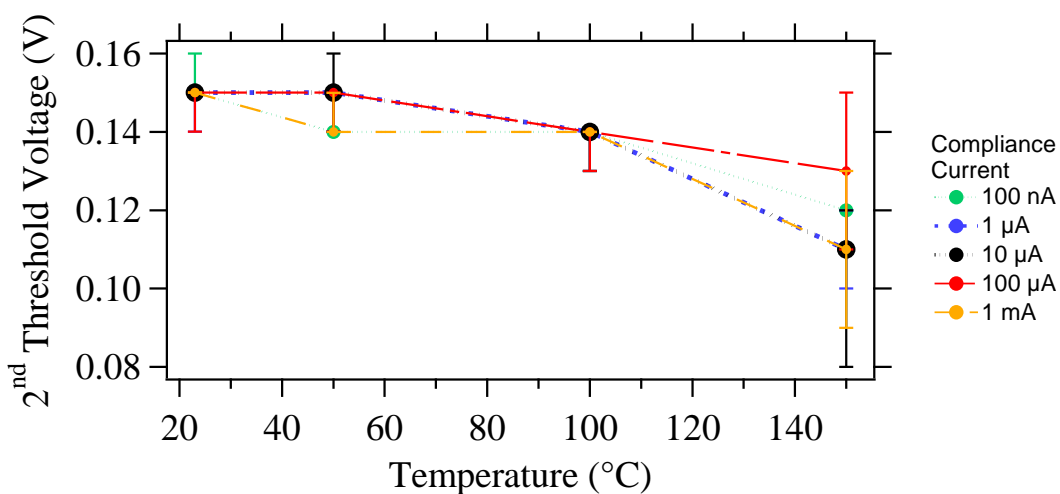
Figure 3.16: Second Threshold Voltages of Ge₂Se₃/Ag₂Se/Ag Stack Devices Versus Temperature for Five Different Compliance Currents.

The Ag_2Se stack has V_{T1} that are all below 150 mV, as seen in Figure 3.15 and

Table 3.4. The V_{T1} decrease slightly with increase in temperature and are consistent

within 20 mV across all temperatures at all compliance currents. This yields an

activation energy of 0.020 eV. The electric field when the silver conductive pathway

bridges the two electrodes at 23 °C is 8.39 x 10^3 Vcm^{-1}.

The V_{T2} are more susceptible to temperature effects at 150 °C compared to the

lower temperatures, decreasing by 30 mV from the 100 °C V_{T2} values. The V_{T2} is also

higher than the V_{T1} for all compliance currents at all temperatures except for 1 mA at 150

°C, which is 10 mV less than V_{T1}.

Table 3.4: Average Threshold Voltage Values for Ge$_2$Se$_3$/Ag$_2$Se/Ag Devices as a Function of Compliance Current and Temperature.

Programming Current	23 °C V_{T1}/V_{T2} (V)	50 °C V_{T1}/V_{T2} (V)	100 °C V_{T1}/V_{T2} (V)	150 °C V_{T1}/V_{T2} (V)	23 °C Post V_{T1}/V_{T2} (V)
100 nA	0.10/0.15	0.1/0.14	0.10/0.14	0.09/0.12	0.11/0.14
1 μA	0.11/0.15	0.11/0.15	0.09/0.14	0.10/0.11	0.12/0.14
10 μA	0.13/0.15	0.12/0.15	0.12/0.14	0.10/0.11	0.13/0.14
100 μA	0.12/0.15	0.12/0.15	0.12/0.14	0.13/0.13	0.12/0.16
1 mA	0.13/0.15	0.11/0.14	0.11/0.14	0.12/0.11	0.12/0.16

The Ag$_2$Se layer virgin devices were not affected by 150 °C thermal exposure.

The post 23 °C V_T values are similar to the 23 °C pre-thermal exposed devices, changing

only 10 mV at most as compared in Table 3.4.

3.2.5 Ge$_2$Se$_3$/In$_2$Se$_3$/Ag

The In$_2$Se$_3$ layered device threshold voltages at each temperature and

programming compliance current for the first write (on a virgin device) and the second

write (post a single write/erase cycle) of the same device are discussed. Six virgin

devices were tested at each temperature and compliance current. The devices were

exposed at each temperature for 20 minutes prior to testing to allow time to equilibrate.

The devices were exposed to 150 °C for a total of 55 minutes. Post 150 °C, devices

remained on the probe station and were allowed to slowly cool to 23 °C overnight.

Devices were tested after approximately 18 hours. For each graph provided, bars above

and below the average values are high and low, respectively, not error bars.

The first and second threshold voltages are shown across five compliance currents

in Figure 3.17. The first and second threshold voltages are also shown across the four

temperatures in Figure 3.18 and Figure 3.19, respectively, for easy comparison of thermal

effects.
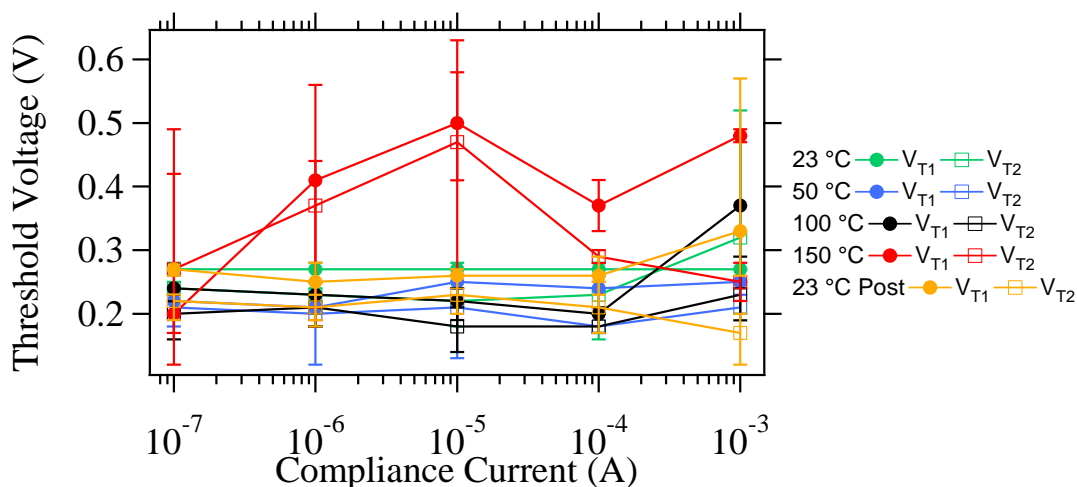
Figure 3.17: Threshold Voltages of Ge₂Se₃/In₂Se₃/Ag Stack Devices Versus Temperature for Five Different Compliance Currents.

Both first and second threshold voltages are consistent across all compliance

currents except for devices programmed at 150 °C. The threshold voltages at the elevated

temperature range from 200 mV to 600 mV, as seen in Figure 3.17. The bottom

electrode pads had a residual film that smeared at the higher temperature during probing.

This residue probably increased the resistance between the probe tip and electrode,

requiring additional potential to create the conductive pathway.
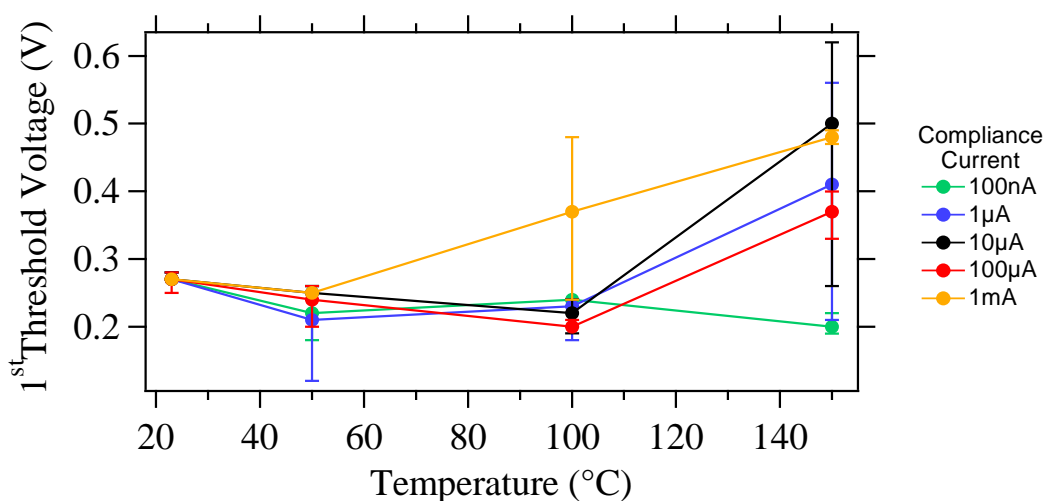
Figure 3.18: Average First Threshold Voltages of Ge_2Se_3/In_2Se_3/Ag Stack Devices Versus Temperature for Five Different Compliance Currents.

The In_2Se_3 V_{T1} exhibits a decrease with increase in temperature up to 100 °C, as

seen in Figure 3.18, and yields an activation energy of 0.024 eV. The electric field at the

point of a silver conductive path formation at 23 °C was 1.74 x 10^4 Vcm^{-1}. At 100 °C,

the 1 mA programmed devices have a much greater range in values, which causes an

overall increase in the average value. The 1 mA devices were the last to be programmed

within each temperature, and contact issues between probe tip and bottom electrode were

noticed.   The first threshold voltage increased more at 150 °C. The 100 nA devices

remained consistent across all temperatures. The remaining programmed devices of 1

μA, 10 μA, 100 μA, and 1 mA compliance currents had V_{T1}'s that increased at 150 °C.

There are likely additional phenomena that take place at the elevated temperature of 150 °C.
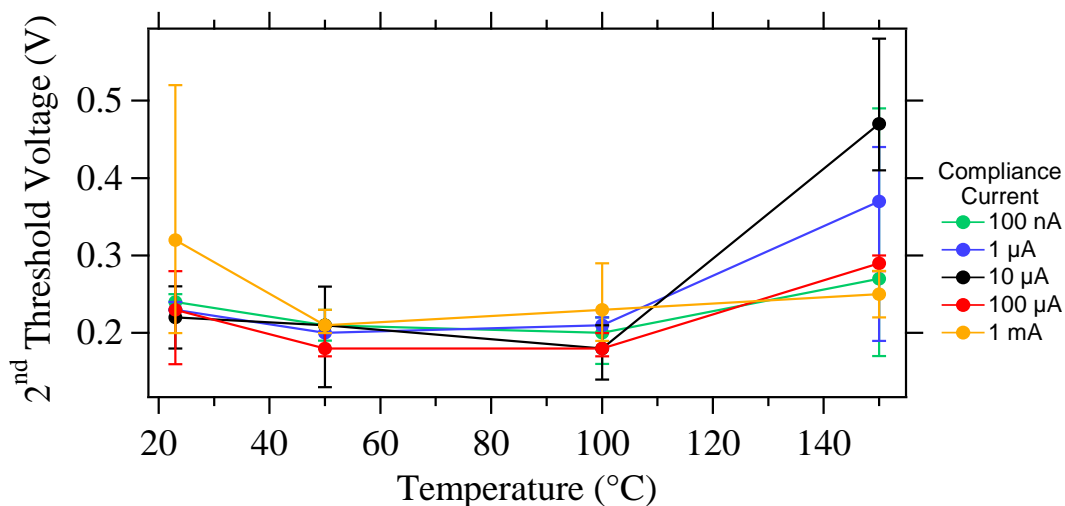
Figure 3.19: Average Threshold Voltages of Ge$_2$Se$_3$/In$_2$Se$_3$/Ag Stack Devices Versus Temperature for Five Different Compliance Currents.

The second threshold voltages were consistent up through 100 °C, as seen in

Figure 3.19. The 23 °C 1 mA compliance current test is skewed by one high data point

of 0.52 V when the typical value is 0.22 V, as listed in Table 3.9. The high outlier can't

be removed by a q-test. At 150 °C, all V_{T2}'s increased, similar to the V_{T1}. All second

threshold voltages are less than the first threshold voltages except for 100 nA at 150°C.

Figure 3.19 shows an average of 0.27 V whereas Table 3.5 shows the V_{T2} value at 150 °C

as 0.18 V. The difference is due to the fact that two of the six devices had high V_{T2} at

0.49 V, 0.41 V and the remaining four had an average of 0.18 V. The two high values

seem to be the result of contact issues between probe tip and electrodes.

Table 3.5: Typical Threshold Voltage Values for $Ge_2Se_3/In_2Se_3/Ag$ Device as a Function of Temperature and Programming Compliance Current.

Programming Current	23 °C V_{T1}/V_{T2} (V)	50 °C V_{T1}/V_{T2} (V)	100 °C V_{T1}/V_{T2} (V)	150 °C V_{T1}/V_{T2} (V)	23 °C Post V_{T1}/V_{T2} (V)
100 nA	0.27/0.24	0.22/0.21	0.24/0.20	0.21/0.18	0.27/0.22
1 µA	0.27/0.23	0.21/0.20	0.23/0.21	0.41/0.37	0.25/0.21
10 µA	0.27/0.22	0.25/0.21	0.22/0.18	0.50/0.47	0.26/0.23
100 µA	0.27/0.23	0.24/0.18	0.20/0.18	0.37/0.29	0.26/0.21
1 mA	0.27/0.22	0.25/0.21	0.37/0.23	0.48/0.25	0.27/0.17

The exposure to the temperature during testing did affect the virgin devices by a reduction of approximately 20 mV for both first and second threshold voltages. This could be the result of relaxation of the Ge_2Se_3 film (16). The values are listed in Table 3.5.

3.2.6 GeTe/SnSe/Ag

The GeTe/SnSe/Ag-layered device threshold voltages at each temperature and programming compliance current for the first write (on a virgin device), and the second write (post a single write/erase cycle) of the same device are discussed below and values are shown in Figure 3.20. Five virgin devices were tested at each temperature and compliance current. The devices were exposed at each temperature for 20 minutes prior to testing to allow time to equilibrate. The devices were exposed to 150 °C for a total of 50 minutes. Post 150 °C, devices remained on the probe station and were allowed to slowly cool to 23 °C, and were tested after approximately 5 hours. For each graph

provided, bars above and below the average values are high and low, respectively, not error bars.
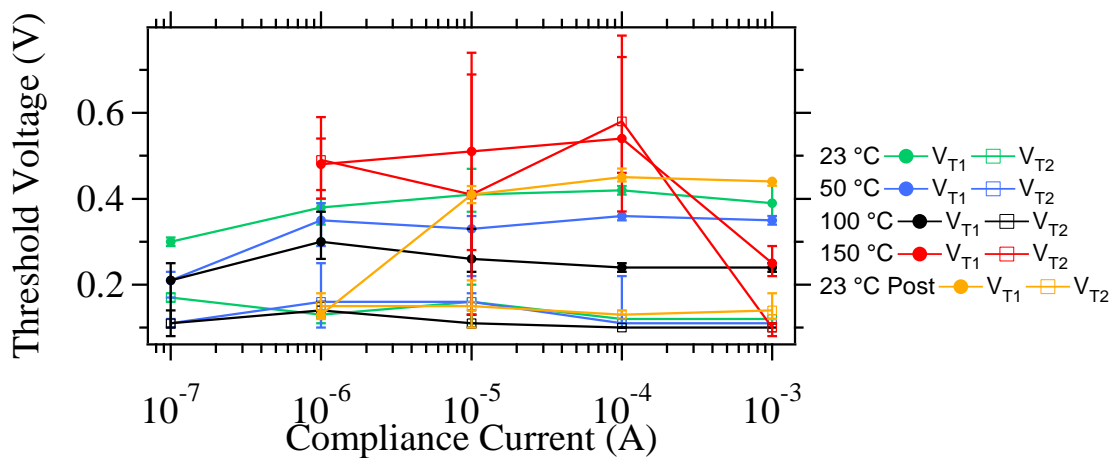
Figure 3.20: Threshold Voltages of GeTe/SnSe/Ag Stack Devices Versus Temperature for Five Different Compliance Currents.

Figure 3.21 and Figure 3.22 are first and second threshold voltages versus four temperatures.
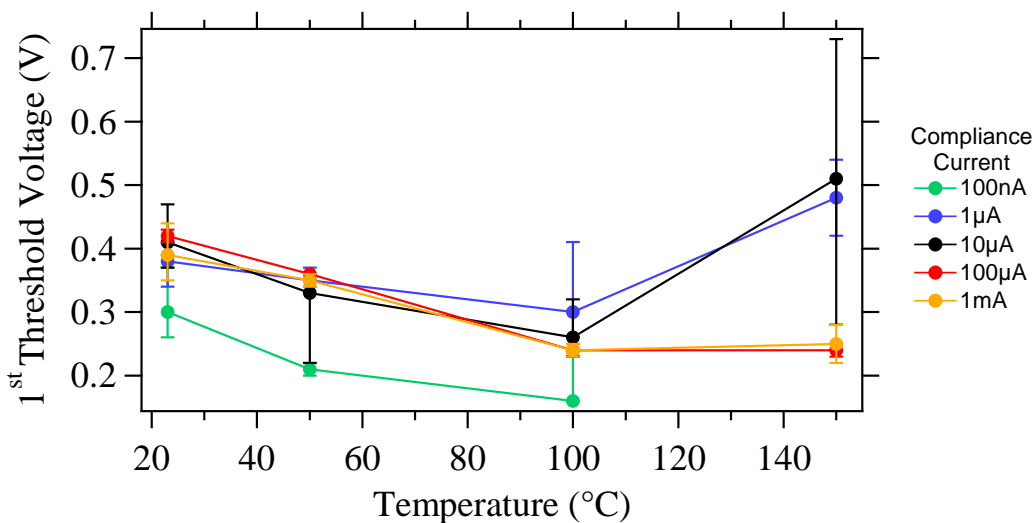
Figure 3.21: First Threshold Voltages of GeTe/SnSe/Ag Stack Devices Versus Temperature for Five Different Compliance Currents.

The GeTe/SnSe stack devices that programmed into a low resistance had a decrease in V_{T1} with increased temperature as seen in Figure 3.21, and yields an activation energy of 0.059 eV. The V_{T1} of 1 µA and 10 µA programmed current devices decreased with temperature until 150 °C, at which time the V_T increased by 80 mV and 250 mV, respectively. At 150 °C, the 100 nA compliance current did not allow a large enough applied potential to reach a threshold voltage; and with an insufficient erase there is no V_{T2}. The 100 nA compliance current devices did switch from high to low resistance states at lower temperatures but were not fully written so there is no sharp current increase. A representative IV plot of a 100 nA programmed device is shown in Figure 3.22. In Figure 3.22, the bottom plot is a zoomed in region of the write sweeps. The 100 nA behaves the same as the 1 µA but does not reach a threshold voltage due to the compliance current. The 100 nA programmed device's V_T shown in figures and tables are the voltage at which the compliance current was reached.
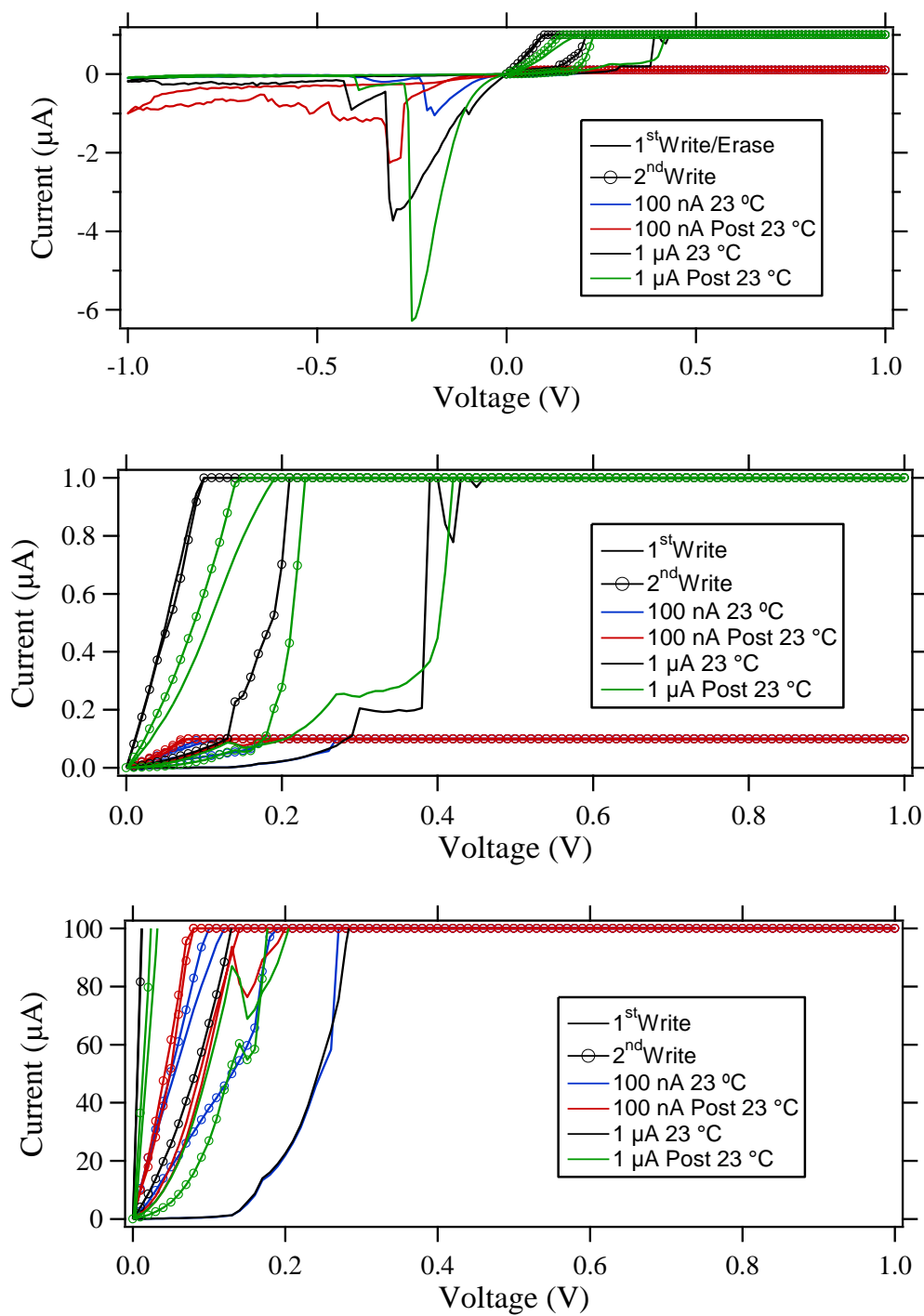
**Figure 3.22: Representative IV Curves of GeTe/SnSe/Ag Stack Devices
Programmed at 100nA and 1µA: Top – Full Scale; Middle – Zoomed in 1 µA;
Bottom – Zoomed in 100 nA.**
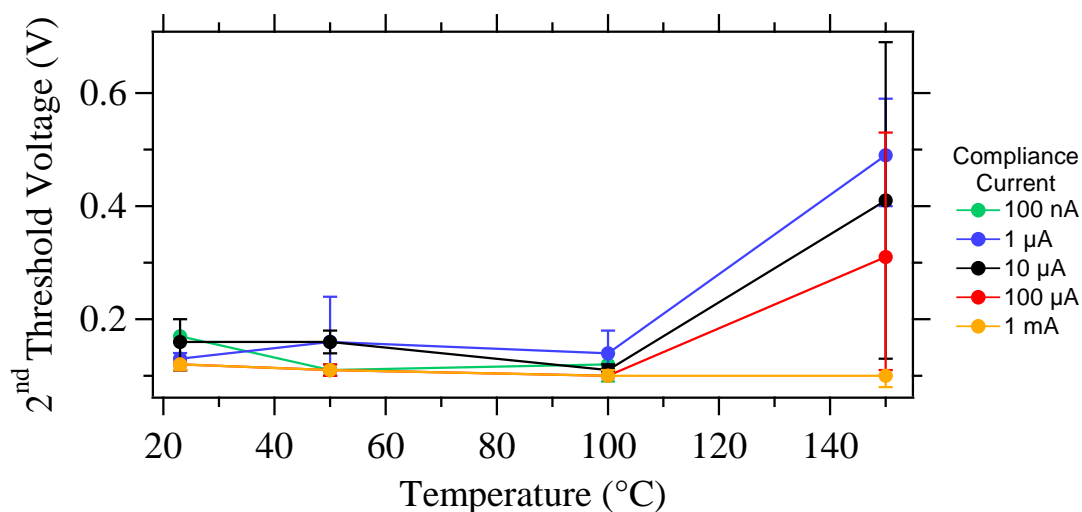
Figure 3.23: Second Threshold Voltages of GeTe/SnSe/Ag Stack Devices Versus Temperature for Five Different Compliance Currents.

The second threshold voltages remained fairly consistent across the temperature range. The 100 nA compliance current V_{T2} data point at 150 °C is absent due to an insufficient erase that would have put the device into a lower resistance state. At 150 °C, the 1 μA, 10 μA, and 100 μA programmed devices had a change in the second threshold voltages by 350 mV, 300 mV, and 480 mV, respectively. The 1 mA devices programmed at 150 °C did not reach the compliance current but still switched between a high and low resistance state. An IV plot is shown in Figure 3.24 of a representative device. At the elevated temperature of 150 °C, there are additional interactions causing unusual device behavior.
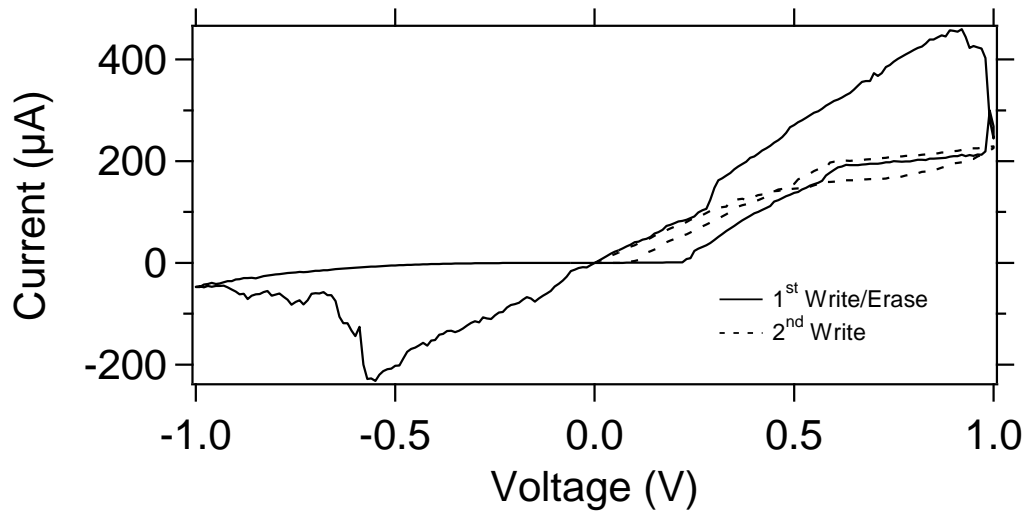
Figure 3.24: IV Curves of a Virgin GeTe/SnSe/Ag Stack Device at 150 °C with 1 mA Compliance Current.

Table 3.6: Average Threshold Voltage Values for GeTe/SnSe/Ag Devices as a Function of Programming Current and Temperature. (*) Signifies the Voltage When Compliance Current Was Reached. (-) No Threshold Voltage

Programming Current	23 °C V_{T1}/V_{T2} (V)	50 °C V_{T1}/V_{T2} (V)	100 °C V_{T1}/V_{T2} (V)	150 °C V_{T1}/V_{T2} (V)	23 °C Post V_{T1}/V_{T2} (V)
100 nA	0.30*/0.17	0.21*/0.11	0.16*/0.12	-/-	-/-
1 µA	0.38/0.13	0.35/0.16	0.30/0.14	0.38/0.49	0.42*/0.15
10 µA	0.41/0.16	0.33/0.16	0.26/0.11	0.51/0.41	0.41/0.15
100 µA	0.42/0.12	0.36/0.11	0.24/0.10	0.54*/0.58*	0.45/0.13
1 mA	0.39/0.12	0.35/0.11	0.24/0.10	0.25/0.10	0.44/0.14

The post thermal 23 °C virgin devices did not reach the threshold voltage with a compliance current of 100 nA and did not erase the device into a higher resistance that

could produce a V_{T2}, as seen in Table 3.6. The V_{T1} of the 1 mA programmed devices were most affected by the thermal exposure, increasing by 50 mV.

The post thermal exposure second threshold voltages are very similar to the pre-thermal exposure devices, only increasing by 10-20 mV. Representative IV write sweep plots of 100 nA and 1 μA programmed devices, pre and post thermal exposure, are shown in Figure 3.22. The middle graph is a close up to show the 1 μA programmed device, and the bottom graph is a close up to show the 100 nA programmed device in greater detail. Both 1 μA and 100 nA devices have the same initial behaviors.

3.3 Comparison of Metal-Selenide Layers

The threshold voltages for the Ge_2Se_3-based devices do vary depending on the metal-selenide layer as shown in Table 3.7 and Table 3.8. From highest to lowest, V_{T1} are devices with the metal layers: Sb_2Se_3, In_2Se, PbSe, SnSe, and Ag_2Se with values of 0.31 V, 0.27 V, 0.24 V, 0.18 V, and 0.13 V, respectively. The PbSe-layered devices typically appeared in the low resistance state initially and, thus, did not allow accurate determination of V_{T1}. The V_{T2} do not follow the same trend as the first voltage threshold. From greatest to least, V_{T2} are devices with the metal layers: In_2Se, Sb_2Se_3, PbSe, SnSe, and Ag_2Se with values of approximately 0.24 V, 0.21 V, 0.17 V, 0.17 V, and 0.15 V.

Table 3.7: Typical Voltage Threshold Values for All Metal-Selenide Devices at Five Different Programming Currents and Four Different Temperatures. (-) No Threshold Voltage, (*) Signifies Voltage When Compliance Current Was Reached.

| Programming Current | Sb_2Se_3 | | | | V_{T1}/V_{T2} (V) |
	V_{T1}/V_{T2} (V) at 23 °C	V_{T1}/V_{T2} (V) at 50 °C	V_{T1}/V_{T2} (V) at 100 °C	V_{T1}/V_{T2} (V) at 150 °C	Post at 23°C
100 nA	0.31/0.22	0.28/0.20	0.24/0.19	0.21/0.20	0.27/0.21

Programming Current	V_{T1}/V_{T2} (V) at 23 °C	V_{T1}/V_{T2} (V) at 50 °C	**Sb₂Se₃** V_{T1}/V_{T2} (V) at 100 °C	V_{T1}/V_{T2} (V) at 150 °C	V_{T1}/V_{T2} (V) Post at 23°C
1 µA	0.31/0.21	0.30/0.19	0.25/0.19	0.21/0.20	0.26/0.21
10 µA	0.32/0.21	0.29/0.19	0.25/0.20	0.21/0.18	0.26/0.20
100 µA	0.31/0.21	0.28/0.20	0.24/0.19	0.21/0.17	0.26/0.19
1 mA	0.31/0.21	0.28/0.20	0.25/0.19	0.21/0.15	0.26/0.21
Programming Current	V_{T1}/V_{T2} (V) at 23 °C	V_{T1}/V_{T2} (V) at 50 °C	**SnSe** V_{T1}/V_{T2} (V) at 100 °C	V_{T1}/V_{T2} (V) at 150 °C	V_{T1}/V_{T2} (V) Post at 23°C
100 nA	-/0.17	0.15/0.16	0.12/0.15	0.09/0.14	0.13/0.17
1 µA	0.18/0.17	0.16/0.16	0.14/0.15	0.10/0.14	0.15/0.17
10 µA	0.18/0.17	0.16/0.16	0.14/0.15	0.11/0.15	0.17/0.17
100 µA	0.17/0.18	0.15/0.17	0.14/0.15	0.12/0.15	0.15/0.18
1 mA	0.18/0.2	0.16/0.19	0.14/0.16	0.12/0.14	0.17/0.18
Programming Current	V_{T1}/V_{T2} (V) at 23 °C	V_{T1}/V_{T2} (V) at 50 °C	**PbSe** V_{T1}/V_{T2} (V) at 100 °C	V_{T1}/V_{T2} (V) at 150 °C	V_{T1}/V_{T2} (V) Post at 23°C
100 nA	-/-	-/-	-/-	-/-	-/-
1 µA	-/-	0.14[*]/0.15[*]	0.13[*]/0.18[*]	0.16[*]/0.16[*]	0.20*/0.22*
10 µA	0.24/0.17	0.21/0.17	0.17/0.15	0.18/0.15	0.22/0.21
100 µA	0.29/0.24	0.20/0.14	0.20/0.17	0.20/0.14	0.27/0.20
1 mA	0.54/0.39	0.25/0.14	0.21/0.15	0.20/0.14	0.27/0.20
Programming Current	V_{T1}/V_{T2} (V) at 23 °C	V_{T1}/V_{T2} (V) at 50 °C	**Ag₂Se** V_{T1}/V_{T2} (V) at 100 °C	V_{T1}/V_{T2} (V) at 150 °C	V_{T1}/V_{T2} (V) Post at 23°C
100 nA	0.10/0.15	0.1/0.14	0.10/0.14	0.09/0.12	0.11/0.14
1 µA	0.11/0.15	0.11/0.15	0.09/0.14	0.10/0.11	0.12/0.14
10 µA	0.13/0.15	0.12/0.15	0.12/0.14	0.10/0.11	0.13/0.14
100 µA	0.12/0.15	0.12/0.15	0.12/0.14	0.13/0.13	0.12/0.16
1 mA	0.13/0.15	0.11/0.14	0.11/0.14	0.12/0.11	0.12/0.16
Programming Current	V_{T1}/V_{T2} (V) at 23 °C	V_{T1}/V_{T2} (V) at 50 °C	**In₂Se₃** V_{T1}/V_{T2} (V) at 100 °C	V_{T1}/V_{T2} (V) at 150 °C	V_{T1}/V_{T2} (V) Post at 23°C
100 nA	0.27/0.24	0.22/0.21	0.24/0.20	0.21/0.18	0.27/0.22
1 µA	0.27/0.23	0.21/0.20	0.23/0.21	0.41/0.37	0.25/0.21
10 µA	0.27/0.22	0.25/0.21	0.22/0.18	0.50/0.47	0.26/0.23
100 µA	0.27/0.23	0.24/0.18	0.20/0.18	0.37/0.29	0.26/0.21
1 mA	0.27/0.22	0.25/0.21	0.37/0.23	0.48/0.25	0.27/0.17

Table 3.8: Activation Energies and Electric Field at V_{T1} Values of Metal-Selenide Devices.

Device	Activation Energy (eV)	Electric Field at 23 °C (Vcm^{-1})
Sb_2Se_3	0.032	2.0×10^4
SnSe	0.031	1.16×10^4
PbSe	0.044	1.27×10^4
Ag_2Se	0.020	8.39×10^3
In_2Se_3	0.024	1.74×10^4

The threshold voltage is independent of programming current (except when the compliance current limit is reached prior to the threshold voltage, which doesn't allow a determination of the threshold voltage). An increase in temperature reduces the first threshold voltages. The additional thermal energy into the system yielded activation energies listed in Table 3.8. The effect of temperature on threshold voltages appeared greatest with the In_2Se3-based devices at 150 °C. The threshold voltages of the Ag_2Se devices were affected the least by temperature and showed no post thermal exposure effects. The Sb_2Se_3 devices also showed no post thermal exposure effect on the threshold voltages. The minimal change in V_{T2} seen in the devices due to temperature suggests that once the conductive channel has formed, the ions move due to the applied electric field and not from thermal energy.

3.4 Comparison of Germanium-Chalcogenide Layers

The germanium-chalcogenide layer has an impact on the first threshold voltage listed in Table 3.9. The GeTe/SnSe/Ag devices have an average V_{T1} at 23 °C of 400 mV,

which decreases to 240 mV at 100 °C. The GeTe-based devices programmed at 150°C with 1 µA and 10 µA compliance currents increase to approximately 500 mV. The 100 nA compliance current tested devices did not have a threshold voltage at the highest temperature. However, the higher compliance currents remained consistent at the higher temperatures. The Ge_2Se_3/SnSe/Ag devices have an average V_{T1} at 23 °C of 180 mV, which decreases to 110 mV at 150 °C.

The second threshold voltages of both devices are very similar up through 100 °C. At 150 °C, the GeTe devices' second threshold voltage increase by 200-300 mV from the 100 °C values, as seen in Table 3.9. However, the Ge_2Se_3 devices only vary by 60 mV across the entire temperature range. Both devices exhibit minimal post thermal effects on first and second threshold voltages.

Table 3.9: Typical Voltage Threshold Values for GeTe/SnSe/Ag and Ge₂Se₃/SnSe/Ag Devices as a Function of Temperature and Compliance Programming Current. (*) Signifies the Voltage When Compliance Current Was Reached. (-) No Threshold Voltage.

Programming Current	V_{T1}/V_{T2} (V) at 23 °C	V_{T1}/V_{T2} (V) at 50 °C	Ge₂Se₃ V_{T1}/V_{T2} (V) at 100 °C	V_{T1}/V_{T2} (V) at 150 °C	V_{T1}/V_{T2} (V) Post at 23°C
100 nA	-/0.17	0.15/0.16	0.12/0.15	0.09/0.14	0.13/0.17
1 µA	0.18/0.17	0.16/0.16	0.14/0.15	0.10/0.14	0.15/0.17
10 µA	0.18/0.17	0.16/0.16	0.14/0.15	0.11/0.15	0.17/0.17
100 µA	0.17/0.18	0.15/0.17	0.14/0.15	0.12/0.15	0.15/0.18
1 mA	0.18/0.2	0.16/0.19	0.14/0.16	0.12/0.14	0.17/0.18
Programming Current	V_{T1}/V_{T2} (V) at 23 °C	V_{T1}/V_{T2} (V) at 50 °C	GeTe V_{T1}/V_{T2} (V) at 100 °C	V_{T1}/V_{T2} (V) at 150 °C	V_{T1}/V_{T2} (V) Post at 23°C
100 nA	0.30*/0.17	0.21*/0.11	0.16*/0.12	-/-	-/-
1 µA	0.38/0.13	0.35/0.16	0.30/0.14	0.38/0.49	0.42*/0.15
10 µA	0. 41/0.16	0.33/0.16	0.26/0.11	0.51/0.41	0.41/0.15
100 µA	0.42/0.12	0.36/0.11	0.24/0.10	0.54*/0.58*	0.45/0.13
1 mA	0.39/0.12	0.35/0.11	0.24/0.10	0.25/0.10	0.44/0.14

Table 3.10: Activation Energies and Electric Field at V_{T1} of SnSe Devices with Ge₂Se₃ or GeTe Memory Layers.

Device	Activation Energy (eV)	Electric Field at 23 °C (Vcm⁻¹)
Ge₂Se₃/SnSe/Ag	0.031	1.16×10^4
GeTe/SnSe/Ag	0.059	2.58×10^4

There is a large difference in activation energies for the chalcogenides as seen in Table 3.10. The electric field for the GeTe device at the first threshold is 2.58×10^4 Vcm⁻¹, twice that of the Ge₂Se₃ device as seen in Table 3.10. The first threshold voltages of the GeTe devices are more than double that of the Ge₂Se₃ devices at 23 °C and 50 °C.

3.5 Conclusion

In this chapter, the threshold voltages were investigated on six different layered devices. The effects of programming current and temperature were examined on the threshold voltages of the first and second write sweeps. The devices were also investigated post temperature measurements on virgin devices to investigate the effect of thermal exposure to 150 °C. The five different metal-selenide devices with Ge_2Se_3 were compared. Also compared were SnSe devices with varying memory layers of either Ge_2Se_3 or GeTe.

CHAPTER 4: RESISTANCE CHARACTERISTICS

4.1 Introduction

The resistance of an ion-conducting device is the defining attribute that can be varied due to programming conditions. The silver conductive channel that bridges the two electrodes will determine the low resistance of the device. The amorphous medium without a silver channel will determine the high resistance state. The amorphous memory layer, either Ge_2Se_3 or GeTe, is inherently resistive. Without the silver conductive channel, the resistance is high and the device is considered 'OFF.' When the conductive channel is formed during a write sweep, the device will switch into a low resistance state and be considered 'ON.'

In this chapter, we discuss the effects of compliance current and programming temperature on device resistance.

4.2 Programming Current and Temperature Effects on Resistance

The DC sweeps used for the measurements discussed in this section were described in Chapter 2. The DC sweeps performed had compliance currents of 100 nA, 1 μA, 10 μA, 100 μA, and 1mA. The temperatures at which testing was administered were 23 °C, 50 °C, 100 °C, and 150 °C and retested at 23 °C post thermal exposure. All measurements had the W/E/W sequence described in Chapter 2. The second write resistance values are similar to the first write resistance values with the second write

resistance values used in comparison for simplicity. In the following figures, bars above

and below the average values are high and low values, respectively, not error bars.

4.2.1 Stack Ge$_2$Se$_3$/ Sb$_2$Se$_3$/Ag

The Sb$_2$Se$_3$ device erase and second write resistance values are shown in Figure

4.1 for the varying compliance currents at all four temperatures. Five to six virgin

devices were tested at each compliance current and temperature. Post 150 °C, devices

remained on the probe station overnight and were allowed to slowly cool to 23 °C, and

were tested approximately 17 hours later. Bars above and below the average points

provided in figures are the high and low threshold voltage values, not error bars. Second

write resistance values are used in graphs and tables for simplicity because the first write

resistance values are similar, as shown in Table 4.1.
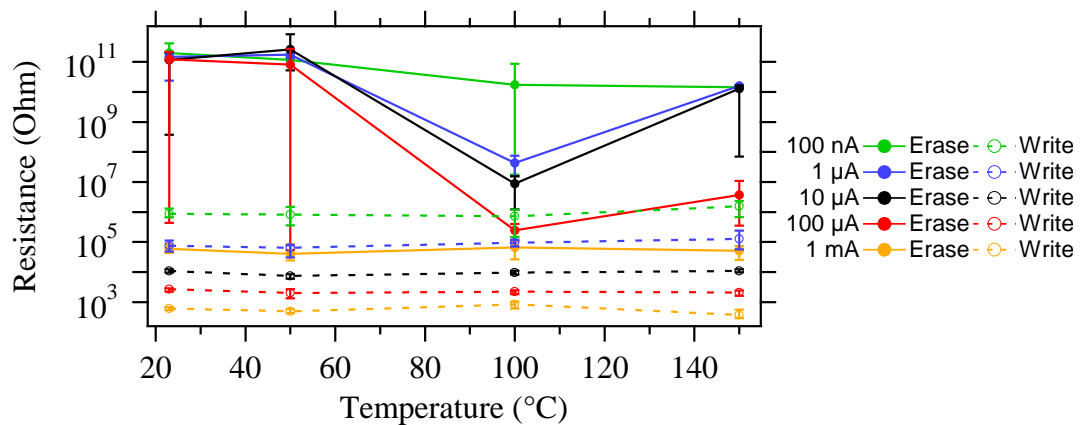
Figure 4.1: Plot of Erase and Second Write Resistances Versus Temperature with Varying Programming Compliance Currents for Ge$_2$Se$_3$/ Sb$_2$Se$_3$/Ag Devices.

The second write resistance values are consistent across the temperature range

shown by the parallel dashed lines of Figure 4.1. As the programming current is

increased from 100 nA to 1 mA, the device's 'ON' resistance decreases by over three orders of magnitude.

The erase resistance values in Figure 4.1 are consistent for all programming currents up to 50 °C. The erase resistance of the 100 nA programmed devices slightly decreases with an increase in temperature. The erase resistance of the 1 µA, 10 µA, and 100 µA programmed devices decreased at 100 °C with an increase at 150 °C. Even with a fluctuation of the erase resistance at the higher temperatures, the devices still maintain one order of magnitude difference between the second write and erase resistance values. To maintain a large ratio of the 'OFF' and 'ON' resistance values is the fundamental requirements for resistance type memory. The 1 mA programmed erase resistance devices were least effected by temperature, but the value is significantly lower at 10^5 Ω compared to other programmed devices at 10^{11} Ω. The 1 mA programmed devices had over two orders of magnitude differences between the erase and second write resistances, plus exhibit tight control around the average value. The other devices had a greater disparity around the average erase resistance values. However, the lowest 'OFF' resistance values are still orders greater than the second write resistance values. The best programming current for the Sb_2Se_3 devices for separation of high and low resistance, high precision, and thermal stability would be a programming current of 100 nA or 1 mA.

The programming current used in writing the device does impact how much power is required to erase the device back to a high resistance state. This is evident in Figure 4.2, which shows the power at the erase threshold at four different temperatures.

The power is calculated by multiplying the current and the voltage at the point the device changed from a low resistance state to a high resistance state.
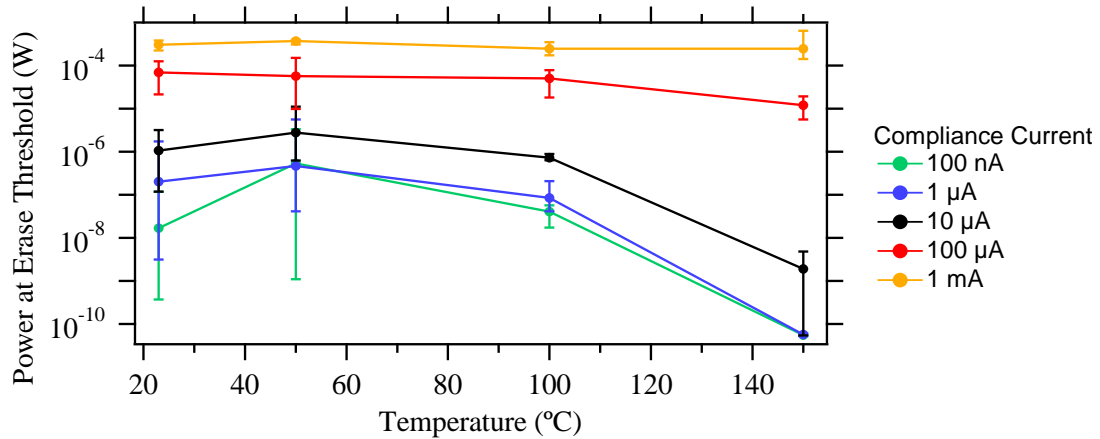
Figure 4.2: Plot of Power at the Erase Threshold Versus Temperature with Varying Programming Compliance Currents for Ge$_2$Se$_3$/ Sb$_2$Se$_3$/Ag Devices.

The temperature increase above 100 °C does assist in erasing the devices, which lowers the power required to erase the devices as seen in Figure 4.2. The higher programming current devices require more power than the additional thermal energy to significantly aid in erasing the devices. When the programming current increases, which increases the ON/OFF resistance ratio, it is at the expense of greater power needed to erase the devices back into a high resistance state. The 1 mA programming current writes the devices into such a low resistance state that even mWatts of power can not erase the devices into as high of a resistance state as the other programming currents. There are three orders of magnitude of difference between the 1 mA and 100 μA erased resistance values, 1.1×10^8 Ω compared to 1.5×10^{11}Ω, as seen in the erase resistance column in Table 4.1.

Table 4.1: Average Erase and Second Write Resistance Values at 23 °C Pre- and Post-Thermal Exposure of 150 °C for Ge_2Se_3/ Sb_2Se_3/Ag Devices. The Virgin Devices, Pre- and Post-Thermal Exposure, Had an Initial Resistance of Approximately $5x10^{11}$ and $3x10^{11}\Omega$, Respectively.

Program Current	1st Write Resistance (Ω)		Erase Resistance (Ω)		2nd Write Resistance (Ω)	
	Pre-thermal exposure	Post-thermal exposure	Pre-thermal exposure	Post-thermal exposure	Pre-thermal exposure	Post-thermal exposure
100 nA	$7.4x10^5$	$5.5x10^5$	$2.0x10^{11}$	$1.5x10^{11}$	$8.7x10^5$	$9.6x10^5$
1 µA	$7.7x10^4$	$6.1x10^4$	$1.5x10^{11}$	$8.0x10^{10}$	$7.4x10^4$	$1.4x10^5$
10 µA	$9.4x10^3$	$8.7x10^3$	$1.2x10^{11}$	$1.2x10^8$	$1.1x10^4$	$1.4x10^4$
100 µA	$2.4x10^3$	$2.6x10^3$	$1.2x10^{11}$	$2.3x10^7$	$2.7x10^3$	$3.2x10^3$
1 mA	$8.7x10^2$	$1.4x10^3$	$1.1x10^8$	$6.8x10^7$	$6.6x10^2$	$9.5x10^2$

There is a slight decrease in initial resistance values of the post-thermal exposed virgin devices compared to the pre-thermally exposed devices in Table 4.1. This is possibly due to a relaxation of the Ge_2Se_3 layer (16).

The thermal exposure did affect the erase resistances of the 10 µA and 100 µA programming current devices in Table 4.1. The post thermal exposure values for those devices are not similar to the pre-thermal exposed devices, whereas the other erase resistances are similar for the other programming currents. This result suggests a possible variation in film of the region of wafer used for testing those devices. The write resistance appears to be unaffected by exposure to the elevated temperature of 150 °C; the pre and post thermal write resistances have very similar values.

4.2.2 <u>Stack Ge$_2$Se$_3$/ SnSe/Ag</u>

The plot of erase and second write resistances for the Ge$_2$Se$_3$/ SnSe/Ag stack is

shown in Figure 4.3. Three to five virgin devices were tested at each temperature and

compliance current. The devices were exposed at each temperature for 20 minutes prior

to testing to allow time to equilibrate. The devices were exposed to 150 °C for a total of

45 minutes. Post 150 °C, devices remained on the probe station, then were allowed to

slowly cool to 23 °C, and were tested after approximately 4 hours. For each graph

provided, bars above and below the average values are high and low, respectively, not

error bars. Second write resistance values are used in graphs and tables for simplicity but

first write resistance values are similar as shown in Table 4.2.
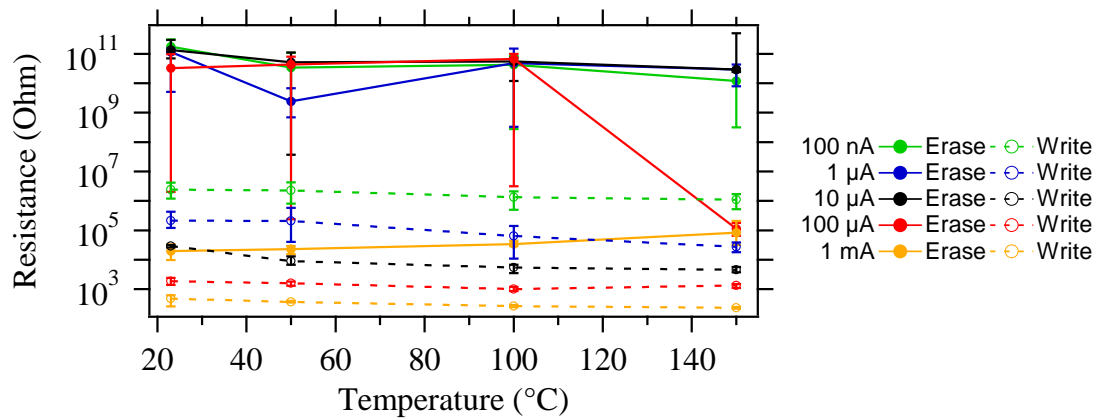
Figure 4.3: Plot of Erase and Second Write Resistances Versus Temperature at Five Programming Compliance Currents for Ge$_2$Se$_3$/SnSe/Ag Stack.

The second write resistances are not affected by temperature, as seen by the

horizontal dashed lines in Figure 4.3. The write resistance values are parallel to each

other and decrease as programming current is increased across all temperatures.

The erase resistance values in Figure 4.3 are consistent across all temperatures except for the 100 µA programmed devices, which have a sharp decline at 150 °C. The resistance value at that 150 °C for the 100 µA device is similar to the 1 mA programmed current device's erase resistance. This would suggest that the joule heating from the high current flow through the silver conductive channel in conjunction with the thermal exposure creates an annealing effect of the Ge_2Se_3 layer (16). However, at 150 °C, the spread between the second write and erase resistances is still two orders of magnitude different for all programming currents.

The erase resistances for the lower programming currents are not as controlled as the higher programming currents of 1 mA. This can be seen from the high and low bars around the average values of Figure 4.3. However, the erase resistances in the 1 mA case are much lower than in the cases of the other programming currents. The 100 µA programmed devices are not as easy to erase at 150 °C, as seen from the sharp decrease in erase resistance from 10^{11} to $10^5 \, \Omega$. The 10 µA programming current provides the tightest control, greatest separation between high and low resistance and is not influenced by temperature.

The erase threshold power requirements to turn the device 'OFF' across four temperatures and for five programming currents are shown in Figure 4.4. The power at the second write threshold is shown in Figure 4.5 at four temperatures and five programming currents.
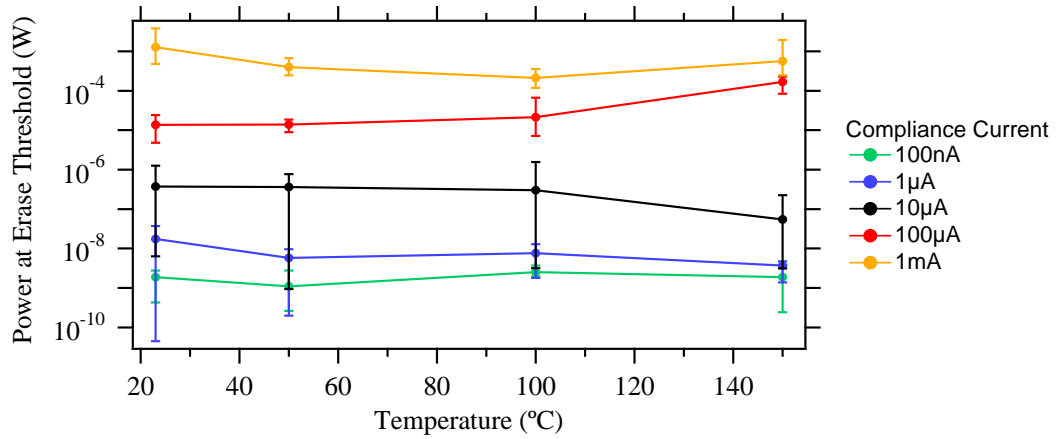
Figure 4.4: Plot of Power at Erase Threshold at Four Temperatures for Five Programming Compliance Currents for Ge$_2$Se$_3$/ SnSe/Ag Devices.

    The power required to place the devices into a high resistance state does increase

with increase in programming current as shown in Figure 4.4. The temperature up to

150 °C does not provide significant thermal energy to decrease the consumed power.

Table 4.2: Average Erase and Write Resistance Values at 23 °C Pre- and Post-Thermal Exposure of 150 °C for Ge$_2$Se$_3$/SnSe/Ag Devices. The Virgin Devices, Pre- and Post-Thermal Exposure, Had an Initial Resistance of Approximately 1x10^8 and 5x10^7 Ω, Respectively.

Program Current	1st Write Resistance (Ω)		Erase Resistance (Ω)		2nd Write Resistance (Ω)	
	Pre-thermal exposure	Post-thermal exposure	Pre-thermal exposure	Post-thermal exposure	Pre-thermal exposure	Post-thermal exposure
100 nA	2.1x10^6	2.9x10^6	1.8x10^{11}	3.9x10^{10}	2.4x10^6	3.8x10^6
1 µA	1.3x10^5	1.8x10^5	9.4x10^{10}	4.3x10^{10}	2.1x10^5	1.8x10^5
10 µA	9.3x10^3	6.4x10^3	1.4x10^{11}	2.0x10^{10}	2.9x10^4	9.7x10^3
100 µA	1.8x10^3	2.2x10^3	3.2x10^{10}	6.0x10^4	1.9x10^3	1.1x10^3
1 mA	9.8x10^2	9.5x10^2	2.0x10^4	2.0x10^4	4.8x10^2	1.9x10^2

The initial resistance, provided in Table 4.2, varies by a half an order of magnitude; this variation would suggest that there was an annealing effect on the Ge_2Se_3 memory material system (16).

The 100 µA programmed device erase resistance is affected by the thermal exposure as seen in Table 4.2. There is approximately six orders of magnitude difference of the erase resistances between the pre and post thermal exposed devices. The post thermal exposure value is close to the 1 mA erase resistance value. The added thermal energy into the virgin device prior to programming perhaps caused a structural change that provides greater affinity of the silver to bond with the germanium while erasing. These Ag-Ge bonds could provide the 'stepping stones' for conduction in the 'OFF' state (6).

The write resistances are not affected greatly by the exposure to heat. The post thermal exposure devices have a slight decrease of write resistance compared to the pre-thermal exposed devices.

4.2.3 Stack Ge_2Se_3/ PbSe/ Ag

The erase and second write resistance values for the Ge_2Se_3/PbSe/Ag devices are shown in Figure 4.5. The devices were exposed at each temperature for 20 minutes prior to testing to allow time to equilibrate. The devices were exposed to 150 °C for a total of 47 minutes. Post 150 °C, devices remained on the probe station over night. The devices were allowed to cool to 23 °C and were tested after approximately 16 hours. For each graph provided, bars above and below the average values are high and low, respectively,

not error bars. The second write resistance value is used in figures and tables for simplicity because the first write resistance values are similar as shown in Table 4.3.
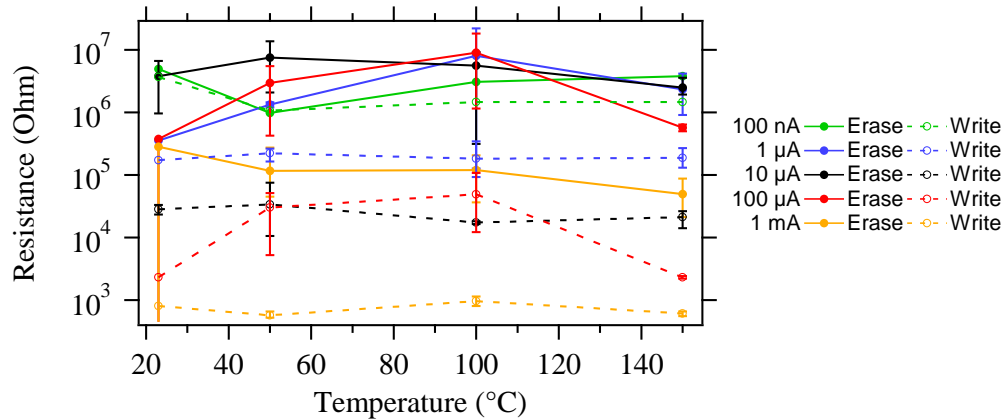
Figure 4.5: Plot of Erase and Second Write Resistances Versus Temperature for Five Programming Currents for Ge$_2$Se$_3$/PbSe/Ag Stack.

The second write resistances in Figure 4.5 decrease with increasing programming current overall. The 100 µA programming current written resistance does increase at 50 °C and 100 °C. These data points have one device with a higher value that skews the average but is not removed by q-test. Q-test is described in Chapter 3.1.

The erase resistance values for the 100 nA programming current are very similar to the write resistance values. This suggests that the PbSe device was not able to switch between a high and low resistance state at any temperature with a 100 nA programming current. The 1 µA programming current was not able to switch from a high to low resistive state at 23 °C as well. The devices' erase resistances were marginally increased at 50 °C, and the spread between erase and written improved slightly at 100 °C and 150 °C by approximately one order of magnitude.

The power needed to erase the devices into a higher resistance increases with an increase in programming current as seen in Figure 4.6.
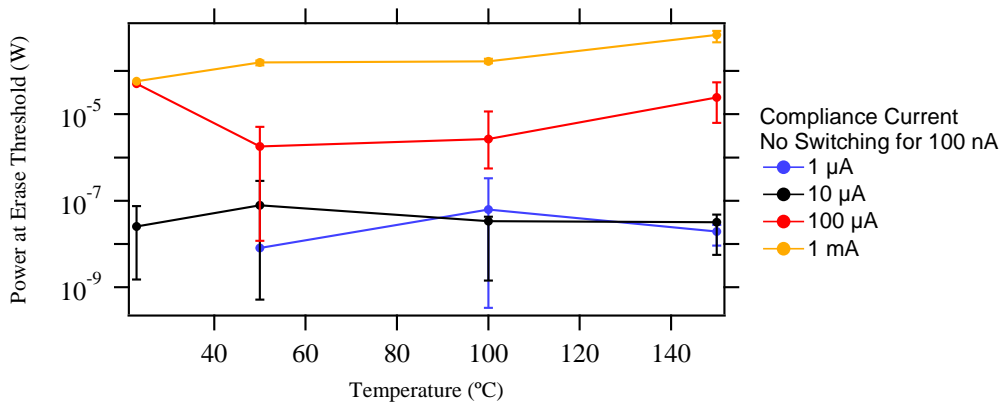
Figure 4.6: Plot of Power at Erase Threshold Versus Temperature with Varying Programming Compliance Currents for Ge$_2$Se$_3$/ PbSe/Ag Devices.

The greatest spread between erase and written resistance values are from the 100 µA and 1 mA programming currents. The 1 mA programming current, however, has greater precision than the 100 µA programming current. Overall, the 1 mA programming current is the best option for Ge$_2$Se$_3$/PbSe/Ag devices due to thermal stability while writing. Devices exhibit precision with a large spread between high and low resistance values.

Table 4.3: Average Erase and Write Resistance Values at 23 °C Pre- and Post-Thermal Exposure for Ge$_2$Se$_3$/PbSe/Ag Devices. The Virgin Devices, Pre- and Post-Thermal Exposure, had an Initial Resistance of Approximately 6x10^6 and 8x10^6 Ω Respectively.

Program Current	1st Write Resistance (Ω)		Erase Resistance (Ω)		2nd Write Resistance (Ω)	
	Pre-thermal exposure	Post-thermal exposure	Pre-thermal exposure	Post-thermal exposure	Pre-thermal exposure	Post-thermal exposure
100 nA	2.5×10^6	3.4×10^6	5.0×10^6	1.5×10^7	3.7×10^6	6.5×10^6
1 µA	1.3×10^5	1.3×10^6	3.6×10^5	1.1×10^7	1.7×10^5	1.6×10^6
10 µA	7.2×10^4	2.8×10^4	3.8×10^6	1.3×10^7	2.8×10^4	1.6×10^4
100 µA	8.0×10^2	1.8×10^3	3.8×10^5	1.5×10^7	2.3×10^3	1.7×10^3
1 mA	8.5×10^2	3.6×10^2	2.8×10^5	3.2×10^5	8.0×10^2	3.5×10^2

The initial resistances of both pre- and post-thermal exposure are similar, as shown in Table 4.3. The thermal exposure did not produce an annealing effect on the material system. The initial resistance values are already relatively low compared to the other bi-layer devices.

The erase resistances are greater after the thermal exposure whereas the second write resistance values are approximately the same. The thermal exposure process increased the spread between the two different resistance states.

4.2.4 Stack Ge$_2$Se$_3$/Ag$_2$Se/Ag

Figure 4.7 shows the erase and second write resistance values for the Ag$_2$Se-layered devices. Three to five virgin devices were tested at each temperature and compliance current. The devices were exposed at each temperature for 20 minutes prior

to testing to allow time to equilibrate. The devices were exposed to 150 °C for a total of

45 minutes. Post 150 °C, devices remained on the probe station and were allowed to cool

to 23 °C, and were tested after approximately 4 hours. For each graph provided, bars

above and below the average values are high and low, respectively, not error bars.

Second written resistance values are used in graphs and tables because the first write

resistance values are similar.
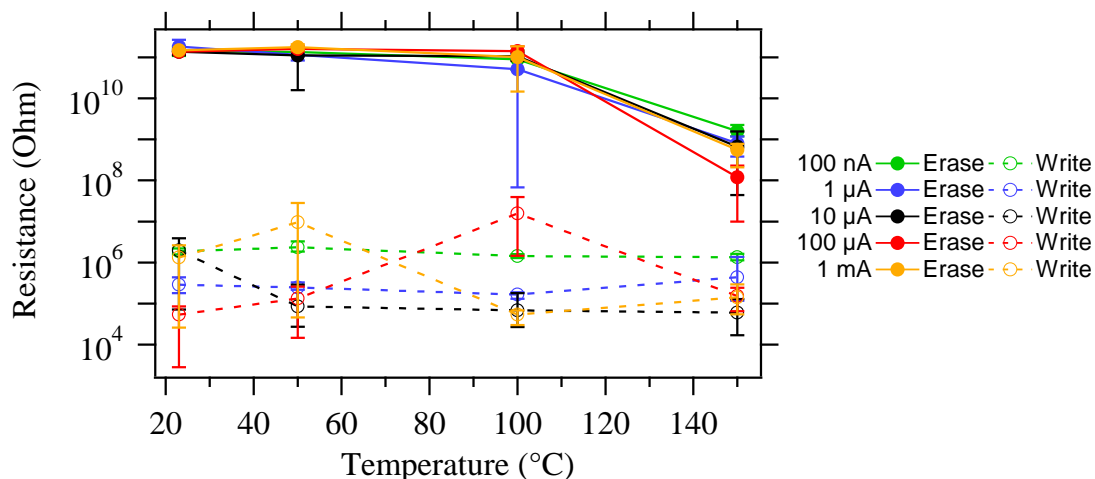
Figure 4.7: Plot of Erase and Second Write Resistances Versus Four Temperatures for Five Programming Compliance Currents for Ge$_2$Se$_3$/Ag$_2$Se/Ag Stack.

The written resistance values are sporadic and show no trend except that across all

temperatures, all programming currents will yield a low resistance between 10^4 to $10^7\,\Omega$.

The most controlled devices were the 100 nA and 1 µA programmed devices.

The erase resistances are all very similarly for all compliance currents at all

temperatures. Up to 100 °C, the erase resistance is around $10^{11}\,\Omega$; and at 150 °C, all of

the values decrease approximately to 10^8-$10^9\,\Omega$. The additional heat has possibly

relaxed the Ge$_2$Se$_3$ layer (16). The overall spread between the 'ON' and 'OFF' state is

about five orders of magnitude up to 100 °C.   The lower compliance currents also have less variation about the average values. The higher compliance currents of 100 µA and 1 mA have greater deviations from the average values than the lower programming currents when writing. The 100 nA programming current creates the largest separation of high and low resistance and is only affected by the 150 °C temperature, similar to other programming currents.

The power required to erase the devices into a high resistance state are shown in Figure 4.8. The lower programming currents of 100 nA and 1 µA follow a trend like the previous devices such that an increase of compliance current at writing requires greater power to erase. The higher compliance currents of 10 µA, 100 µA, and 1 mA all have similar power requirements at the erase threshold.
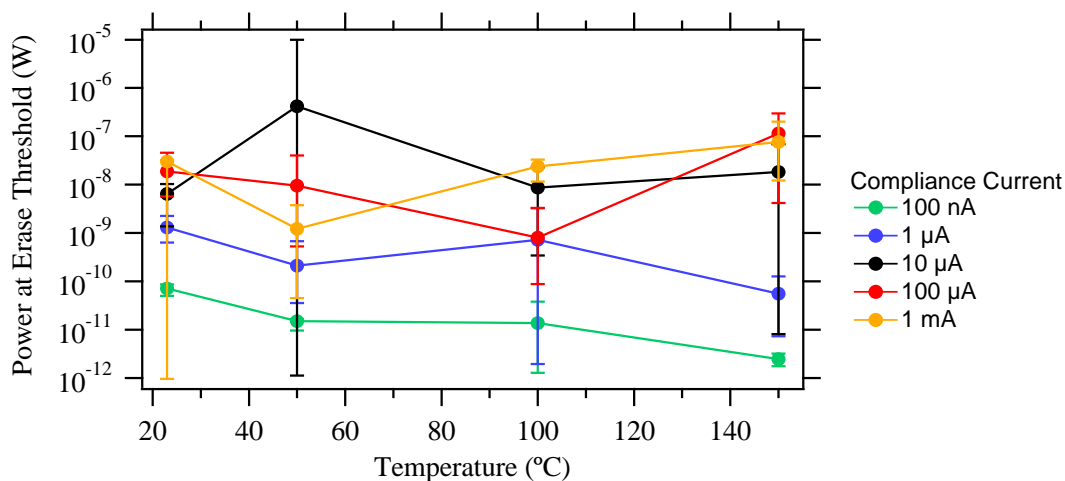
Figure 4.8: Plot of Power at Erase Threshold Versus Temperature with Five Programming Currents for Ge$_2$Se$_3$/ Ag$_2$Se/Ag Devices.

Table 4.4: Average Erase and Write Resistance Values at 23 °C Pre- and Post-Thermal Exposure for $Ge_2Se_3/Ag_2Se_3/Ag$ Devices. The Virgin Devices, Pre- and Post-Thermal Exposure, Had an Initial Resistance of Approximately $2x10^{11}$ and $5x10^{10}$ Ω, Respectively.

Program Current	*1st Write Resistance (Ω)*		*Erase Resistance (Ω)*		*2nd Write Resistance (Ω)*	
	Pre-Thermal Exposure	Post-Thermal Exposure	Pre-Thermal Exposure	Post-Thermal Exposure	Pre-Thermal Exposure	Post-Thermal Exposure
100 nA	$1.9x10^6$	$8.4x10^5$	$1.4x10^{11}$	$7.4x10^{10}$	$1.9x10^6$	$8.9x10^5$
1 µA	$2.3x10^5$	$1.9x10^5$	$1.8x10^{11}$	$1.5x10^{11}$	$2.9x10^5$	$2.1x10^5$
10 µA	$8.9x10^5$	$6.6x10^3$	$1.4x10^{11}$	$5.7x10^{10}$	$2.0x10^6$	$1.0x10^4$
100 µA	$2.5x10^4$	$3.2x10^5$	$1.4x10^{11}$	$1.0x10^{11}$	$5.4x10^4$	$5.4x10^5$
1 mA	$6.9x10^5$	$5.5x10^3$	$1.5x10^{11}$	$1.1x10^{10}$	$1.3x10^6$	$1.0x10^4$

The initial resistance of post-thermal exposure virgin devices is half an order of magnitude less than the pre-thermal exposed virgin devices as mentioned in Table 4.4. The erase resistances are also affected by the exposure to heat. This change suggests that there is an annealing effect on the Ge_2Se_3 memory and adhesion layers. The write resistances post thermal exposure are typically lower than pre-thermal exposure, except for the 100 µA programmed devices, which were an order of magnitude higher than the pre-thermal resistances. Three devices had been tested post thermal exposure at 100 µA, and one had a write resistance of an order of magnitude less than the pre-thermal exposure.

4.2.5 Stack $Ge_2Se_3/In_2Se_3/Ag$

The In_2Se_3 devices' resistance values are shown in Figure 4.9. Six virgin devices were tested at each temperature and compliance current. The devices were exposed at each temperature for 20 minutes prior to testing to allow time to equilibrate. The devices were exposed to 150 °C for a total of 55 minutes. Post 150 °C, devices remained on the probe station and were allowed to slowly cool to 23 °C overnight. Devices were tested after approximately 18 hours later. For each graph provided, bars above and below the average values are high and low, respectively, not error bars. The second write resistance values are used in figures and tables for simplicity because the first write resistance values are similar.
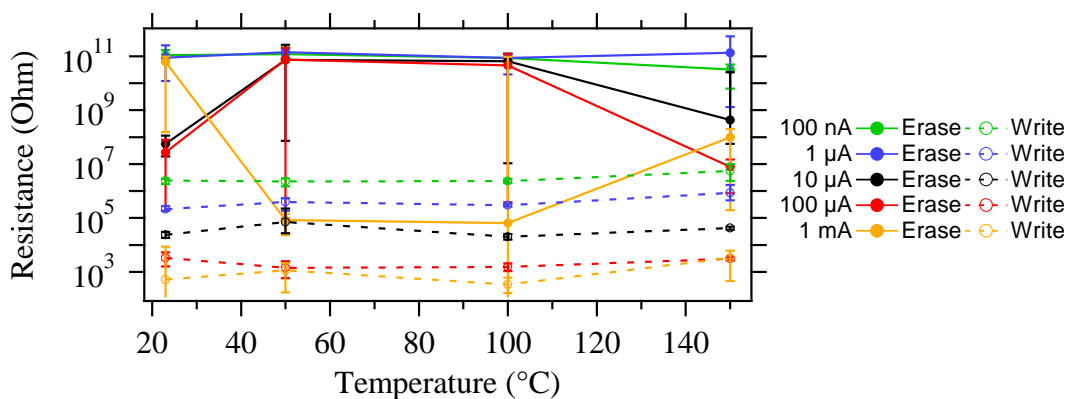
Figure 4.9: Plot of Erase and Second Write Resistances Versus Temperature at Varying Programming Compliance Currents for $Ge_2Se_3/In_2Se_3/Ag$ Stack.

The programmed written resistance values for these devices decrease with an increase of programming current across all temperatures.   The second write resistance values are unaffected, as seen by the parallel lines of Figure 4.9.

The erase resistance values for the In$_2$Se$_3$ devices are shown in Figure 4.9. The 100 nA and 1 µA programmed devices behave similarly across all temperatures and stay a consistent $10^{11}\,\Omega$. The 10 µA and 100 µA devices at 50 °C and 100 °C have about half the devices erase to $10^{11}\,\Omega$ and the other half to approximately $10^7\,\Omega$. Additional devices would need to be programmed at those temperatures to get a better statistical analysis. The overall best programming current would be either 100 nA or 1 µA to provide the largest separation between high and low resistance as well as lack of temperature effects.

The power necessary to erase the devices into a high resistance state at each compliance current is seen in Figure 4.10.
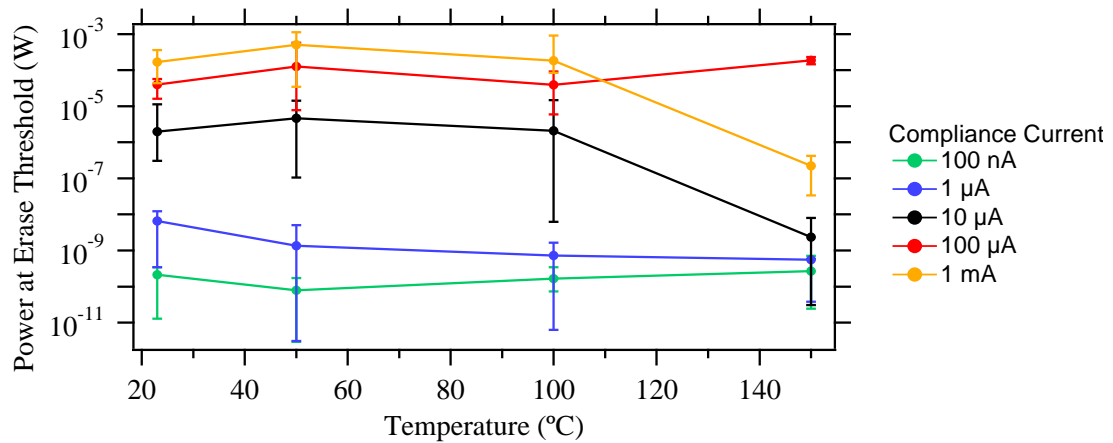
Figure 4.10: Plot of Power at Erase Threshold Versus Temperature with Five Programming Compliance Currents for Ge$_2$Se$_3$/ In$_2$Se$_3$/Ag Devices.

With increased programming current, there is an increase in the power needed to erase. The increase in power is explained because the higher programming currents create a device with lower resistance, which causes an increase in current flow during the initial erase sweep. At 150 °C, for 1 mA and 10 µA, there is a decrease in power;

whereas the 100 µA programmed devices have an increase in power requirement necessary to erase properly. There is unpredictable device behavior at the elevated temperature of 150 °C, which is well beyond the recommended 85 °C operating specifications for testing.

The post thermal exposure resistances are compared to pre thermal exposure resistances in Table 4.5.

Table 4.5: Average Erase and Write Resistance Values at 23 °C Pre- and Post-Thermal Exposure for In$_2$Se$_3$/Ge$_2$Se$_3$/Ag Devices. The Virgin Devices, Pre- and Post-Thermal Exposure, Had an Initial Resistance of Approximately 3x10^{11} Ω.

Program Current	1st Write Resistance (Ω)		Erase Resistance (Ω)		2nd Write Resistance (Ω)	
	Pre-Thermal Exposure	Post-Thermal Exposure	Pre-Thermal Exposure	Post-Thermal Exposure	Pre-Thermal Exposure	Post-Thermal Exposure
100 nA	1.9x10^6	9.3x10^5	1.1x10^{11}	1.4x10^{11}	2.5x10^6	1.4x10^6
1 µA	2.4x10^5	1.8x10^5	8.8x10^{10}	1.2x10^{11}	2.1x10^5	1.9x10^5
10 µA	2.3x10^4	3.5x10^4	5.6x10^7	2.1x10^7	2.4x10^4	3.6x10^4
100 µA	8.0x10^3	2.0x10^4	2.7x10^7	1.1x10^7	3.3x10^3	1.6x10^4
1 mA	5.5x10^3	2.6x10^4	6.2x10^{10}	5.2x10^{10}	5.2x10^3	1.9x10^4

The initial resistance values for pre- and post-thermal exposure are the same as mentioned in Table 4.5. The erase resistance was unaffected by the thermal exposure. The write resistance of the 100 µA and 1 mA programming current devices was slightly increased by thermal exposure as seen in Table 4.5.

4.2.6 <u>Stack GeTe/SnSe/Ag</u>

The resistance values for the GeTe/SnSe/Ag devices are shown in Figure 4.11 and in Table 4.6. Five virgin devices were tested at each temperature and compliance current. The devices were exposed at each temperature for 20 minutes prior to testing to allow time to equilibrate. The devices were exposed to 150 °C for a total of 50 minutes. Post 150 °C, devices remained on the probe station and were allowed to cool to 23 °C, and were tested after approximately 5 hours. For each graph provided, bars above and below the average values are high and low, respectively, not error bars. Second write resistance values are used in figures and tables for simplicity because the first write resistances are similar.
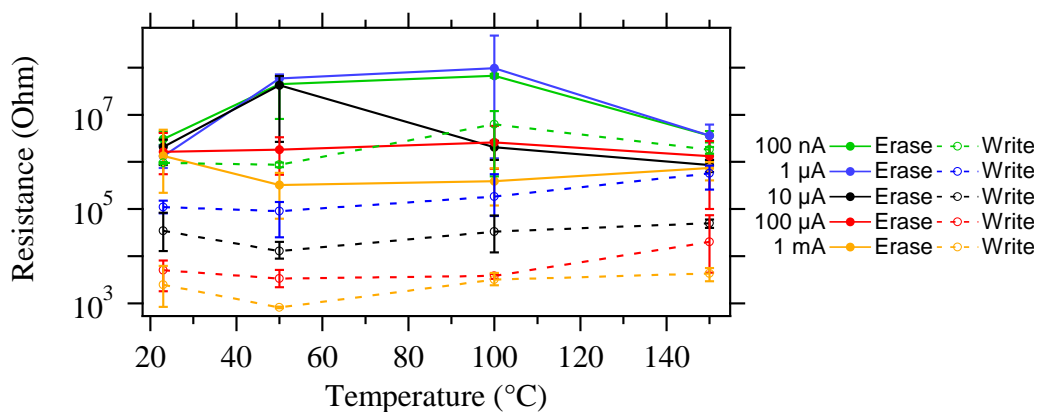
Figure 4.11: Plot of Erase and Second Write Resistances Versus Temperature for Five Programming Currents for GeTe/SnSe/Ag Stack.

The written resistances decrease with an increase of programming current. The write resistances also exhibit a trend that increases as temperature is increased. This would indicate it is more difficult to create a conductive silver channel within the GeTe layer with increased thermal energy. The 100 nA programming current is insufficient in

creating an 'OFF' and 'ON' state with this material at 150 °C, as can be seen with both

the write and erase resistances at $10^6\,\Omega$. At 23 °C, the 1 µA programmed devices

switched on with a resistance an order of magnitude less than that of the off state.

However, the spread between the 'ON' and 'OFF' resistance states increased by

approximately two orders of magnitude as programming current was increased.

The erase resistance values for the GeTe/SnSe/Ag devices are shown in Figure

4.11. The lower programming currents of 100 nA, 1 µA, and 10 µA devices are more

susceptible to changes in temperature from 50 °C to 100 °C. The higher programming

currents of 100 µA and 1 mA are consistent across the temperature range. Overall, the

best programming currents for this device are either 100 µA or 1 mA due to the greatest

separation in high and low resistance, thermal stability while programming and greatest

precision.

The power at the erase threshold is shown in Figure 4.12 for five programming

currents at four temperatures.
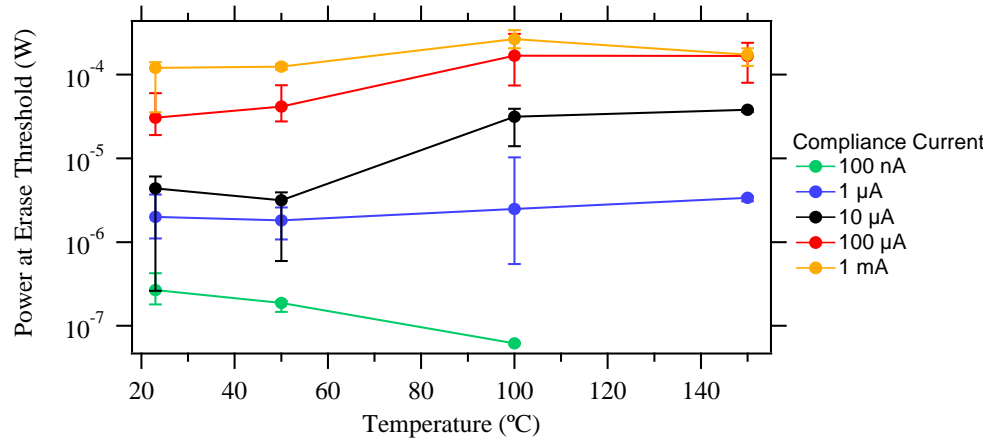
Figure 4.12: Plot of Power at Erase Threshold Versus Temperature with Varying Programming Compliance Currents for GeTe/ SnSe/Ag Devices.

The power to erase the devices will increase with increase in compliance current as seen in Figure 4.12. The GeTe/SnSe/Ag devices have a slight increase in erase power due to temperature at the higher compliance currents. This increased current flow can be attributed to the additional excited carriers due to the elevated temperatures.

Table 4.6: Average Erase and Write Resistance Values at 23 °C Pre- and Post-Thermal Exposure for GeTe/SnSe/Ag Devices. The Virgin Devices, Pre- and Post-Thermal Exposure, Had an Initial Resistance of Approximately $2x10^8$ and $4x10^6\,\Omega$, Respectively.

Program Current	1st Write Resistance (Ω)		Erase Resistance (Ω)		2nd Write Resistance (Ω)	
	Pre-Thermal Exposure	Post-Thermal Exposure	Pre-Thermal Exposure	Post-Thermal Exposure	Pre-Thermal Exposure	Post-Thermal Exposure
100 nA	$1.1x10^6$	$1.5x10^6$	$3.1x10^6$	$4.2x10^6$	$9.5x10^5$	$1.2x10^6$
1 µA	$1.2x10^5$	$2.1x10^5$	$1.3x10^6$	$5.3x10^6$	$1.1x10^5$	$1.2x10^5$
10 µA	$3.4x10^4$	$2.9x10^4$	$2.1x10^6$	$2.4x10^7$	$3.4x10^4$	$2.0x10^4$
100 µA	$4.8x10^3$	$3.5x10^3$	$1.6x10^6$	$5.2x10^5$	$5.0x10^3$	$3.3x10^3$
1 mA	$1.5x10^3$	$3.7x10^3$	$1.4x10^6$	$7.4x10^5$	$2.5x10^3$	$5.8x10^3$

The initial resistance of the virgin devices was significantly altered by the thermal exposure from $2x10^8$ to $4x10^6 \, \Omega$, as mentioned in Table 4.6. The post-thermal exposure initial resistance value is similar to the erase resistances of the pre-thermal exposed devices. This would suggest there was an annealing effect that relaxed the GeTe layer from joule heating as well as the thermal exposure. Once the silver conductive channel is disrupted, the erase high resistance state is a function of the medium (8).

4.3 Comparison of the Metal-Selenide Layered Devices

The erase resistances were affected by temperature and compliance currents depending on the metal-selenide layer. Four of the five different metal-selenide devices, Sb_2Se_3, SnSe, PbSe, and In_2Se_3, had a significant decrease in erase resistance due to a programming current of 1 mA and/or at elevated temperatures. All four types of devices had the erase resistance drop down to $10^5 \, \Omega$ due to the two interactions of programming current and/or thermal energy. The Ag_2Se devices' erase resistance were unaffected by the programming current but were influenced by the temperature. At 150 °C, the erase resistance of the Ag_2Se devices went from $10^{11} \, \Omega$ down to $\sim 10^8 \, \Omega$. The PbSe devices had the lowest erase resistance overall at $10^7 \, \Omega$ compared to the other four devices of $10^{11} \, \Omega$.

The write resistance averages for all varying metal-Se/Ge_2Se_3 devices were independent of temperature except for Ag_2Se devices, which fluctuated between 10^4 to $10^7 \, \Omega$. The write resistances for the four devices, Sb_2Se_3, SnSe, PbSe, and In_2Se_3, were dependent, however, on the compliance current used during the programming or write cycle as seen in Table 4.7. The second write resistance values across each programming

current for all four different devices are very similar. In addition, there is an

approximately one order of magnitude drop in write resistance for each decade increase

in programming current for the four different devices.

Table 4.7: Average Second Write Resistance Values from All Temperature Ranges for the Varying Metal-Chalcogenide Layers. Ag$_2$Se Is Excluded Due to Variation of Write Resistance Values from Changes in Temperature.

Program Current	Sb$_2$Se$_3$ Device 2nd Write Resistance (Ω)	SnSe Device 2nd Write Resistance (Ω)	PbSe Device 2nd Write Resistance (Ω)	In$_2$Se$_3$ Device 2nd Write Resistance (Ω)
100 nA	9.9x10^5	1.8x10^6	1.9x10^6	3.2x10^6
1 µA	9.0x10^4	1.3x10^5	1.9x10^5	4.4x10^5
10 µA	9.7x10^3	7.0x10^3	2.5x10^4	4.0x10^4
100 µA	2.2x10^3	1.5x10^3	2.1x10^4	2.3x10^3
1 mA	5.8x10^2	3.4x10^2	7.3x10^2	2.5x10^3

4.4 Comparison of the Chalcogenide Memory Layered Devices

The difference between the Ge$_2$Se$_3$/SnSe/Ag and GeTe/SnSe/Ag devices is

evident in the erase resistances. The highest resistance the GeTe device will achieve is

10^6 Ω compared to the Ge$_2$Se$_3$ device of 10^{11} Ω. There are several possible reasons why

there is such a disparity between the two cells even though the cell dimensions and film

thicknesses are same. One reason could be just from the difference in film quality from

the deposition process. The Ge$_2$Se$_3$ film was sputtered, and the GeTe film was thermally

evaporated. Sputtered films in general have better film quality and step coverage than

thermally evaporated films.   The most obvious reason for the disparity in erase

resistance values is that GeTe thin film is known to have a lower glass transition

temperature (150 °C) than Ge$_2$Se$_3$, (340 °C) (12). The wafers could have been exposed

to slightly warmer than room temperature during storage, and that temperature difference

might have been enough over time to cause some annealing effects on the GeTe layer.

Table 4.8: Average Second Write Resistance Values from All Temperature Ranges for the Varying Chalcogenide Memory Layers.

Programming Current	SnSe/Ge$_2$Se$_3$/Ag Device 2nd Write Resistance (Ω)	SnSe/GeTe/Ag Device 2nd Write Resistance (Ω)
100 nA	1.8x10^6	2.5x10^6
1 μA	1.3x10^5	2.4x10^5
10 μA	7.0x10^3	3.3x10^4
100 μA	1.5x10^3	8.1x10^3
1 mA	3.4x10^2	2.7x10^3

The chalcogenide memory layer GeTe device does have a slightly higher write

resistance at the greater programming currents compared to the Ge$_2$Se$_3$ device as seen in

Table 4.8. The difference is not significant until the 1 mA programmed devices are

compared. The GeTe devices programmed with 1 mA compliance current is one order of

magnitude greater than the Ge$_2$Se$_3$ devices.

4.5 Conclusion

In this chapter, the resistance was explored for six different chalcogenide-layered

virgin devices. The effects of programming current and temperature were examined on

the written resistance as well as the erase resistance. The devices were also investigated

post thermal exposure on virgin devices to see the effect of the temperature

measurements. The five different metal-selenide device resistance results were compared

in addition to two different chalcogenide memory layers.

CHAPTER 5: TOTAL IONIZING DOSE EFFECTS ON RETENTION AND

PROGRAMMING OF SnSe-BASED DEVICES

5.1 Introduction

Integrated circuits can be exposed to many different radiation environments. For space applications, the radiation environment will vary with altitude on the earth's surface whether in aircraft or an orbiting satellite. The variation in particles, energies, and total dose will cause some devices to fail in one radiation environment but maintain functionality in another. Radiation can cause single-event effects (SEE), which is when one single particle creates an observable effect. An example of an SEE is the creation of an e-h pair in a gate oxide and the subsequent degradation of the device. Another type of radiation effect considers all particles by summing the total radiation dose to produce an observable effect. This type is referred to as total ionizing dose (TID).

The types of particles present in earth's space radiation environment include electrons, protons, and some heavy ions trapped in the magnetosphere, as well as solar and galactic cosmic rays. Galactic cosmic rays are not from our solar system and consist mostly of protons and alpha particles (helium nuclei) (17; 18). Heavy ions are typically low in energy within the earth's atmosphere and are easily shielded. At lower earth orbital altitudes, there is an increase in proton flux compared to electron flux. Flux is the rate at which particles infringe upon a unit surface and is in units of particles/cm^2-s. Proton energies range from 10 MeV up to 500 MeV, with shielding attenuating proton

energies below 10 MeV (17). Electron energies can range up to 7 MeV but are not important for single-event effects but are considered in total ionizing dose effects (18). Total ionizing dose ranges are important to know because high dose rates simulate device response in weapon environments, and low dose rates simulate the natural space radiation environment. The U.S. Military has a standard guideline MIL-STD-883, Method 1019, that requires dose rates from 50 to 300 rad(Si)/s or 28 to 168 rad(SiO_2)/s (17). A rad is defined as radiation absorbed dose, and one rad is equal to 100 ergs of energy deposited per gram of material. One erg is 6.24×10^{11} eV. The material that has the infringement of energy is specified and typically has units of rad (Si)/s or rad (SiO_2)/s.

The effects from different types of particles and concentration will also depend on altitude from the earth's crust or angle of inclination, as well as the shielding of the packaged parts. The shield, which can be a space vehicle such as a satellite or spacecraft, modifies the incident radiation energy on an integrated circuit. The shielding alters the energy and concentration of the particles but will also create additional secondary particles from the incoming particles that pass through (17). Electrons that decelerate in the shielding and emit bremsstrahlung radiation in the form of x rays is an example of secondary effects.

In this chapter, a description of the x-ray source used for the irradiation of test devices for total ionizing effects is provided. Also, a description of the tests is provided, such as total ionizing dose effects on device programming, as well as retention studies on

irradiated programmed devices. This is followed by the electrical characterization results
of irradiation and DC sweep measurements.

5.1.1 Device Description

The layered devices used in the radiation testing were Ge_2Se_3/SnSe/Ag and
GeTe/SnSe/Ag sandwiched between two tungsten electrodes as described in Chapter 2.

5.1.2 Instrument Description

The most common radiation sources used for such tests include a Co-60 gamma
ray radiation source and an X-ray source. These sources are used because they are cost
effective for evaluation of radiation effects on microelectronics. To utilize the Co-60
source, however, requires an isotope license, and commonly the devices need to be
packaged. An X-ray irradiation source for wafer stage fabrication, however, does not
need to be at a radiation facility with isotope licenses.

The X-ray irradiation system by Aracor is commonly used for total ionizing dose
effects due to the ease of irradiation measurements during wafer processing. The Aracor
model 4100 semiconductor irradiation system utilizes a tungsten target X-ray that has a
characteristic energy of 10 keV. The low 10 keV energy X-rays ease the power and
shielding requirements for the Aracor tool. The 10 keV energy X-rays also minimize the
slope of the depth dose profile so the incident radiation is within the SiO_2 layer, not the
underlying Si, and the measured dose is in $rad(SiO_2)$/s (19). An example of the system
used in these tests is seen in Figure 5.1.

The Aracor system has demonstrated good correlation with the Co-60 source for some instances and in other cases large differences (17; 19). For bulk silicon transistors, Schwank et al. found that laboratory x-ray irradiation simulated the low-earth orbit proton rich environment better than a Co-60 source (20). The opposite is true for the electron rich environment; the Co-60 source was shown better simulating total dose degradation than an x-ray source (17). Whichever environment is being investigated, it is customary to use the x-ray source for process development and the Co-60 source for radiation hardness testing purely as historical practice and not because of technical reasons (17).

Figure 5.1: Image of an Aracor 4100 Wafer-Level X-ray Irradiator (17).

The Aracor wafer-level x-ray source can achieve a dose rate from 100 rad(SiO_2)/s to over 2000 rad(SiO_2)/s. The material of interest for most devices is either in units of rad(Si) or rad(SiO_2). The total ionizing dose for this initial study is in SiO_2 instead of Si units due to the fact that the penetration depth of the X-rays is in the SiO_2 layer. The U.S. military standard MIL-STD-883, Method 1019, specifies the performed testing needs to have dose rates from 50 to 300 rad(Si)/s (18). This equates to approximately 28 to 168 rad(SiO_2)/s since the dose in SiO_2 is about 0.56 times the dose deposition in Si (17). The military standard 883, Method 1019, has a sequence of testing procedures that are required and can be reviewed elsewhere (17; 21). The type of testing administered in this study allows a conservative look at the radiation hardness of devices. A thorough testing for radiation hardness would include a US standard MIL-STD-833, test Method 1019 (18).

5.2 Electrical Testing and Measurements of Total Ionizing Dose Effects on Programmed Devices

Electrical testing on the layered structures was performed using the Aracor system and the HP4156B mentioned in Chapter 2. All virgin devices came from the same cleaved piece of wafer approximately 1cm^2 in size. Ten devices each were programmed at 100 nA, 100 μA, and 1 mA compliance currents on a probe station. The devices were then transferred (by manual handling) to the Aracor system and irradiated for 69 minutes at a radiation rate of 120 rad(SiO_2)/s for a total dose of 500 krad(SiO_2). The Aracor accelerating voltage was set at 50 kV, and the associated beam current was 5 mA. The

cleaved piece was then manually transferred back to the probe station, and a resistance read was performed by sweeping the devices from 0 to 50 mV. A control on retention was performed on virgin devices not exposed to radiation. The control devices were cleaved from the same wafer 20 mm from the experimental devices prior to radiation exposure. The control devices were programmed on the same probe station, and a subsequent read sweep with an approximate time delay of the irradiated devices programming and read sweeps. The controls were handled and moved as the experimental devices to simulate the handling of the irradiated devices. It is possible for the stress from moving the devices or the placement of the probe tips down onto the electrode pads to generate significant charge.   The sensitivity to electrostatic discharge could potentially switch the device resistance since the threshold voltages are 200 mV or less.

5.2.1 Electrical Characteristics of Total Ionizing Dose Effects on Programmed GeTe/SnSe/Ag Stack Devices

The GeTe/SnSe/Ag cleaved wafer piece had ten, nine, and six devices programmed at 100 nA, 100 µA, and 1 mA compliance currents, respectively, on a probe station.   The cleaved wafer was manually moved across the lab to the Aracor system and subsequently exposed to radiation for a total dose of 500 krad(SiO_2). The cleaved wafer piece was transferred back to the probe station, and a read sweep from 0 to 50 mV was performed. The results are compared to the non-irradiated control devices.

5.2.1.1 <u>Total Ionizing Dose Effects on the Retention of Resistance State for GeTe/SnSe/Ag Devices with a Programmed 100 nA Compliance Current.</u>

The time difference between the programming and the read sweep of the irradiated devices was approximately 3.25 hrs. The time difference for the control devices was 3.5 hrs. Figure 5.2 shows the second write programmed resistance and read resistance values for both control and irradiated two terminal devices.

Figure 5.2: Plot of Resistances for GeTe/SnSe/Ag Stack Irradiated and Control Devices with a Programming 100 nA Compliance Current.

As seen in Figure 5.2, the irradiated GeTe devices maintained the programmed resistance state across all ten devices compared to only half the control devices when 100 nA compliance current is used. The control devices were moved from the probe station after the initial programming and back to the probe station for a final read sweep to simulate the motion of the irradiated devices. This movement could have caused an electrostatic discharge that affected the performance of the devices. The GeTe/SnSe/Ag control devices were programmed and read the following day from the irradiated sources and due to environmental reasons possibly have an impact on device behavior.

5.2.1.2 Total Ionizing Dose Effects on the Retention of Resistance State for GeTe/SnSe/Ag Devices with a Programmed 100 µA Compliance Current.

The time difference between the 100 µA compliance current programming and the read sweep of the 100 µA irradiated devices was approximately 3.25 hrs. The time difference for the control devices was 3.5 hrs. Figure 5.3 shows the second write programmed resistance and read resistance for both control and irradiated two-terminal devices programmed with the 100 µA compliance current.

Figure 5.3: Plot of Resistances for GeTe/SnSe/Ag Stack Irradiated and Control Devices with a Programming 100 µA Compliance Current.

The irradiated devices have read resistances that are approximately within one order of magnitude of the programmed resistance, as well as seven out of nine of the control devices.

5.2.1.3 Total Ionizing Dose Effects on the Retention Resistance State for GeTe/SnSe/Ag Devices with a Programmed 1 mA Compliance Current.

The time difference between the programming and the read sweep of the 1 mA irradiated devices was approximately 3.0 hrs and 3.5 hrs for the control devices. Figure

5.4 shows the programmed resistances and read resistances of both irradiated and control

device programmed with 1 mA compliance current.

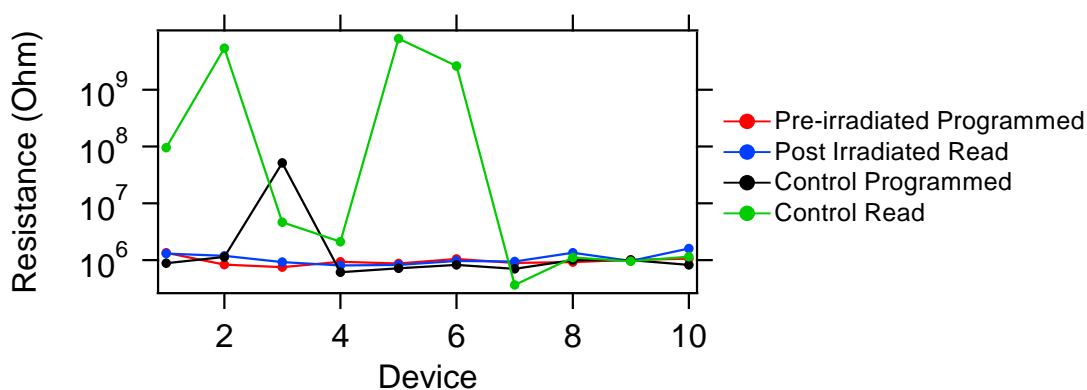**Figure 5.4: Plot of Resistances for GeTe/SnSe/Ag Stack Irradiated and Control Devices with a Programming 1 mA Compliance Current.**

Both the control and irradiated devices in Figure 5.4 maintain the resistance state

within an order of magnitude when programmed with 1 mA compliance current.

5.2.2 Electrical Characteristics of Total Ionizing Dose Effects on Programmed
Ge_2Se_3/SnSe/Ag Stack Devices

The Ge_2Se_3/SnSe/Ag cleaved wafer piece had ten devices programmed at each

compliance current of 100 nA, 100 µA, and 1 mA on a probe station.   The cleaved wafer

was manually moved across the lab to the Aracor system and subsequently exposed to

radiation for a total dose of 500 krad(SiO_2). The cleaved wafer piece was transferred

back to the probe station and a read sweep from 0 to 50 mV was performed. The results

are compared to the non-irradiated control devices. The control and irradiated devices

were programmed on the same day.

5.2.2.1 <u>Total Ionizing Dose Effects on the Retention of Resistance State for</u>
<u>Ge_2Se_3/SnSe/Ag Devices with a Programmed 100 nA Compliance Current.</u>

The time difference between the programming and the read sweep of the 100 nA
irradiated devices was approximately 3.6 hrs and 3.8 hrs for the control devices. Figure
5.5 is a plot of resistance for each of the irradiated and control devices programmed with
100 nA compliance current.
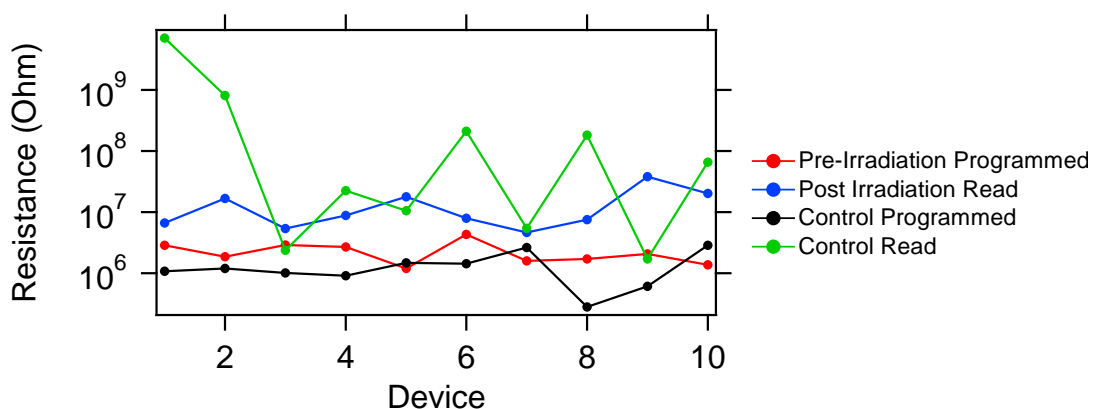
Figure 5.5: Plot of Resistances for Irradiated Ge_2Se_3/SnSe/Ag Stack and Control
Devices with a Programming 100 nA Compliance Current.

The control devices maintained the programmed resistance state within an order
of magnitude 50% of the time shown in Figure 5.5. Of the remaining five control
devices, two had changes greater than two orders of magnitude in resistance. Nine out of
ten irradiated devices maintained the programmed resistance within an order of
magnitude. The change in resistance state could be a function of handling and
electrostatic discharge.

5.2.2.2 <u>Total Ionizing Dose Effects on the Retention of Resistance State for</u>
<u>Ge$_2$Se$_3$/SnSe/Ag Devices with a Programmed 100 µA Compliance Current.</u>

The time difference between the programming and the read sweep of the 100 µA
irradiated devices was approximately 3.5 hrs and 3.8 hrs for the control devices. Figure
5.6 is a plot of resistance for each of the irradiated and control devices programmed with
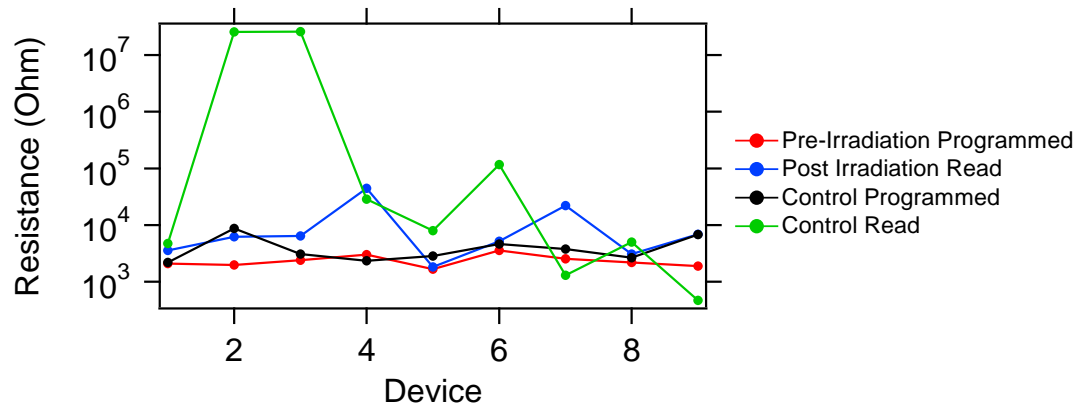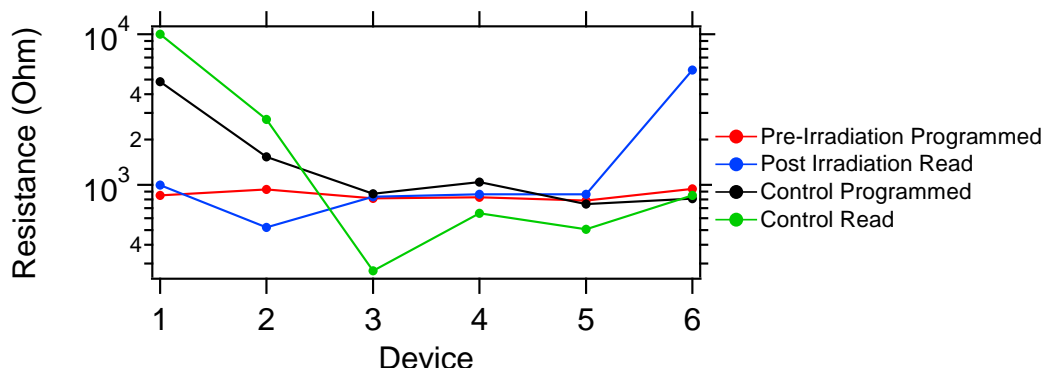100 µA compliance currents.
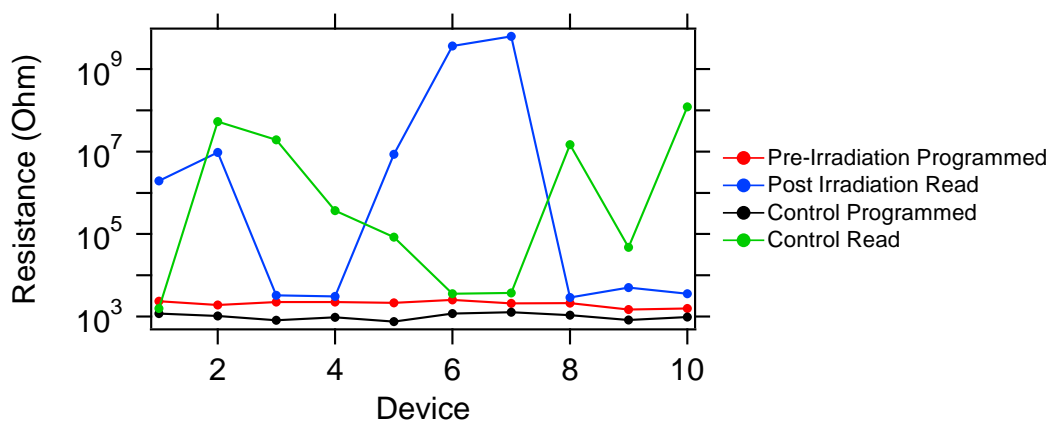
Figure 5.6: Plot of Resistances for Ge$_2$Se$_3$/SnSe/Ag Stack Irradiated and Control
Devices with a Programming 100 µA Compliance Current.

Both irradiated and control devices programmed in a low resistance state of 10^3 Ω

seen in Figure 5.6. Only five irradiated samples maintained the low resistance state, three

devices increased in resistance by three orders of magnitude to 10^7 Ω and two devices

increased in resistance to 10^9 Ω. The control devices did not fully erase into the high

resistance state as the irradiated devices. Approximately half of the control devices

maintained a resistance state within two orders of magnitude.

5.2.2.3 Total Ionizing Dose Effects on the Retention of Resistance State for Ge$_2$Se$_3$/SnSe/Ag Devices with a Programmed 1 mA Compliance Current.

The time difference between the programming and the read sweep of the 1 mA irradiated devices was approximately 3.5 hrs and 3.75 hrs for the control devices. Figure 5.7 is a plot of resistance for each of the irradiated and control devices programmed with 1 mA compliance current.
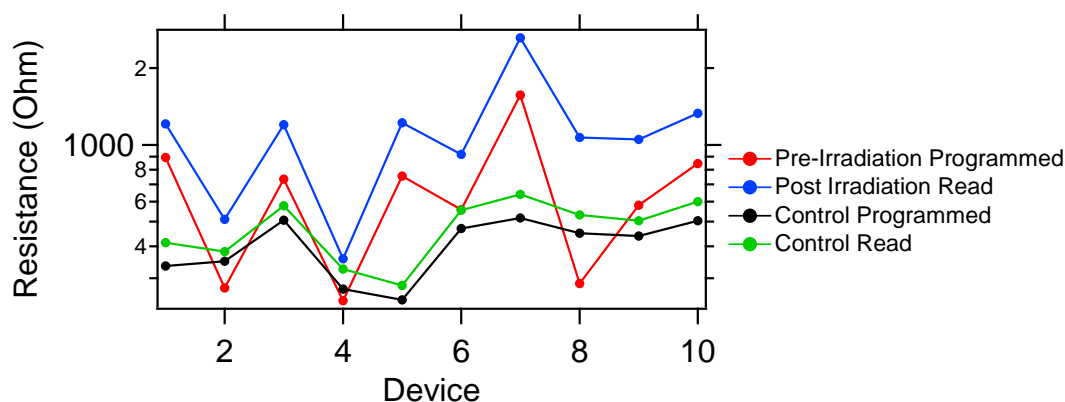
Figure 5.7: Plot of Resistances for Ge$_2$Se$_3$/SnSe/Ag Stack Irradiated and Control Devices with a Programming 1 mA Compliance Current.

A compliance current of 1 mA programmed all devices around 1000 Ω or less, as shown in Figure 5.7. The time control devices show no significant change in resistance after 3.75 hrs. The control read values follow the programmed value. The irradiated devices also maintain the low resistance state within a few hundred ohms, as seen in Figure 5.8. There is not a significant effect on the devices due to time or radiation when programmed at 1 mA.
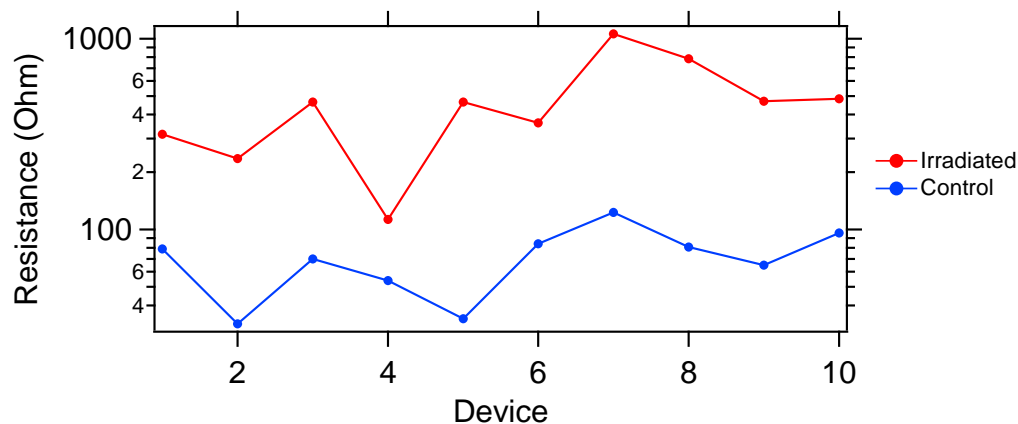
Figure 5.8: Plot of Difference in Programmed Resistance and Read Resistances for Ge₂Se₃/SnSe/Ag Stack Irradiated and Control Devices with a Programming 1 mA Compliance Current.

5.2.3 Comparison of GeTe/SnSe/Ag and Ge₂Se₃/SnSe/Ag Devices Immunity to Radiation

The Ge₂Se₃/SnSe/Ag device had greatest retention over time when programmed with 1 mA compliance current. These devices appeared to be unaffected by the radiation and maintained the low resistance state.

The GeTe/SnSe/Ag irradiated devices had the best low resistance state retention with a 100 nA programming current. The control devices did not behave as ideally, but the variability can be attributed to other complications from ESD effects.   However, the control devices that did switch with a 1 mA programming current had better retention of the low resistance state. The irradiated devices programmed with 1 mA compliance current had good retention with only one device increasing by an order of magnitude, as seen in Figure 5.4. Each device had good retention after approximately 3.5 hrs when programmed with 1 mA compliance current.

5.3 Electrical Testing and Measurements of Radiation Effects on Device Programming Parameters

These set of virgin devices were cleaved from the same wafer into pieces, and only one device was probed from each piece. The cleaved wafer pieces were centered on the chuck under the radiation source, and probe tips were placed down onto pads. The devices were exposed to a dose rate of 286 rad(SiO_2)/s and 283 rad(SiO_2)/s for GeTe and Ge_2Se_3 devices, respectively. After a specific time, 17.4 minutes for GeTe and 17 minutes for Ge_2Se_3 devices, yielded a total ionizing dose of 300 krad(SiO_2). At which time, the W/E/W cycle was initiated while the device continued to be irradiated. The radiation source was shut off after a total of 18 minutes per device. The programming currents used are 100 nA, 1μA, 10 μA, and 100 μA. The power is calculated by multiplying the threshold voltage (1st, 2nd or erase) by the current at that potential. The irradiated results are compared to control devices programmed with the same compliance currents on the Aracor probe station.

5.3.1 Total Ionizing Dose Effects on Programming GeTe/SnSe/Ag Devices

The GeTe/SnSe/Ag devices described in Chapter 2 are used in the following tests. There were two to four virgin devices programmed, one from each individual wafer pieces at each compliance current of 100 nA, 1μA, 10 μA, 100 μA, and 1 mA for both control and irradiated devices.

The average threshold voltages are shown in Figure 5.9 for both the irradiated and control devices. Bars above and below the average value are high and low, respectively.
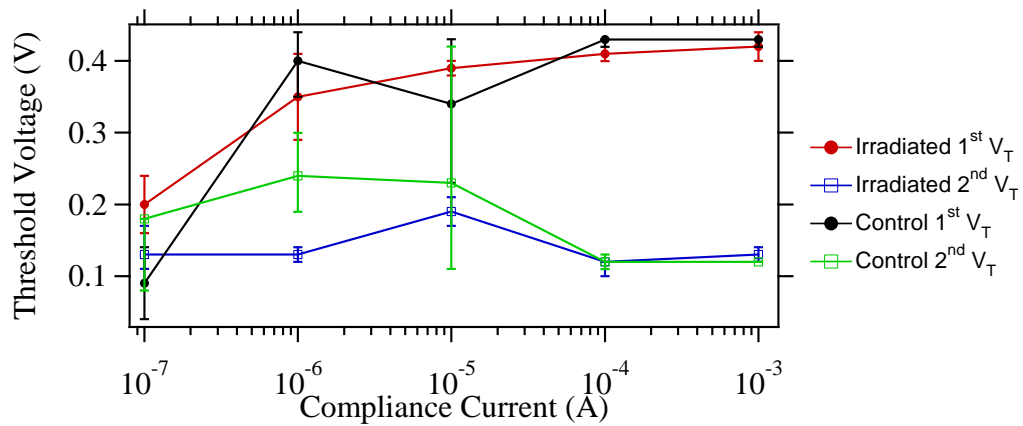
Figure 5.9: 1ˢᵗ and 2ⁿᵈ Threshold Voltages for Irradiated and Control GeTe/SnSe/Ag Devices.

The threshold voltages of the irradiated devices are similar to the control devices as seen in Figure 5.9. The V_{T2} values are less than the V_{T1} values. The V_{T1} increases with an increase in compliance current. This can be attributed to the device having the additional potential before reaching the compliance current to create additional silver conductive pathways. The 100 nA control device V_{T1} is the voltage at which the compliance current was reached. The devices were already in a low resistance state and could not be programmed lower with 100 nA programming current. The erase sweep did increase the resistance of the device and therefore there is a V_{T2} from the second write sweep.

The resistance values for the irradiated and control devices at each compliance current is shown in Figure 5.10 and listed in Table 5.1.
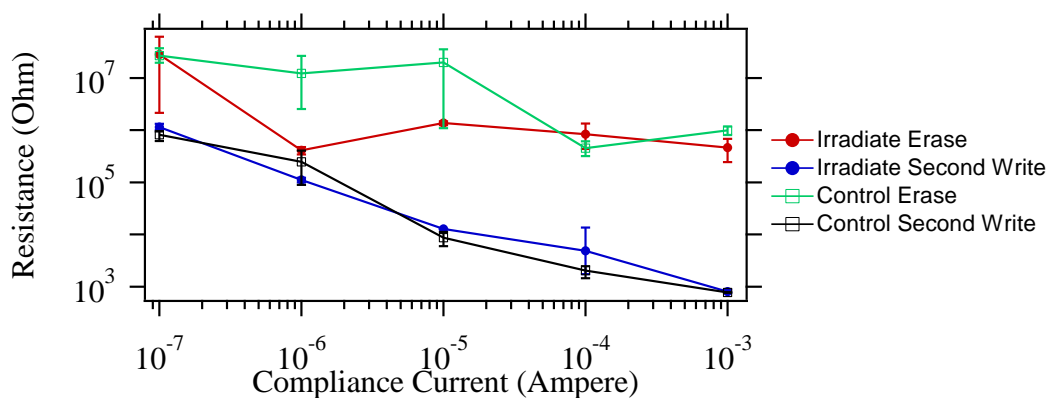
Figure 5.10: Write and Erase Resistances for Irradiated and Control GeTe/SnSe/Ag Devices.

The write resistance for both the irradiated and control devices follow the same trend: a decrease in resistance with increase of compliance current as seen in Figure 5.10. The values are very similar, and no radiation effect is evident on the write resistances. The erase resistances of both irradiated and control devices are similar at each extreme of the compliance current spectrum. The irradiated erase resistance is approximately an order of magnitude less than the control resistance when programmed with 1 μA and 10 μA compliance currents. The initial resistance values of the devices, listed in Table 5.1, have an average initial resistance of $3x10^7$ Ω compared to $6x10^6$ Ω of the control devices. This would suggest a possible radiation effect on the virgin devices. However, that is not the case; the initial resistance values of the same devices from a different part of the wafer have an even higher initial resistance of $2x10^8$ Ω, as mentioned in Table 4.6. The greater initial resistance of the irradiated devices is the reason there is a V_{T1}, because the devices did program into a lower resistance state with 100 nA programming current after the first write sweep. The 100 nA control devices do not have a V_{T1} because the initial

value was the same as the 1st write resistance. However, the control devices were put in

an even higher resistance state of 2.7x10^7 Ω after the erase sweep. The greater erase

resistance produced a V_{T2} because there is approximate 1.5 orders of magnitude

difference between the two resistances.

Table 5.1: Typical Values for GeTe/SnSe/Ag Device Programmed with: 100 nA, 1 μA, 10 μA, 100 μA, and 1 mA Compliance Currents. (-) No Measureable Threshold Voltage

Program Current	100 nA Irradiated/ Control	1 μA Irradiated/ Control	10 μA Irradiated/ Control	100 μA Irradiated/ Control	1 mA Irradiated/ Control
Initial Resistance (Ω)	2.2×10^7/ 1.1×10^6	5.6×10^6/ 6.3×10^6	4.5×10^7/ 1.7×10^7	3.4×10^7/ 4.3×10^6	7.1×10^7/ 9.6×10^5
1st Write Resistance (Ω)	1.3×10^6/ 1.0×10^6	7.4×10^4/ 1.4×10^5	1.4×10^4/ 1.4×10^4	5.1×10^3/ 2.3×10^3	8.3×10^2/ 8.1×10^2
Erase Resistance (Ω)	2.8×10^7/ 2.7×10^7	4.1×10^5/ 1.2×10^7	1.4×10^6/ 2.0×10^7	8.3×10^5/ 4.5×10^5	4.6×10^5/ 9.9×10^5
2nd Write Resistance (Ω)	1.2×10^6/ 8.2×10^5	1.1×10^5/ 2.5×10^5	1.3×10^4/ 8.6×10^3	4.9×10^3/ 2.0×10^3	8.0×10^2/ 7.7×10^2
1st Threshold Voltage (V)	0.2/(-)	0.35/0.40	0.39/0.34	0.41/0.43	0.42/0.43
Erase Voltage Threshold (V)	-0.29/-0.28	-0.19/-0.40	-0.19/-0.23	-0.32/-0.24	-0.33/-0.36
2nd Threshold Voltage (V)	0.13/0.12	0.13/0.24	0.19/0.23	0.12/0.12	0.13/0.12
Power at 1st Threshold (W)	6.6 n/ (-)	71.4 n/ 80 n	125 n/ 211 n	200 n/ 694 n	102 n/1 μ
Power at Erase Threshold (W)	285 n/ 107 n	2.6 μ/ 770 n	1.6 μ/ 3.2 μ	21.9 μ/ 24.5 μ	115 μ/ 135 μ
Power at 2nd Threshold (W)	722 p/ 833 n	56 n/ 70.3 n	163 n/ 76 n	55.3 n/ 53.4 n	107 n/ 84.3 n

The power calculation as described in Chapter 1 of both irradiated and control devices at each threshold are all very similar. The largest difference is the power at the 1st thresholds of both 100 μA and 1 mA programmed devices. This difference does make sense when the initial resistances are analyzed. The 1 mA irradiated device had an initial resistance of 7.1×10^7 Ω whereas the control devices had an initial resistance of 9.6×10^5 Ω. Both the control and irradiated devices had 1st write resistances of 10^2 Ω. The same correlation can be seen with the 100 μA programmed devices.

An example sweep of 10 μA programmed devices, irradiated and control, is seen in Figure 5.11. All of the sweeps are very similar among the compliance current regimes. The slight voltage and current variations seen between the control and irradiated devices are also evident within control samples as well.
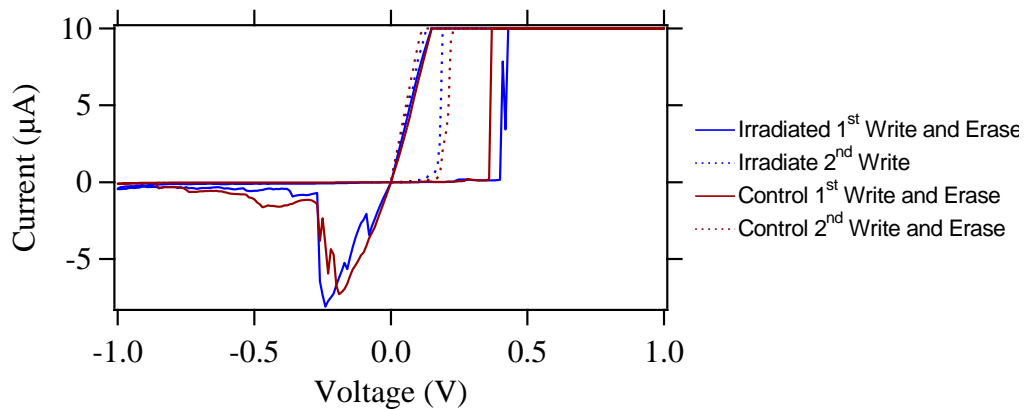
Figure 5.11: Representative DC Sweep Traces of Control and Irradiated GeTe/SnSe/Ag Devices while Programming with 10 μA Compliance Current.

5.3.2 Total Ionizing Dose Effects on Programming Ge_2Se_3/SnSe/Ag Devices

The Ge_2Se_3/SnSe/Ag devices described in Chapter 2 are used in the following

tests. There were two to four virgin devices programmed at each compliance current of

100 nA, 1μA, 10 μA, 100 μA, and 1 mA, each on individual wafer pieces for both control

and radiation testing. The threshold voltages and resistance values for Ge_2Se_3/SnSe/Ag

devices are shown in Figure 5.12 and Figure 5.13, respectively.
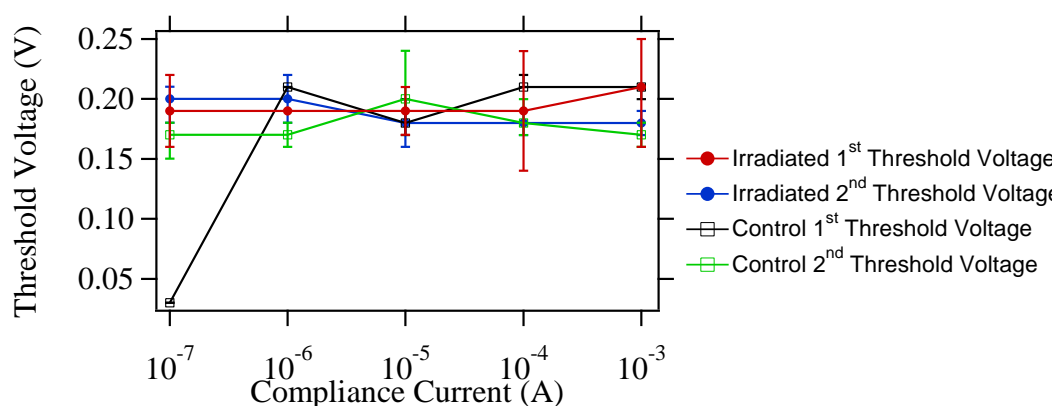
Figure 5.12: 1st and 2nd Threshold Voltages for Ge_2Se_3/SnSe/Ag Devices During Irradiation and Non-Irradiated Controls.

All threshold voltages are within approximately 50 mV of each other as seen in

Figure 5.12. The outlier 100 nA control device value of 0.03 V is the voltage when the

compliance current was reached. The devices did not program with 100 nA compliance

current into a lower resistance state due to the device already being essentially 'On' at

that current/voltage. However, the erase sweep did increase the resistance to turn the

device 'Off,' which then a distinct V_{T2} is seen when the devices turn 'On' again from the

second write sweep. The irradiated devices do have an initial higher resistance than the

control devices as listed in Table 5.2. The greater initial resistance of the irradiated

devices showed switching to a lower resistance during the 1st write sweep, producing a

V_{T1} for all compliance currents. The higher initial resistance values of the irradiated

devices are similar to the Ge_2Se_3/SnSe/Ag device initial resistance values from Table 4.2.

The lower initial resistance values of the control devices in this study can possibly be

attributed to the location on the wafer from where the devices were cleaved.
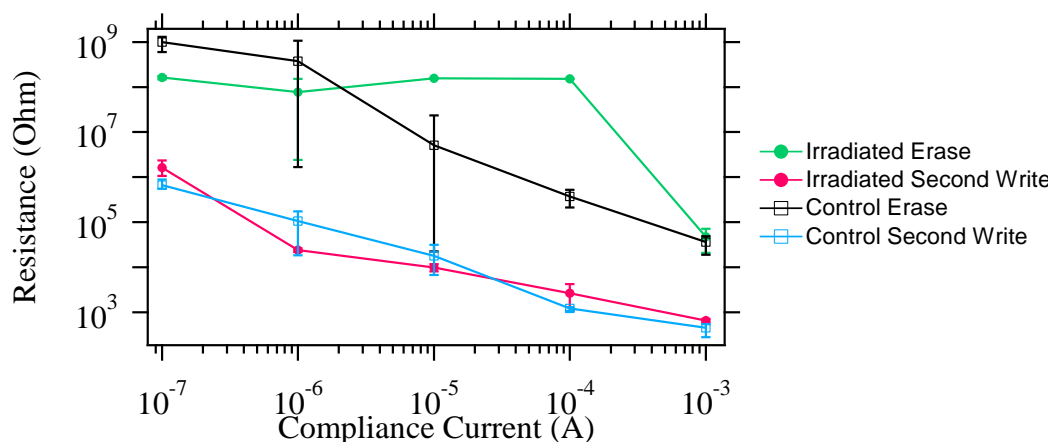
Figure 5**.13: Write and Erase Resistances for Ge$_2$Se$_3$/SnSe/Ag Devices During Irradiation and Non-Irradiated Controls.**

Both control and irradiated programming have a decrease in write resistance with

increased compliance current as seen in Figure 5.13. The erase resistances also follow

the same trend as the write resistances. The difference is that the irradiated devices are

more fully erasing into a higher resistance state with 10 µA and 100 µA programming

than the control devices. This is likely an anomaly due to the lack of devices tested. The

average difference of approximately two orders of magnitude between the write and erase

resistances is still maintained with increased programming current.

Table 5.2: Typical Values for Ge$_2$Se$_3$/SnSe/Ag Device Programmed with a 1 mA Compliance Current. (-) Symbolizes No Switch in Resistance at Threshold.

Program Current	100 nA Irradiate/ Control	1 µA Irradiated/ Control	10 µA Irradiated/ Control	100 µA Irradiated/ Control	1 mA Irradiated/ Control
Initial Resistance (Ω)	1.7×10^8/ 6.4×10^5	1.1×10^8/ 2.7×10^5	1.4×10^8/ 1.0×10^5	5.6×10^7/ 2.7×10^5	1.1×10^8/ 2.6×10^7
1st Write Resistance (Ω)	1.5×10^6/ 2.0×10^5	2.2×10^4/ 9.5×10^4	9.9×10^3/ 1.2×10^4	3.2×10^3/ 1.1×10^3	8.3×10^2/ 6.9×10^2
Erase Resistance (Ω)	1.6×10^8/ 9.9×10^8	7.7×10^7/ 3.7×10^8	1.6×10^8/ 5.1×10^6	1.5×10^8/ 3.7×10^5	4.7×10^4/ 3.6×10^4
2nd Write Resistance (Ω)	1.6×10^6/ 6.7×10^5	2.4×10^4/ 1.1×10^5	9.8×10^3/ 1.8×10^4	2.6×10^3/ 1.2×10^3	6.6×10^2/ 4.6×10^2
1st Threshold Voltage (V)	0.19/(-)	0.19/0.21	0.19/0.18	0.19/0.21	0.21/0.21
Erase Threshold Voltage (V)	-0.07/ -0.13	-0.11/ -0.16	-0.07/ -0.09	-0.12/ -0.10	-0.36/ -0.37
2nd Threshold Voltage (V)	0.20/ 0.17	0.20/ 0.17	0.18/ 0.16	0.18/ 0.18	0.18/ 0.17
Power at 1st Threshold (W)	258 p/ (-)	541 n/ 7.0 n	1.1 n/ 448 n	1.2 µ/ 2.8 µ	621 n/ 1.1 µ
Power at Erase Threshold (W)	204 p/ 134 n	133 p/ 682 n	82 n/ 503 n	7.0 µ/ 4.2 µ	332 µ/ 367 µ
Power at 2nd Threshold (W)	242 p/ 140 p	181 p/ 5.2 n	75 p/ 8.5 n	140 p/ 609 n	143 µ/ 1.2 µ

5.3.3 Comparison of GeTe/SnSe/Ag and Ge$_2$Se$_3$/SnSe/Ag Devices Total Ionizing Dose Effects Due to Radiation Exposure While Programming.

Both types of devices do not show a definitive influence on the voltage thresholds or the write/erase resistances due to the radiation exposure when compared to their respective control devices. Also, both layered devices showed a variation in initial resistance due to possible processing variation across the wafer.

5.4 Conclusion

In this chapter, we did an initial investigation of TID effects on programmed GeTe/SnSe/Ag and Ge$_2$Se$_3$/SnSe/Ag, as well as the TID effects on programming while devices were irradiated. Overall, the initial study shows no significant effect on the operation of the devices due to radiation exposure. However, changes to the experimental set up would need to be adjusted so as to minimize electrostatic discharge effects from handling the devices.

CHAPTER 6**:** CONCLUSION

6.1 Introduction

The electrical characterization results for the metal-selenide/germanium-

chalcogenide/Ag ion conducting devices are summarized in this chapter. This is followed

by a discussion on proposed future work.

6.2 Summary of Work

6.2.1 Metal-Selenide Layer Comparisons

In this work, devices were fabricated in which the metal-selenide layer was varied

to determine if the metal-selenide layer had an influence on the electrical properties of the

ion-conducting device.   The metal-selenide layers tested were Sb_2Se_3, SnSe, PbSe,

In_2Se_3, and Ag_2Se. The DC programming threshold voltages and the programmed

resistance states were measured for each type of device.

The average threshold voltage was found to vary depending upon the metal-

selenide layer material.   From highest to lowest, V_{T1} are devices with the metal layers:

Sb_2Se_3, In_2Se, PbSe, SnSe, and Ag_2Se with values of 0.31 V, 0.27 V, 0.24 V, 0.18 V, and

0.13 V, respectively. An overall trend of a decrease in V_{T1} as the operating temperature

was increased was shown for all metal-selenide layered devices. V_T was found to be

independent of programming current except when compliance current is reached prior to

switching the device. The V_{T2} was lower for all metal-selenide devices except for Ag_2Se,

which remained approximately the same as V_{T1}. It was rationalized that this is likely due to the formation of a permanent channel in the Ge_2Se_3 layer when the device is programmed the first time. Subsequent programming is thought to use this channel for the Ag^+ migration upon application of a potential across the device. The similarity of the V_T's after initial programming supports this line of reasoning.

The write resistance was found to be independent of programming temperature except for the $Ge_2Se_3/Ag_2Se/Ag$ device in which the resistance decreased as a function of programming temperature. In all device types, the first and second write resistances were similar. The write resistance was dependant on programming current and had approximately one order of magnitude drop in resistance for each decade of increase in programming current.

For each device type, except the $Ge_2Se_3/Ag_2Se/Ag$ device, the erase resistance state showed an overall decrease in resistance with an increase in temperature. This trend was also observed in the case of erasing a device that had been programmed at the 1 mA programming current. When a device had previously been programmed with a 1 mA programming current, the subsequent erase resistance is significantly lower than for the cases of the other programming currents. In the case of the $Ge_2Se_3/Ag_2Se/Ag$ device, the erase resistance was unaffected by programming current.

6.2.2 Germanium-Chalcogenide Layer Comparisons

The germanium-chalcogenide layer was varied between Ge_2Se_3 and GeTe in the SnSe-based devices in order to explore the role of the chalcogenide influence on Ag^+ migration. The V_{T1} of GeTe is approximately double that of Ge_2Se_3, and both decrease with an increase in temperature. The electric field at the first threshold for GeTe was twice that of Ge_2Se_3.

The Ge_2Se_3 devices had a greater erase resistance of 10^{11} Ω when programmed with 10 µA or less at 23 °C compared to the erase resistance of GeTe, which was 10^6 Ω. GeTe had a slightly higher write resistance than Ge_2Se_3, but both devices still had a decrease in write resistance with an increase of programming current.

Overall the devices exhibited little or no post-thermal effects.

6.2.3 Total Ionizing Dose Effect Comparisons

The total ionizing dose effects on programming a device and in retention of a programmed resistance state were investigated on Ge_2Se_3/SnSe/Ag and GeTe/SnSe/Ag devices using a W target X-ray source at the Air Force Research Laboratory at Kirkland, AFB.

The total ionizing dose radiation exposure of 500 krad(SiO_2) did not affect the programmed low resistance state of either Ge_2Se_3/SnSe/Ag or GeTe/SnSe/Ag devices. Both devices were shown to have good retention after 3.5 hours.

The total ionizing dose radiation exposure of 300 krad(SiO_2) during device programming did not have a clear influence on the voltage thresholds or the write/erase resistances when compared to the respective control devices.

6.3 Future Work

In future work, pulsed electrical measurements that explore the AC switching characteristics of the devices and the data retention (i.e., resistance state lifetime) as a function of applied programming signal should be studied.   There is a need to determine the optimal pulse conditions, which include pulse width (time) and amplitude (applied potential), that increases cycling and extends the data retention when studying how pulse programming influences device operation. Additional electrical tests that need to be performed include the data retention of both high and low resistance states when a low potential is applied across the device at intervals over an extended period of time. This type of testing is considered a "read" disturb test.   These are all important factors when characterizing these devices.

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