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Limitations of Poole–Frenkel Conduction in Bilayer HfO_2/SiO_2 MOS Devices

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***Abstract*—The gate leakage current of metal–oxide–semiconductors (MOSs) composed of hafnium oxide (HfO_2) exhibits temperature dependence, which is usually attributed to the standard Poole–Frenkel (P–F) transport model. However, the reported magnitudes of the trap barrier height vary significantly. This paper explores the fundamental challenges associated with applying the P–F model to describe transport in HfO_2/SiO_2 bilayers in n/p MOS field-effect transistors composed of 3- and 5-nm HfO_2 on 1.1-nm SiO_2 dielectric stacks. The extracted P–F trap barrier height is shown to be dependent on several variables including the following: the temperature range, method of calculating the electric field, electric-field range considered, and HfO_2 thickness. P–F conduction provides a consistent description of the gate leakage current only within a limited range of the current values while failing to explain the temperature dependence of the 3-nm HfO_2 stacks for gate voltages of less than 1 V, leaving other possible temperature-dependent mechanisms to be explored.**

***Index Terms*—Carrier transport, cryogenic, hafnium oxide (HfO_2), high-k dielectric, metal–oxide–semiconductors (MOS), Poole–Frenkel (P–F).**

I. Introduction

THE NEXT generation of metal–oxide–semiconductor (MOS) field-effect transistors (MOSFETs) requires an increase in gate-oxide capacitance (per unit area) that can no longer be accommodated by reduction in the thickness of the typical gate oxides. High dielectric constant (high-k) oxides have received considerable attention as a solution to reduce gate leakage current while increasing the gate-oxide capacitance. Hafnium oxide (HfO_2) is the prime candidate for replacing silicon dioxide (SiO_2) and has recently been introduced in production. One of the continued challenges in the use of HfO_2 is the strong temperature dependence of the leakage current as compared with that of SiO_2 [1].

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For high-temperature measurements (300 K to ~500 K), many studies of electron transport in HfO_2 have attributed the gate leakage current to the Poole–Frenkel (P–F) conduction mechanism of electrons in HfO_2 [2]–[5]. Although P–F emission is widely employed as an explanation of the temperature dependence of gate leakage current in HfO_2 (and high-k dielectrics, in general), significant discrepancies have arisen in the reported trap-energy barrier heights (e.g., 0.35 eV [2], 0.68 eV [6], 1.11–1.36 eV [7], and 1.5 eV [5]). While the inconsistencies in the reported barrier heights may be attributed to different growth methods, pre- and postgrowth processing, and device technologies used, this paper explores several fundamental challenges that are present in extracting trap-energy barriers in HfO_2 gate stacks based on using the standard P–F model.

This paper examines whether the standard P–F model can describe charge transport over a wide temperature range in HfO_2/SiO_2 bilayer dielectric stacks (6 K–400 K). In this paper, P–F analysis is applied to data collected over a broad range of temperatures and stress-free voltages. Particular attention is given to the following: 1) the P–F derived trap-energy barrier height's dependence on HfO_2 thickness; 2) calculation of the electric field in the oxide layer in which P–F conduction is suspected to take place; and 3) whether P–F transport occurs at typical MOSFET use conditions. The analysis of the data from HfO_2/SiO_2 bilayer dielectric stacks reveals that the P–F behavior only occurs at very narrow temperature and electric-field ranges. Ignoring these limitations may lead to a variety of reported trap-barrier-height values of which several are physically unfounded. Furthermore, the analysis shows a leakage-current thickness dependence, which is not consistent with the P–F model. It is also found that certain approximations used to calculate the electric field in the dielectric can lead to significant errors in the P–F analysis. The data further brings to light that the standard P–F conduction model is unsuitable at the use conditions for highly scaled high-k dielectrics in MOS devices. The presented evidence suggests that the P–F model may be insufficient to explain transport behavior in high-k dielectric stacks.

II. P–F Transportation Mechanism

The standard P–F mechanism was initially defined in a short paper by Frenkel in 1938 [8]. Frenkel's paper describes how the electron trap barrier height (ϕ) is reduced in the presence of an electric field (E_{ox}) by

$$\Delta q\phi = \beta\sqrt{E_{\mathrm{ox}}} \tag{1}$$

where the P–F constant β is given by [9]

$$\beta = \sqrt{\frac{q^3}{\pi\varepsilon_0\varepsilon_r}} \tag{2}$$

and q, ε_0, and ε_r are the electron charge, permittivity of free space, and the high-frequency dielectric constant, respectively [10], [11]. The derivation of the energy-potential lowering effect (1) depends on the hydrogenic potential. That is, the standard P–F mechanism incorporates the concept of a hydrogenic impurity for which the ionization energy potential is determined using the effective mass approximation [12]–[14]. The hydrogenic impurity includes both a charged ion impurity and a charged trapped carrier, which interact with each other. In his model, Frenkel only considered electrons and donor traps [8]. However, in the effective-mass approximation, the difference between the hydrogenic ionization energy potential for an electron and hole is simply the effective mass of the respective carriers. Hence, there is no reason why the P–F model cannot be applied to holes as it is applied to electrons.

According to Frenkel, for trapping to occur, the impurity must be ionized in the nontrapped state and neutral in the trapped state [10]. Since Frenkel's publication, the literature contains numerous papers of assorted derivations of P–F conduction (e.g., [9]), applications to various materials, and discussions on its limitations (e.g., [14] and [15]). A widely accepted mathematical expression for the standard P–F conduction $(J_{\rm FP})$ can be written as

$$J_{\rm FP} = CE_{\rm ox}e^{-\frac{q\phi-\beta\sqrt{E_{\rm ox}}}{\xi KT}} \tag{3}$$

where C, K, T, and ξ, are a constant, Boltzmann's constant, temperature, and a factor that depends on acceptor compensation [11], [15], respectively. The value of ξ is usually between one and two. In Frenkel's original paper, $\xi = 2$. In much of the literature, $\xi = 1$ (e.g., [6], [7], and [16]–[21]) which corresponds to heavily compensated traps [11]. The standard P–F conduction mechanism does not define how the traps are filled, only how they are emptied. The resulting P–F detrapping process is assumed to be the limiting step in the conduction mechanism. Traps are usually considered to be filled through quantum–mechanical tunneling [22]. An example depicting the P–F conduction path in HfO_2 with a SiO_2 interfacial layer (IL) is shown in Fig. 1.

Identifying the P–F transport can be achieved by constructing a P–F plot where (3) is linearized by plotting $\ln(J/E_{\rm ox})$ versus $E_{\rm ox}^{1/2}$. If the P–F plot shows that the data are linear, P–F conduction is inferred. The slope of the line yields $\beta/\xi KT$ from which the high-frequency dielectric constant can be extracted if ξ is known; however, usually it is assumed to be one. If C in (3) is known, ϕ can be extracted from the y-intercept

$$\ln(C) - \frac{q\phi}{\xi KT}. \tag{4}$$

If C is not known, data from more than one temperature can be used to eliminate C.

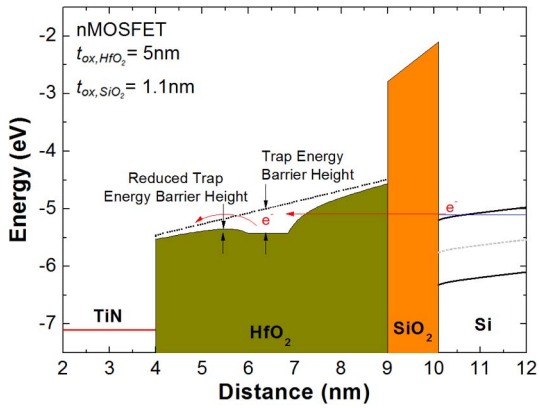

Fig. 1. Simulated energy-band diagram showing the lowering of the trap potential barrier height in the presence of an electric field in HfO_2 with a SiO_2 IL. The dashed line represents the conduction band in the HfO_2 without the trap. The diagram was created using [23], a ϕ of 0.45 eV, and a relative high-frequency dielectric constant of 7.8; values extracted from the data and discussed in Section IV. The trap potential is located in the middle of the HfO_2 layer.

An alternative approach to extracting ϕ is achieved by following [6] and [18] in which (3) is linearized against the inverse of temperature as

$$\ln\left(\frac{J_{\rm FP}}{E_{\rm ox}}\right) = \ln(C) - \frac{q\phi-\beta\sqrt{E_{\rm ox}}}{\xi K}\frac{1}{T} \tag{5}$$

which predicts Arrhenius behavior. The slope of the resulting line is proportional to the reduced trap barrier height (ϕ_r), $q\phi - \beta E_{\rm ox}^{1/2}$. Note that the reduced trap-energy barrier height decreases with increasing electric field. Extracting the slope in (5) at various electric fields yields ϕ which can be found by extrapolating $E_{\rm ox}^{1/2}$ to zero. This latter approach to finding ϕ is the method used in this paper.

Regardless of the method utilized, the value of the electric field must be specific to the dielectric layer under consideration [1]. Calculating the electric field has been treated in various ways in the literature necessitating a discussion on how the electric-field calculation affects the extraction of ϕ. Three common methods of calculating the electric field in a dual-dielectric layer stack (shown here for layers composed of HfO_2 and SiO_2) can be written in the form of (6) (e.g., [6] and [16]), (7) (e.g., [22]), and (8) (e.g., [19] and [24]) [1]

$$E_{\rm ox} = \frac{V_{\rm Gate} - V_{\rm FB}}{t_{\rm ox,physical}} \tag{6}$$

$$E_{\rm ox,HfO_2} = \frac{V_{\rm Gate} - V_{\rm FB}}{t_{\rm ox,HfO_2}}\frac{C_{\rm ox,SiO_2}}{C_{\rm ox,HfO_2} + C_{\rm ox,SiO_2}} \tag{7}$$

$$E_{\rm ox,HfO_2} = \frac{V_{\rm Gate} - V_{\rm FB} - \phi_s(V_{\rm Gate})}{t_{\rm ox,HfO_2}}\frac{C_{\rm ox,SiO_2}}{C_{\rm ox,HfO_2} + C_{\rm ox,SiO_2}} \tag{8}$$

where $V_{\rm Gate}$, $V_{\rm FB}$, $t_{\rm ox}$, $C_{\rm ox}$, and ϕ_s are the gate voltage, flatband voltage, oxide thickness, oxide capacitance, and surface potential in the semiconductor, respectively. Equation (6) treats the dual dielectric as a single dielectric. Equation (7) improves the electric-field calculation in the HfO_2 by considering the mismatch in the dielectric constants. Equation (8) is a further refinement accounting for the potential drop in the silicon (ϕ_s).

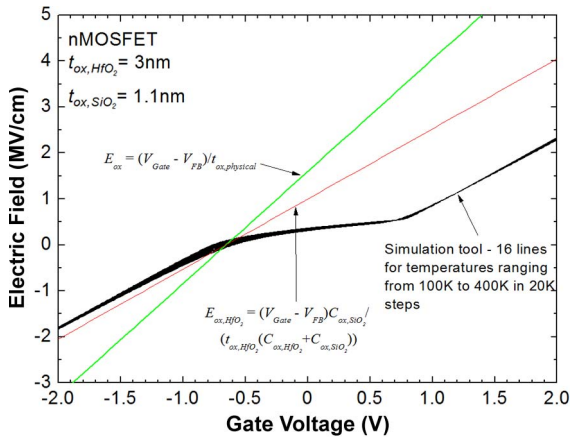

Fig. 2. Calculated electric field in a $TiN/HfO_2/SiO_2/Si$ gate stack using (6) and (7) and [23] and [26] for (8). Simulations for temperatures ranging from 100 K to 400 K are shown [23]. After [1].

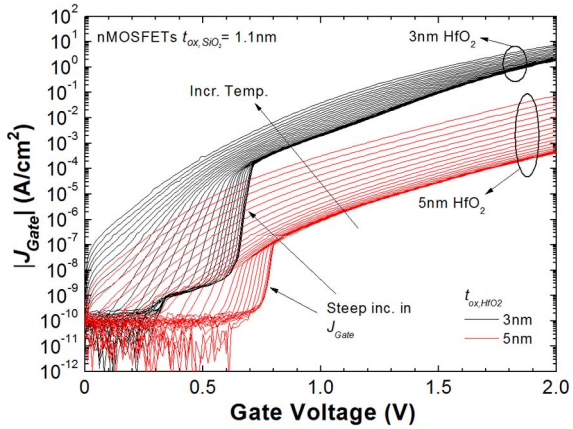

Fig. 3. Typical gate leakage currents for 3- and 5-nm HfO_2/SiO_2 nMOSFETs. Significantly higher temperature dependence in 5-nm HfO_2/SiO_2 gate leakage current is observed compared with the 3-nm HfO_2/SiO_2. A steep increase in the gate leakage current with respect to the gate voltage is observed near the threshold voltage.

The accuracy of (8) depends on the accuracy to which ϕ_s is known. One method of reducing the error by accounting for the potential drop in the silicon is the use of simulation software (e.g., [23] and [25]) from which ϕ_s or $E_{\mathrm{ox,HfO2}}$ can be extracted. Fig. 2 shows a comparison of the calculated electric field using (6) and (7), and the Boise State University energy-band simulation tool to account for ϕ_s [23], [26].

As observed in Fig. 2, there is a large difference between the calculated electric field using (6)–(8). As will be shown, the large difference in the calculated values of electric field using (6)–(8) has a substantial impact on the calculated ϕ. Fig. 2 also shows the electric field in HfO_2 as a function of gate voltage for temperatures ranging from 100 K to 400 K as calculated by [23] and [26]. It has been shown that a minimal variation in the electric field occurs below 100 K [1]. The electric field shows little variation with temperature at the simulated doping concentration $(2.5 \times 10^{18}\ \mathrm{cm}^{-3})$. Because the electric field remains nominally unchanged with respect to temperature, the temperature dependence of ϕ_s for highly doped substrates can be assumed constant. From this exercise, Fig. 2 shows that the use of the simplifying equations of (6) and (7) can lead to substantial error when calculating the electric field as compared with (8).

III. Experimental Procedure

The devices used in this study are n/pMOSFETs fabricated using a standard CMOS process flow including a 10-s 1000-°C anneal for dopant activation and 480-°C forming-gas anneals. The gate stack of each MOSFET consists of a titanium nitride (TiN) metal gate and a dielectric bilayer of either 3 nm or 5 nm of HfO_2 grown by atomic layer deposition on a 1.1-nm chemically grown SiO_2 IL. A more detailed description of the fabrication process is presented in [27]. Control devices fabricated with a 2-nm SiO_2 gate dielectric are used for comparison. In order to increase the signal to noise ratio in the gate-leakage-current measurements, large MOSFETs of 30-μm/30-μm (width/length) and 50-μm/50-μm dimensions were tested. A Janis Research custom-built variable-temperature probe station (5.6 K–450 K) with actively cooled Kelvin probes, to limit heat injection into the devices, was used for all measurements. A Keithley 4200SCS with remote preamps was interfaced with the variable-temperature probe station. Gate-leakage-current measurements were performed for the electron-substrate injection regime (positive gate biases). The electric-field calculations were performed using [23] and [26] and were calibrated using the flatband voltage and material parameters extracted using capacitance–voltage measurements in [27].

IV. Results and Discussion

Based on the P–F model, varying the thickness of the HfO_2 in the HfO_2/SiO_2 gate stack should not have an effect on the extracted trap-energy barrier height (ϕ). To test this model's prediction, the leakage current through the 3- and 5-nm thick HfO_2/SiO_2 gate stack was examined as a function of applied voltage over a wide range of temperatures. Typical gate leakage currents for nMOSFETs composed of 3-nm HfO_2 and 5-nm HfO_2 for temperatures ranging from 6 K to 400 K are shown in Fig. 3 for electron-substrate injection. As expected, the gate-leakage-current density (J_{Gate}) for the 5-nm HfO_2 stack is decades lower than the 3-nm HfO_2 stack. For both nMOSFETs and pMOSFETs (not shown), the gate-leakage-current rate of increase with temperature is higher for the 5-nm HfO_2 than for the 3-nm HfO_2.

Another intriguing aspect of Fig. 3 is the steep increase in the gate-current density with gate voltage near a gate bias of 0.5 V. For pMOSFETs (not shown), a corresponding steep increase in the gate leakage current is observed at negative polarities [1]. The steep decrease in gate leakage current at low gate biases is due to the decrease of minority carriers below the threshold voltage resulting in supply-limited transport [1]. Above the threshold voltage, the gate leakage current is dominated by the transport path through the dielectric, whether due to tunneling, defect-mediated tunneling, or some other transport mechanism [1].

Typically, P–F analysis is performed in the transport-path-limited region, as opposed to the supply-limited transport regime, of the gate-leakage-current plot (e.g., voltages above ~0.7 V in Fig. 3). Following the second method for calculating ϕ described in Section II, a $J_{\mathrm{Gate}}/E_{\mathrm{ox,HfO2}}$ P–F plot at various temperatures is shown in Fig. 4. For P–F transport to dominate according to (3), the data in Fig. 4 should be linear. Except for a small electric-field interval, the data in Fig. 4

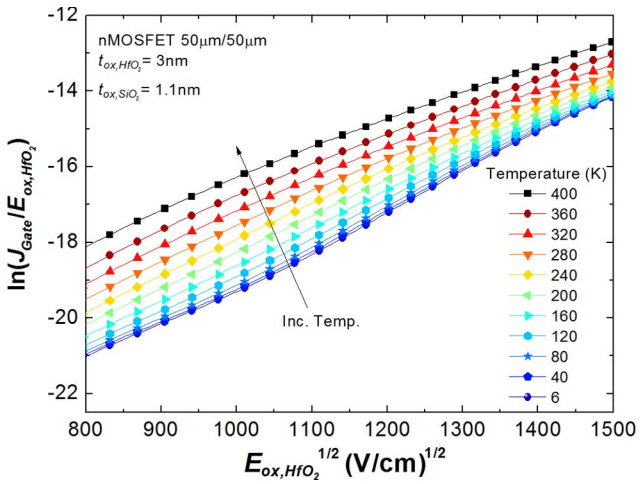

Fig. 4. P–F plot of the gate leakage current of a 3-nm HfO_2 1.1-nm SiO_2 nMOSFET for temperatures ranging from 6 K to 400 K. Most temperatures are not plotted to increase clarity of the data.

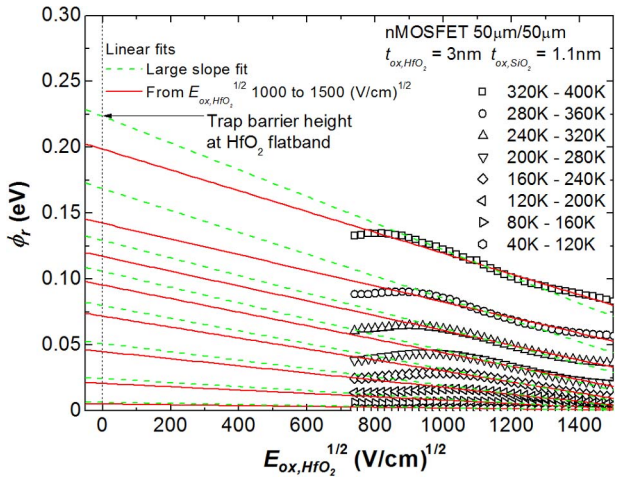

Fig. 6. Reduced trap barrier height (ϕ_r) at various electric-field strengths using eight different temperature ranges from e.g., Fig. 5. ϕ_r at flatband (vertical dashed line), or ϕ, is determined by linear extrapolation, e.g., red (solid) and green (dashed) lines.

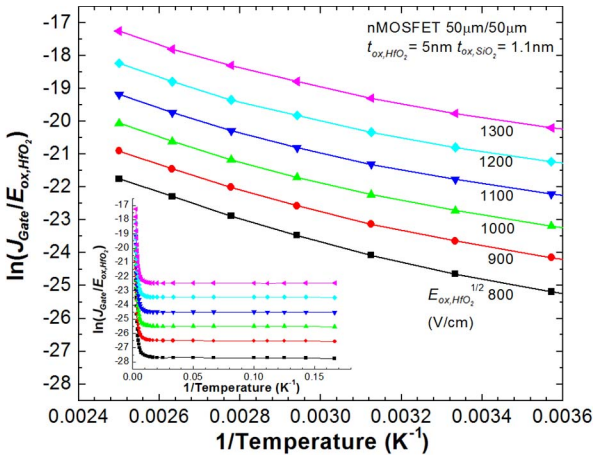

Fig. 5. Arrhenius P–F plot at various electric field strengths of a 5-nm HfO_2 1.1-nm SiO_2 nMOSFET for temperatures 280 K to 400 K. Inset plot is for temperatures 6 K to 400 K.

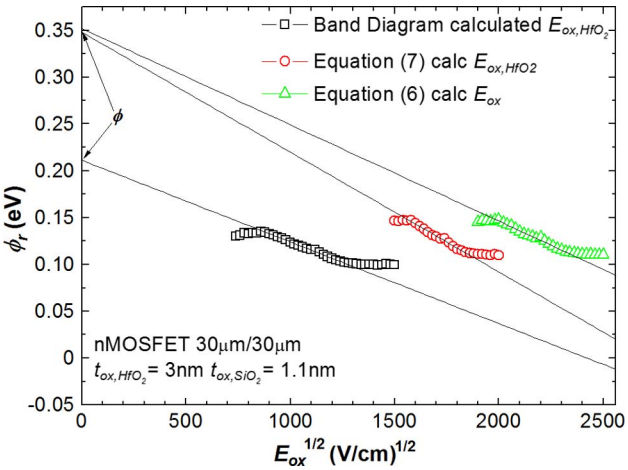

Fig. 7. ϕ extraction using ϕ_r's extracted using the electric field calculated in three different ways. The black lines are linear best fit to the most linear segment of the data

are not linear for the entire electric-field range shown [800 to 1550 $(\mathrm{V/cm})^{1/2}$]. To describe the nonlinear data in a P–F plot, a saturation P–F analysis approach has been proposed in [28] and developed in [15] and [29] whereby Fermi–Dirac statistics are used instead of Maxwell–Boltzmann. In classic P–F, below the saturation voltage, carriers are thermally ionized over the trap barrier. The presence of the electric field assists carriers in overcoming the trap barrier. For voltages at or above the saturation voltage, the trap barrier is reduced to zero, and the Coulombic traps have no effect on the carriers. Saturation P–F dominates when the conductivity $(J_{\mathrm{Gate}}/E_{\mathrm{ox,HfO2}})$ for various temperatures approaches a crossing point, where temperature is not needed for the carrier to overcome the trap potential. However, in this paper, the conductivity data in Fig. 4 is not observed to cross or approach crossing indicating that the P–F saturation is not occurring. Therefore, saturation P–F analysis for the nonlinear data observed in Fig. 4 is not applicable.

To verify whether the P–F transport follows the Arrhenius-type behavior (5), the conductivity $(J_{\mathrm{Gate}}/E_{\mathrm{ox,HfO2}})$ is plotted versus the inverse temperature at various electric fields as shown in Fig. 5. The inset of Fig. 5 displays the entire temperature range examined, whereas Fig. 5 only shows 280 K to 400 K. The entire temperature range shows a strong temperature-dependent region $(T > 200\ \mathrm{K})$ and a weak temperature-sensitive region $(T < 50\ \mathrm{K})$. For the strong temperature-dependent regime, ϕ_r at various electric-field strengths is extracted, assuming $\xi = 1$, and plotted against the square root of the electric field, Fig. 6, in order to extract ϕ. The data in Fig. 5 are not completely linear, and thus, the behavior is not standard P–F. The slope of the data is observed to increase with increasing temperature to the highest temperature (400 K) for which measurements were performed. Therefore, ϕ_r extracted from the data will be dependent on the temperature range used as shown in Fig. 6.

Since the data in the Arrhenius P–F plot in Fig. 5 show a slight curvature with the slope increasing as temperature increases, it is evident that (5), obtained by linearizing (3), cannot be applied to the data. Equation (3) was derived assuming a single trap-energy level, hence, the data do not exhibit a single trap-energy-level behavior. The observed nonlinearity of the

data may stem from several possibilities. One possibility is that several series of linear data with dissimilar slopes (i.e., various trap-energy levels) may exist and combine to form nonlinear data. Another possible explanation may be that the wavefunctions of the traps overlap due to a high defect density. Overlapping of the wavefunctions would lead to the potentials of the traps to overlap which may broaden the distribution of trap-energy barrier heights (ϕ's) [30]. An additional possibility might be attributed to the presence of charged traps (not considered in P–F conduction) that are taking part in carrier transport which is indicative of multivalent traps.

Due to the curvature of the data, only a limited range of data can be analyzed and explained using the standard P–F model. This finding highlights two uncertainties with the P–F model. First, if the data are linear over only a narrow range of temperatures, the extracted ϕ seems physically tenuous. Second, when a narrow range of temperatures is selected for analysis, then the temperatures outside the narrow temperature range are not being considered, thereby indicating that other ϕ's exist.

Regardless of the cause, the curvature in the data in Fig. 5 influences the extracted reduced trap-energy barrier height (ϕ_r) depending on the temperature range used to perform the linear fit. Fig. 6 shows ϕ_r extracted for a 3-nm HfO_2 on 1.1-nm SiO_2 nMOSFET using eight different temperature ranges. To obtain ϕ, ϕ_r is extrapolated to $E_{\mathrm{ox,HfO2}} = 0$ shown by the dashed vertical line in Fig. 6. As shown in Fig. 6, the temperature range used for calculating ϕ_r, as well as the range of electric-field strengths to perform the linear regression fit to extrapolate ϕ, yields significantly different results. The green (dashed) lines in Fig. 6 correspond to extracting ϕ using the slope of the ϕ_r's which would result in the greatest ϕ. The red (solid) lines in Fig. 6 correspond to a linear fit using electric-field strengths ranging from 1000 to 1500 $(\mathrm{V/cm})^{1/2}$. Both red and green lines illustrate the wide distribution of ϕ's that can be extracted. The standard P–F model predicts a constant slope for the data plotted in the manner of Fig. 6. The heterogeneity of the slope in Fig. 6 suggests that P–F conduction is not an appropriate model or is limited to a short electric-field range.

As was alluded to earlier, the method of calculating the electric field in the HfO_2 also has significant effects on the extracted ϕ. Fig. 7 shows the various ϕ_r's extracted using (6), (7), and [23] for calculating the electric field. The linear fits, for extrapolating ϕ, were performed over the largest existing linear range which also resulted in the largest ϕ. Using the simplified equations of (6) and (7) to calculate the HfO_2 electric field results in an overestimation of ϕ ($\sim$0.35 eV) when compared with the electric field calculated by [23] ($\sim$0.21 eV). Fig. 7 thus shows the importance the method of electric-field calculation has on the P–F ϕ.

As was shown in Fig. 3, the temperature dependence of the 5-nm HfO_2 devices differed considerably from the 3-nm HfO_2 devices. This temperature-dependence difference is also observed in the P–F ϕ extraction (Fig. 8). Fig. 8 shows the ϕ_r's for nMOSFETs with 5-nm HfO_2 and 3-nm HfO_2. Similar values were obtained for pMOSFETs. The extracted ϕ for the n/pMOSFETs composed of 5-nm HfO_2 is $\sim$0.45 eV below the HfO_2 conduction band for a low electric-field fit and $\sim$0.35 eV below for a high electric-field fit. The P–F analysis

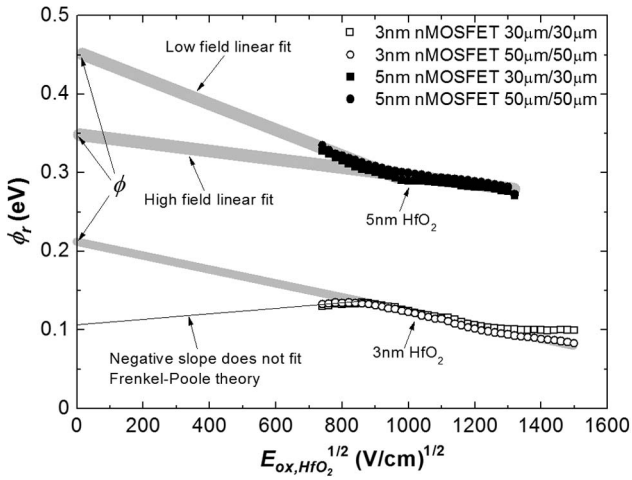

Fig. 8. Electric-field dependence of the ϕ_r (extracted from temperatures ranging from 320 K to 400 K) for the 5-nm HfO_2 and 3-nm HfO_2 nMOSFETs. The thick gray lines represent linear fits to the data. For the 5-nm HfO_2 devices, two linear regimes are observed and give different trap-energy barriers. The thin black linear-fit line for the 3-nm HfO_2 devices shows P–F conduction is not valid in the low-field regime as ϕ_r increases with electric field instead of being reduced.

for n/pMOSFETs composed of 3-nm HfO_2 results in a ϕ of $\sim$0.21 eV below the HfO_2 conduction band. Therefore, the HfO_2 thickness affects the measured ϕ. The similarly calculated ϕ's for n and pMOSFETs verify that the same traps in the HfO_2 are responsible for the gate leakage current whether in nMOS or pMOS configuration and thereby independent of the silicon doping and related processing.

A reason for the thickness dependence of the calculated ϕ may best be understood through Fig. 1. Fig. 1 shows the trap potential of a 0.45-eV trap-energy barrier with a relative high-frequency dielectric constant of 7.8 (a high value) located in the middle of the 5-nm HfO_2 layer. The value of the trap-energy barrier was extrapolated from Fig. 8, while the high-frequency dielectric constant was extracted by calculating β from Fig. 4 using 400 K data and assuming $\xi = 1$. Because the P–F potential is based on the concept of a hydrogenic impurity, the Coulombic potential between the electron and positive trap, shown in Fig. 1, extends over a large distance that is comparable with the HfO_2 layer thickness. Depending on the location of the trap and thickness of the HfO_2, standard P–F conduction may not dominate, and the resulting transport mechanism becomes thickness dependent. P–F analysis, shown in Fig. 8, indicates that the 3-nm HfO_2 layer contains traps with lower ϕ's than the ϕ's extracted for the 5-nm HfO_2. For the high-field regime, the difference observed in ϕ's between the 3- and 5-nm HfO_2 may result from the large delocalized trap potential (Fig. 1) assumed by the P–F model via an effective-mass approximation. A large delocalized trap potential similar in diameter to the thickness of the HfO_2 may reduce ϕ to more than what is predicted in (1). This supposition assumes that P–F conduction is prevalent. Conversely, the differences in observed ϕ's between the 3- and 5-nm HfO_2 may be due to the presence of another carrier-transport mechanism. Regardless of the possible explanations to describe the observed differences, the P–F model does not consider a dielectric-thickness dependence and thus, is inadequate to explain the differences observed in Fig. 8.

For the 3-nm HfO_2 devices shown in Figs. 6 and 8, ϕ_r for electric fields between $\sim$700 and $\sim$900 $(\mathrm{V/cm})^{1/2}$ increases with increasing field strength. If the governing carrier-transport mechanism is P–F conduction, ϕ_r should decrease rather then increase with increasing electric field according to (1). Hence, for the 3-nm HfO_2 devices in this paper, it is evident that the P–F transport does not explain the temperature dependence of the gate-leakage-current density for electric-field strengths below $\sim$900 $(\mathrm{V/cm})^{1/2}$ or gate voltages below 1 V. Consequently, for typical MOSFET operation conditions, $(V_{\mathrm{Gate}} < \sim 1\ \mathrm{V})$, P–F transport is not dominant in 3-nm HfO_2, and a different thermally activated carrier-transport mechanism dominates. This finding agrees with similar findings in [1].

V. Conclusion

Standard P–F analysis (3) has been applied to metal-electrode high-k gate stacks composed of 3- or 5-nm HfO_2 on 1.1-nm SiO_2. Resulting trap barrier heights (ϕ's) ranged from 0.21 eV below the HfO_2 conduction band for the 3-nm HfO_2 sample to 0.45 eV for the 5-nm HfO_2 sample $(T = 320\ \mathrm{K}–400\ \mathrm{K})$.

In this paper, a much broader temperature range (6 K–400 K) than is typical (room temperature to $\sim$400 K) was examined. Evidence indicating that the data do not conform to the P–F framework was determined and is summarized as follows.

1) When implementing standard P–F analysis to extract ϕ from the data, it was found out that the extracted ϕ depends on the temperature range selected (Fig. 6). The standard P–F model predicts monoenergetic trap levels, so ϕ should not vary with temperature.
2) Thicker HfO_2 samples resulted in larger ϕ's than thin HfO_2 samples, resulting in a thickness dependence. The standard P–F model does not predict thickness dependence in the leakage current.
3) For 3-nm HfO_2 MOSFETs, P–F transport could not explain the transport-mechanism trend for gate voltages of less than 1 V. As the device voltage operating regime is in this regime, $\sim$1 V and less, the dominant leakage-current mechanism is not explained by the standard P–F analysis.

The standard P–F model as applied to the high-k dielectrics assumes that the role of defects in the SiO_2 (or high-k/SiO_2 interface) in the temperature dependence of the gate leakage current are negligible. Defects in the IL have been shown to have important implications in the stress-induced leakage current [31]. Since defects in the IL have been shown to have a significant influence in the gate leakage current at room temperature, their effects should be considered in describing the temperature dependence of the gate leakage current.

In summary, not only may the different ϕ's reported using P–F conduction in the literature be dependent on device and processing parameters but they may also depend on the temperature range tested, method of electric-field calculation, chosen electric-field range for the ϕ extraction, and HfO_2 thickness. Consequently, the standard P–F model may only be capable of explaining a narrow range of the gate leakage current in HfO_2 dielectrics. Although beyond the scope of this paper, additional studies are required to identify other possible temperature-dependent conduction mechanisms that describe the data. One potential approach is to include atomic-level properties of the involved defects in the high-k and IL that include lattice-relaxation effects [31].

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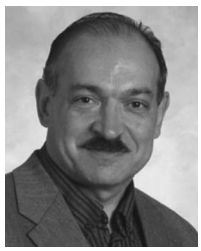

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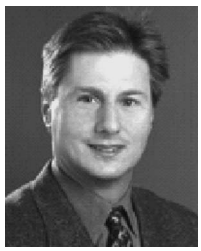

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