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Variable Integrated Analog Resistor

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(54) **VARIABLE INTEGRATED ANALOG RESISTOR**

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(58) **Field of Classification Search** 365/148, 365/159

See application file for complete search history.

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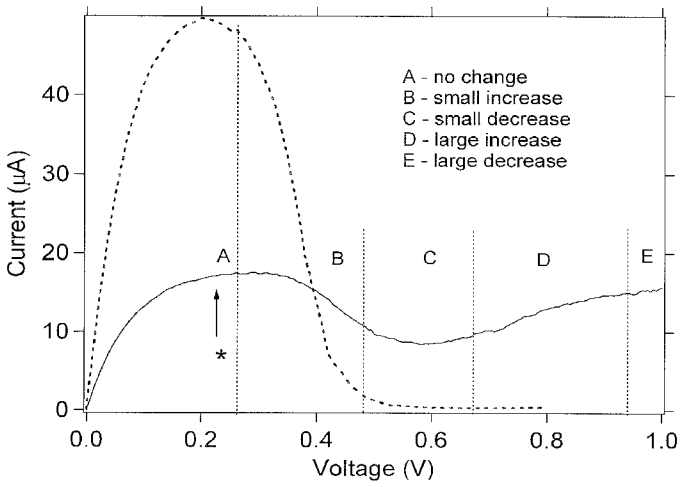
(57) **ABSTRACT**

The invention relates to the use of chalcogenide devices exhibiting negative differential resistance in integrated circuits as programmable variable resistor components. The present invention is a continuously variable integrated analog resistor made of a chalcogenide material, such as a GeSeAg alloy. Continuously variable resistor states are obtained in the material via application of an electrical pulse to it. The pulse sequence, duration and applied potential determine the value of the resistance state obtained.

20 Claims, 2 Drawing Sheets



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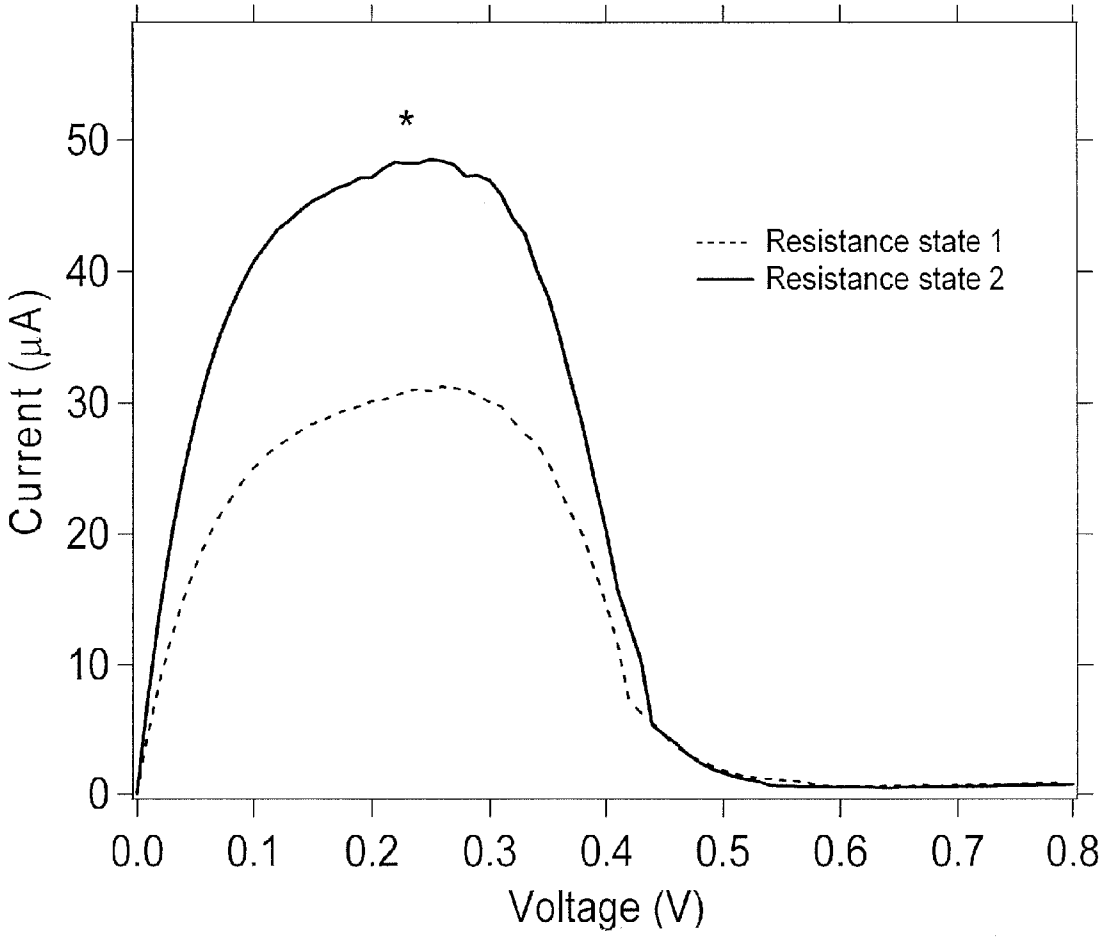
*
Resistance state 1
Resistance state 2
Current (μA)
Voltage (V)
0
10
20
30
40
50
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8

Fig. 1

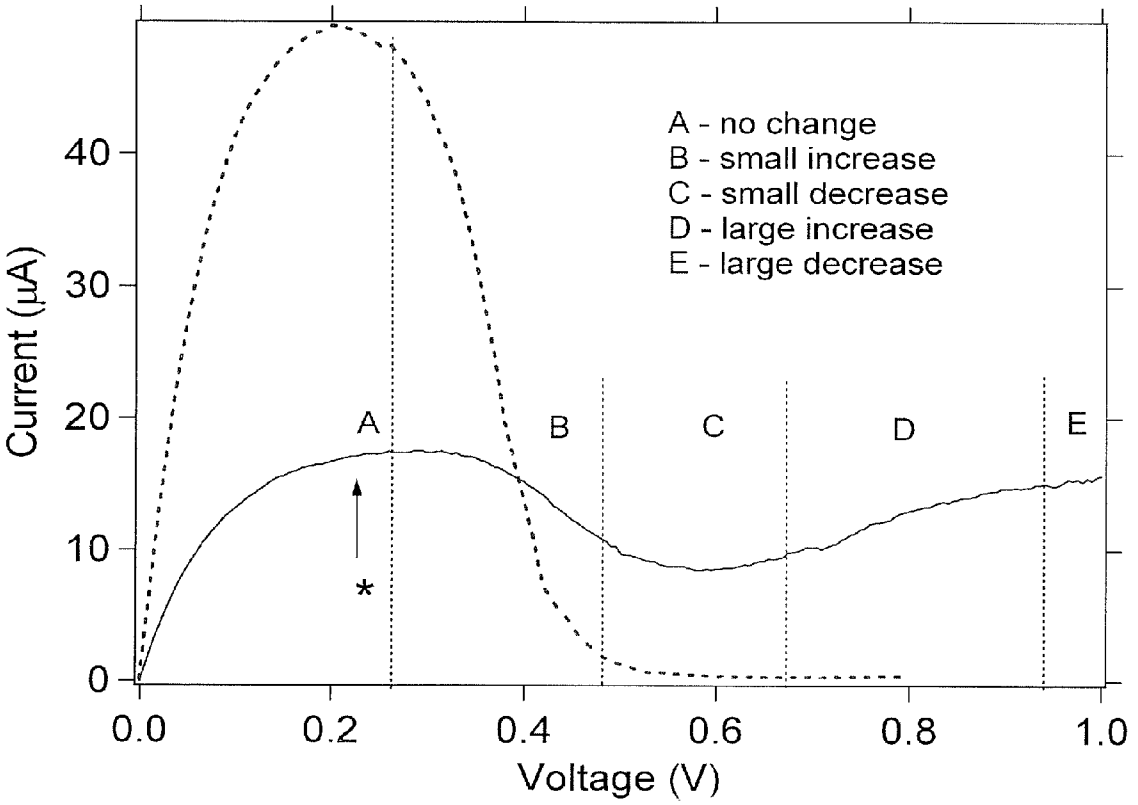
A - no change
B - small increase
C - small decrease
D - large increase
E - large decrease
A
B
C
D
E
*
Current (μA)
0
10
20
30
40
0.0
0.2
0.4
0.6
0.8
1.0
Voltage (V)

Fig. 2

VARIABLE INTEGRATED ANALOG RESISTOR

This application claims priority of Provisional Application Ser. No. 61/137,641, filed Aug. 1, 2008, the entire disclosure of which is incorporated herein by this reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to integrated circuits, and more specifically to an integrated, on-chip resistor with a range of available, different resistance states. Also, this invention pertains to electronically programmable analog variable resistors and circuits using devices exhibiting electrically programmable, different resistances.

2. Related Art

In the current state of the art, there are no integrated circuit resistor elements that are programmable. In an integrated circuit, resistors are typically fabricated in silicon by doping the silicon to a level that fixes the material resistance. This resistance is unchangeable and irreversible in the final integrated circuit. Another way of achieving a resistance in an integrated circuit is by biasing a transistor, such as a MOSFET, at certain conditions. This technique requires constant power and is thus not a low-power, or no-power, passive resistance. With neither technique is it possible to create a range of available resistance states during integrated circuit operation, referred to as variable resistances, which retain their state in the absence of an applied electrical signal.

The lack of available passive variable resistor components prevents certain basic circuit functions that require analog or programmable resistors at the chip level. On-chip integrated, programmable analog resistors would enable, for example, field-programmable circuitry, reconfigurable electronics, reduction in size of the associated circuit electronics, and lower power operation.

Chalcogenide glasses containing an excess of metal ions, e.g. Ag ions, have been shown to exhibit negative differential resistance (NDR). In this context, NDR is the same as differential negative resistance (DNR)—referred to in the prior art. U.S. Pat. Nos. 7,329,558, 7,050,327, and 7,015,494 describe devices displaying NDR/DNR, using these devices in binary electronic memory, and as an analog memory via the current value read at the NDR peak. In the prior art, the NDR device is formed by addition of an excess of metal ions in a chalcogenide glass by either heating a chalcogenide material layered with a metal layer or by application of a fast electrical pulse with pulse width and amplitude specific to the chalcogenide material type. The peak current is programmed by application of a pulse of duration and amplitude that can cause the peak current to be either reduced or increased. The device current is read at or near the voltage corresponding to the peak current value.

NDR devices can be fabricated with standard complementary metal-oxide semiconductor (CMOS) processes at sizes consistent with the state of the art feature sizes, thus integrating well with existing and future integrated circuit technologies. Conventional chalcogenide devices may be comprised of Ge_xSe_{1-x}, wherein $0 \leqq x \leqq 0.9$. Some chalcogenide devices contain copper and/or silver and/or mixtures thereof. For example, chalcogenide devices may comprise any combination of $(Ge_xSe_{1-x})_yCu_{1-y}$ and $(Ge_xSe_{1-x})_yAg_{1-y}$, wherein $0 \leqq x \leqq 0.9$ and wherein $0.1 \leqq y \leqq 0.9$. Also, some chalcogenide devices are of a single layer of chalcogenide material containing an excess of metal which causes the NDR response. Chalcogenide devices exhibiting NDR can be used as continuously variable resistors by programming with material specific pulse conditions, and using the resistance of the device measured between 0V (zero volts) and the potential corresponding to the NDR peak current in an integrated circuit. The pulse conditions applied to the chalcogenide device determine the resistance value obtained. The typical range of resistance values is semi-continuous, and thus analog, within the MOhm range to the Ohm range.

U.S. Pat. No. 7,015,494 (Campbell '494) discloses an integrated device, for example, a tunnel diode, displaying differential negative resistance (DNR)—an operating region in which Ohm's classic relation between current and voltage (I=V/R) does not apply. The '494 device is a layered semiconductor construction on a substrate, the layers being:

1. Ge and one or more of S, Te and Se;
2. a transition metal and one of more of O, S, Te and Se; and,
3. Ge and one or more of S, Te and Se.

The disclosure of the '494 patent, invented by the subject inventor, is incorporated herein by reference.

U.S. Pat. No. 7,050,327 (Campbell '327) discloses a DNR memory device that can be programmed to store information as readable current amplitudes. The memory device is made of the material disclosed in the '494 patent, and the stored data is semi-volatile. The disclosure of the '327 patent, invented by the subject inventor, is also incorporated herein by reference.

SUMMARY OF THE INVENTION

The invention relates to the use of chalcogenide devices exhibiting NDR in integrated circuits as programmable variable resistor components. The present invention is a variable integrated resistor made of a chalcogenide material, such as a GeSeAg alloy. Variable resistor states are obtained in the material via application of an electrical pulse to it. The pulse sequence, duration and applied potential determine the value of the resistance state obtained.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a graph of current vs. voltage for 2 different resistance states for one embodiment of the invention. For FIG. **1**, a GeSeAg device is programmed into two different resistance states, as measured at the peak current voltage of approximately 0.25 V (denoted by the asterisk in FIG. **1**).

FIG. **2** is a graph of current vs. voltage for 2 different devices programmed according to different embodiments of the invention. For FIG. **2**, the potential regions A-E that are used to program the device resistance to higher or lower values are shown. I-V curves for the two devices in different resistance states (as measured at 0.25 V, denoted by asterisk) are shown in the dashed and solid traces.

DETAILED DESCRIPTION OF THE INVENTION

Referring to the figures, there are shown several, but not the only, embodiments of the invented device.

Two-terminal electronic devices fabricated with chalcogenide materials alloyed with metals such as Sn, Ag, and Cu, can be forced, via application of an electrical pulse, to operate in a mode whereby they exhibit a negative differential resistance (NDR) I-V response. This has previously been explored for application in non-volatile memory in U.S. Pat. No. 7,050,327, discussed above. FIG. **1** shows an NDR I-V curve measured from a device consisting of a conventional $Ge_xSe_ySn_z$ Ag alloy. This device, with a diameter of 0.13 um, has been

forced into an NDR mode by application of a short electrical pulse (<10 ns) with an amplitude less than 1 V. This device that has been forced into NDR can operate as a continuously variable resistor when the resistance value is measured at approximately 0.25 V, the potential at which the peak current is measured (denoted by the * in FIG. **1**).

The resistance of an NDR device can be programmed by the application of a sequence of short electrical pulses. The amplitude of the pulses and the number of pulses will determine the programmed resistance state. FIG. **1** shows the IV response of a device programmed into two different resistance states. Resistance state **2** (FIG. **1**, solid curve) was achieved by pulsing the device in Resistance state **1** (FIG. **1** dotted curve) with 5 additional 400 mV, 8 ns pulses. Further pulsing can cause the device to achieve resistances as low as 500 Ohms and as high as 10's of MOhms. The devices can be switched from lower to higher resistances by varying the amplitude of the pulse applied.

The influence of the pulse amplitude on the increase or decrease of the resistance is illustrated in FIG. **2**. When a pulse with a potential value corresponding to a value in region A in FIG. **2** is applied to the conventional NDR device, the current measured at 0.25 V does not change. Thus, application of a pulse with a potential in region A can be used to 'read' the resistance without disturbing it. When a pulse with a potential in region B is applied to the NDR device, the current measured at 0.25 V increases by a small amount (<20%). However, when a potential in region D is applied to the device, the absolute current amplitude at 0.25 V increases significantly (>80%), corresponding to a significant decrease in resistance. Potentials applied to the bit with amplitudes in region C and E cause the peak current to decrease by a small amount (<20%) and a significant amount (>80%), respectively. Thus to cause a low resistance device to switch to a very high resistance device, a pulse with a potential greater than 1 V must be applied. Additionally, multiple pulses applied in each potential region have a cumulative effect on the peak current at 0.25 V. In other words, 10 pulses applied in potential region B may increase the peak current amplitude at 0.25 V by as much as one pulse applied in region D.

Although this invention will be described in terms of certain preferred embodiments, other embodiments will be apparent to those of ordinary skill in the art, including embodiments that do not provide all of the benefits and features set forth herein, and are also within the scope of this invention. It is to be understood that other embodiments may be utilized, and that many circuits that utilize the concept of this programmable resistor can be designed and fabricated, including those that optimize the programming of and the use of the programmable resistor, without departing from the spirit and scope of the present invention.

Although this invention has been described above with reference to particular means, materials and embodiments, it is to be understood that the invention is not limited to these disclosed particulars, but extends instead to all equivalents within the broad scope of the following claims.

The invention claimed is:

1. A method of inducing a programmable resistance in a chalcogenide device exhibiting negative differential resistance wherein the chalcogenide device is an analog variable resistor, the method comprising:

configuring the analog variable resistor to change resistance states in response to electrical pulses, where the pulses fall within at least four possible voltage potential ranges corresponding to at least (1) a small decrease in resistance, (2) a small increase in resistance, (3) a large decrease in resistance, and (4) a large increase in resistance,

wherein possible voltage potential ranges (2) and (4) are related such that at least approximately five electrical pulses in possible voltage potential range (2) cause a resistance change equivalent to approximately one pulse in possible voltage potential range (4), and

further wherein possible voltage potential ranges (1) and (3) are related such that at least approximately five electrical pulses in possible voltage potential range (1) cause a resistance change equivalent to approximately one pulse in possible voltage potential range (3); and

applying an electrical pulse to the chalcogenide device, wherein the electrical pulse falls within one of the at least four possible voltage potential ranges.

2. The method of claim **1** wherein:

inducing a small decrease in resistance comprises pulsing with approximately 0.27 V to approximately 0.47 V;

inducing a small increase in resistance comprises pulsing with approximately 0.47 V to approximately 0.65 V;

inducing a large decrease in resistance comprises pulsing with approximately 0.65 V to approximately 0.92 V; and

inducing a large increase in resistance comprises pulsing with approximately 0.92 V and greater.

3. The method of claim **1** further comprising reading the programmable resistance of the chalcogenide device with an electric pulse between 0 V and the chalcogenide device's negative differential resistance peak voltage value.

4. The method of claim **3** where the electric read pulse is approximately 0.25 V.

5. An analog variable resistor comprising:

a chalcogenide material exhibiting negative differential resistance; and

wherein the analog variable resistor is configured to change resistance states in response to pulses within at least four voltage potential ranges, the at least four voltage potential ranges comprising:

a first voltage potential range, the first voltage potential range inducing a small decrease in resistance;

a second voltage potential range, the second voltage potential range inducing a small increase in resistance;

a third voltage potential range, the third voltage potential range inducing a large decrease in resistance; and

a fourth voltage potential range, the fourth voltage potential range inducing a large increase in resistance; and

wherein the second and fourth possible voltage potential ranges are related such that at least approximately five electrical pulses in the second possible voltage potential range cause a resistance change equivalent to approximately one pulse in the fourth possible voltage potential range, and

further wherein the first and third possible voltage potential ranges are related such that at least approximately five electrical pulses in the first possible voltage potential range cause a resistance change equivalent to approximately one pulse in the third possible voltage potential range.

6. The analog variable resistor of claim **5** wherein the analog variable resistor is configured to have a range of resistivity between 500 Ohms and approximately 10 MOhms.

7. The analog variable resistor of claim **5** wherein the analog variable resistor has a diameter of approximately 0.13 μm.

8. The analog variable resistor of claim **5** wherein the analog variable resistor is programmable over at least ten resistance states.

9. The analog variable resistor of claim 5 wherein the chalcogenide material comprises a $Ge_xSe_ySn_zAg$ alloy.

10. The analog variable resistor of claim 5 wherein the chalcogenide material is configured to have a range of resistive values and the range of resistive values is continuous between 500 Ohms to approximately 10 MOhms.

11. The analog variable resistor of claim 5 wherein the chalcogenide material comprises Ge_xSe_{1-x}, where $0 \leqq x \leqq 0.9$.

12. The analog variable resistor of claim 5 wherein the chalcogenide material comprises Cu.

13. The analog variable resistor of claim 5 wherein the chalcogenide material comprises Ag.

14. The analog variable resistor of claim 11 wherein the chalcogenide material comprises a combination of $(Ge_xSe_{1-x})_yCu_{1-y}$ and $(Ge_xSe_{1-x})_yAg_{1-y}$, where $0.1 \leqq y \leqq 0.9$.

15. The method of claim 1 further comprising applying at least a second electrical pulse to the chalcogenide device.

16. The method of claim 1 further comprising applying a plurality of electrical pulses to induce a programmable resistance, wherein each of the plurality of electrical pulses falls within one of the at least four possible voltage potential ranges.

17. The method of claim 16 wherein the plurality of electrical pulses comprises at least five electrical pulses of approximately 400 mV, each electrical pulse having a duration of about 8 ns.

18. The method of claim 16 wherein the plurality of electrical pulses comprise at least two electrical pulses of approximately 800 mV, each electrical pulse having a duration of about 8 ns.

19. The method of claim 16 wherein the plurality of electrical pulses comprise at least live electrical pulses of approximately 600 mV, each electrical pulse having a duration of about 8 ns.

20. A method of inducing a programmable resistance in an on-chip integrated chalcogenide device comprising two terminals and a $Ge_xSe_ySn_zAg$ alloy, the method comprising:

applying an electrical pulse to the on-chip integrated chalcogenide device and thereby forcing the on-chip integrated chalcogenide device into a negative differential state;

applying a first plurality of additional electrical pulses of a first voltage potential to the on-chip integrated chalcogenide device, wherein the first voltage potential comprises a voltage potential between approximately 0.27 V and 0.47 V, further wherein each of the first plurality of additional electrical pulses comprises a duration of approximately less than 10 ns and is configured to cause a small decrease in resistance of the on-chip integrated chalcogenide device;

applying a second plurality of additional electrical pulses of a second voltage potential to the on-chip integrated chalcogenide device, wherein the second voltage potential comprises a voltage potential between approximately 0.47 V and 0.65 V, further wherein each of the second plurality of additional electrical pulses comprises a duration of approximately less than 10 ns and is configured to cause a small increase in resistance of the on-chip integrated chalcogenide device;

applying a third plurality of additional electrical pulses of a third voltage potential to the on-chip integrated chalcogenide device, wherein the third voltage potential, comprises a voltage potential between approximately 0.65 V and 0.92 V, further wherein each of the third plurality of additional electrical pulses comprises a duration of approximately less than 10 ns and is configured to cause a large decrease in resistance of the on-chip integrated chalcogenide device;

applying a fourth plurality of additional electrical pulses of a fourth voltage potential to the on-chip integrated chalcogenide device, wherein the fourth voltage potential comprises a voltage potential between approximately 0.92 V and greater, further wherein each of the fourth plurality of additional electrical pulses comprises a duration of approximately less than 10 ns and is configured to cause a large increase in resistance of the on-chip integrated chalcogenide device;

wherein the second and fourth voltage potentials are related such that at least approximately five electrical pulses of the second voltage potential cause a resistance change equivalent to approximately one pulse of the fourth voltage potential, and

further wherein the first and third voltage potentials are related such that at least approximately five electrical pulses in the first voltage potential cause a resistance change equivalent to approximately one pulse of the third voltage potential.

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