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Design Considerations for Traveling-Wave Modulator-Based CMOS Photonic Transmitters

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Design Considerations for Traveling-Wave Modulator Based CMOS Photonic Transmitters

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***Abstract*—Systematic design and simulation methodology for hybrid optical transmitters that combine CMOS circuits in a 130 nm process, and a traveling-wave Mach-Zehnder modulator (TWMZM) in 130 nm SOI CMOS process, is presented. A compact Verilog-A model for the TWMZM is adopted for the electro-optical simulation. A bond wire model using a high-frequency solver is included for accurate package simulation. Transmitter post-layout simulation result exhibits 5.48 dB extinction ratio, 9.6 ps peak-to-peak jitter, and the best power efficiency of 5.81 pJ/bit when operating up to 12.5 Gb/s non-return-to-zero data. A pulse amplitude modulation 4-level transmitter with detailed linearity design procedure is presented which has horizontal and vertical eye opening of 49 ps and 203 μW when operating at 25 Gb/s, and the power efficiency is 5.09 pJ/bit.**

***Index Terms*—Non--return-to-zero data (NRZ), pulse amplitude modulation 4-level (PAM-4), silicon photonics, transmitter, traveling-wave Mach-Zehnder modulator (TWMZM), Verilog-A.**

I. Introduction

HIGH-speed, low-power chip-to-chip interconnects are increasingly being demanded in today's large-scale computing and switching system applications. Electrical I/Os have reached a bottleneck in efficiently raising the speed up to > 20 Gb/s per lane data communication, due to the requirement of complex circuits and systems used for compensating the channel loss and dispersion. It has been proven that optical-fiber links can operate at 10 Gb/s two decades ago, but using sophisticated fabrication processes [1], which are still not cost-effective today. Recently, silicon-based photonics integration has emerged as a promising solution to overcome these I/O design challenges, and has opened wider opportunities for circuit designers to exploit photonic devices for high-speed signal processing [2], [3]. For a given lithographic generation, the speed of the silicon photonic devices is usually higher than the achievable speed of CMOS circuits in the same process node [4]. Comparable high-speed MOSFETs are not available for the integration on the same die for the commercial silicon photonic process platform, due to which designers have to rely on advanced CMOS process to design faster circuits to electrically interface with the photonic chip. Packaging challenges involved with bonding of the silicon photonic and CMOS die are critical to the overall signal integrity performance and should be considered during the early design phase. This continuation of our previous work in [5] attempts to bridge the gap between silicon photonics and CMOS circuits by developing compact models for photonic devices, which are employed in circuit simulations to enable hybrid CMOS photonic system design.

This paper focuses on TWMZM compact modeling and CMOS circuit design with NRZ and PAM-4 modulation. The TWMZM is fabricated using an SOI photonic process and the experimental device data is used for compact modeling. Section II describes the MZM device characteristics which are modeled as a Verilog-A compact model for circuit-level simulation. Section III explains the specifications for the driver circuit derived from section II, and discusses the CMOS transmitter (TX) circuit design in detail along with simulation based verification. Section IV presents a PAM-4 TX which targets at a data rate of 25 Gb/s. Finally, section V concludes the paper.

II. TWMZM Device Model

Silicon-based MZMs typically consume relatively more power (> 1 pJ/bit), are large in size (> 1mm), and non-optimal optical loss (> 3 dB for on-state), but they are tolerant to manufacturing variations, temperature change, and laser wavelength drift [6]. The photonic devices used in this work are fabricated using IME SOI integrated photonic process [4]. The idea here is to provide photonic building blocks to realize larger integrated systems, similar to the semiconductor VLSI design, and make them amenable for interfacing with electronic circuits fabricated in standard CMOS processes. A 3 mm length MZM is used in this design. Each of the MZM arms should be modeled as a transmission line when operating at high frequencies as the propagation delay of the signal in the arm is significant and thus the MZM is called a traveling-wave MZM (TWMZM). We employ a TWMZM working under reverse-biased pn junction operation based on the free carrier dispersion mechanism and is illustrated in Fig. 1. Each of the MZM arms, as shown in the cross-section, is called a phase modulator. When the light source, typically at a wavelength of 1550 nm, is split evenly into the two arms, an electrical field forced by the reverse-biased voltage applied on each of the pn junction arms inducing a change in the carrier density, which, in turn induces a phase shift as the optical wave propagates in the MZM arm. When combining the two paths of light together, they interfere either constructively or destructively at the output, depending on the E-field applied on each of the MZM arms [5]. The optical power transfer function (T_{opt}) of the MZM can be derived as in (1).

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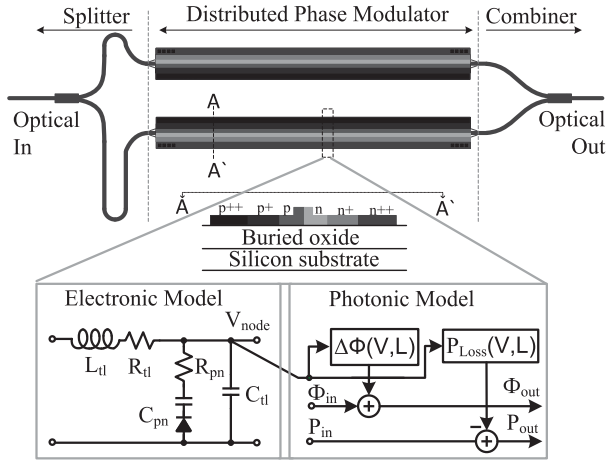

Fig. 1. Top-view of the TWMZM with the cross-section of one arm, and the compact phase modulator model.

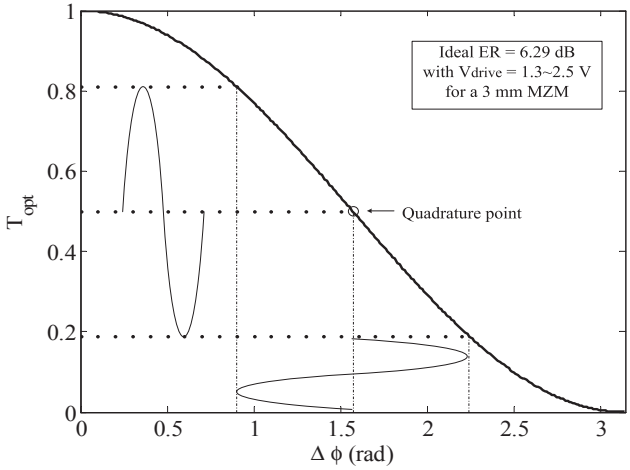

Fig. 2. Optical power transmission characteristic of the TWMZM as a function of the phase difference.

$$T_{opt} = \left|\frac{I_{out}}{I_0}\right|^2 = \frac{1 + cos\left(\phi_{dc} + \triangle\phi_{top} - \triangle\phi_{bot}\right)}{2} \quad (1)$$

Here $\Delta\phi = \phi_{dc} + \triangle\phi_{top} - \triangle\phi_{bot}$ is defined as the absolute phase difference between the two arms. T_{opt} versus $\Delta\phi$ is plotted in Fig. 2. Further, ϕ_{dc} should be set to the quadrature bias point to achieve symmetric modulation. This is achieved by an extra length (~ 100 μm) of waveguide for one of the arms before the split optical waves reach the phase modulators. A Verilog-A TWMZM model developed in our previous work [5] is used to capture the dynamic electro-optic effects between applied junction voltage and waveguide refractive index (RI) change. The model also includes the propagation delay of the light in the waveguide, RLGC network of the phase modulator and non-ideal effects of the optical loss and thermo-optical coefficient. Reader can refer to [5] for detailed formulas and parameters used in the Verilog-A model. Fig. 3 compares the measured [4] and simulated effective RI change and pn junction capacitance versus the applied voltages, showing that the two results are closely matched. The change of RI exhibits a sub-linear (square root like) dependence on the voltage. It can be observed that the modulation efficiency will be improved when it is modulated at lower voltage magnitude with a same voltage swing of 1.2 V. The simulated 20 Gb/s optical eye pattern of a 5 mm MZM is shown in Fig. 4 (a), it closely predicts the optical power levels and ER in the eye pattern shown in Fig. 4 (b) obtained from RF wafer probing in [4]. The MZM model is used for hybrid circuit-level simulations in the next section.

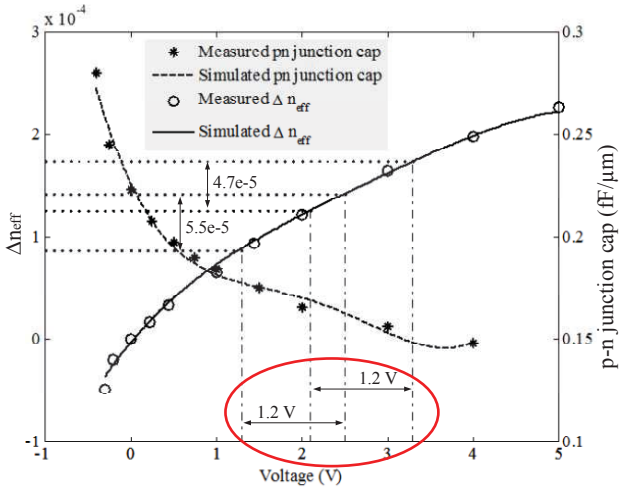

Fig. 3. The change of effective refractive index and pn junction capacitance as a function of the applied voltage.

III. NRZ MZM Driver Design

A flowchart for the CMOS photonic design methodology is shown in Fig. 5. Using a 3 mm length TWMZM model, an ideal ER of 6.29 dB can be achieved with a 1.3-2.5 V voltage drive as shown in Fig. 2. Once the drive voltage needed for the required ER is determined, driver design is then followed. A 130 nm CMOS process which features a 1.2 V core device and 2.5 V I/O device, which maximum operating voltage is 1.6 V and 2.7 V, is employed for implementing the driver circuit. Current mode logic (CML) is the best option to drive large load in high-speed applications [7]. From the previous discussion, it is required that the last stage driver has a minimum 1.2 V voltage swing on each arm of the TWMZM. For speed consideration, the differential pair (diff-pair) should use 1.2 V core devices. For reliability issue, 2.5 V I/O devices ($M3a$, $M3b$) have to be cascoded on 1.2 V devices as shown in Fig. 6, at the sacrifice of speed. Transistor sizing, bias scheme, and parasitic introduced by the pad and bond wire are all critical design considerations for high-speed circuit design, which will be detailed later.

A. CML Large-Signal Analysis

In order to efficiently use the bias current to obtain the desired voltage swing, the input pair ($M_{L1,2}$ and $M_{R1,2}$ in Fig. 6) of the CML driver are operating in the large-signal regime. Three operating regions of the input pair are illustrated along with the dc transfer characteristic as shown in the Fig.

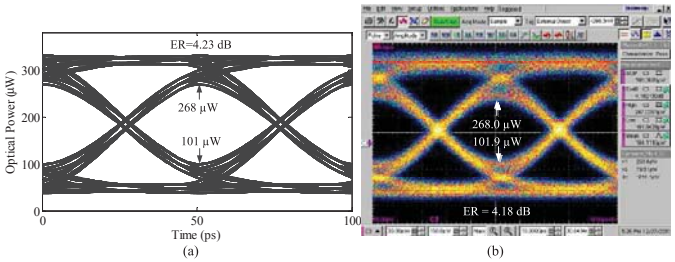

Fig. 4. Eye pattern at 20 Gb/s with 1 Vpp differential drive for a 5 mm MZM using 1555 nm wavelength. (a) Compact model simulation. (b) Measured result in [4].

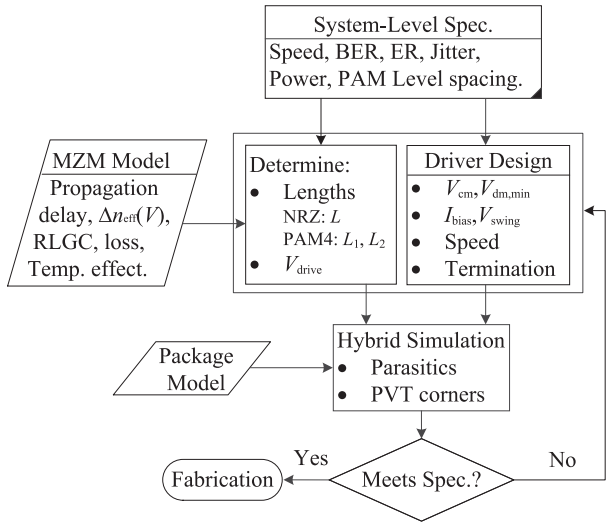

Fig. 5. Flowchart for the MZM-based transmitter design.

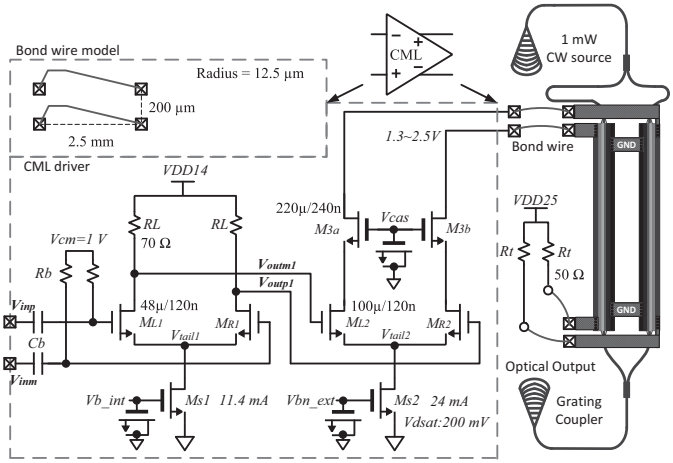

Fig. 6. Schematic of the NRZ TX circuit to drive the MZM.

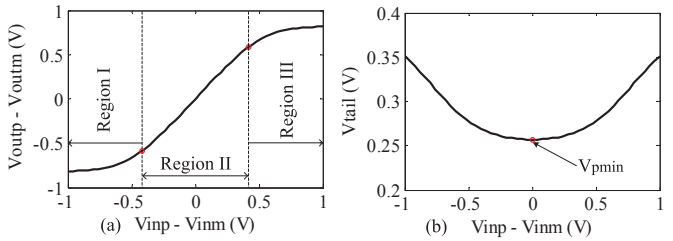

Fig. 7. (a) CML dc transfer characteristic. (b) V_{tail}-input characteristic.

7 (a). The input pair are both in saturation in region II. In region I and III, one transistor of the input pair will enter subthreshold while the other one will either stay in saturation, or in triode if its input amplitude is further increased. The rise-time of the output voltage is mainly determined by the RC time constant. This delay depends on the charging of the load capacitor by the resistors to the supply rail, and thus the total capacitance contributed by the current and the next stage should be minimized. The fall-time of the output is contributed by discharging the load capacitor during which the transistor transitions from subthreshold region to saturation region (It will enter triode region until $V_g > V_d + V_{TH}$ when the amplitude is large), with the discharge current reaching close to the tail current. Here, output slew-rate limitation is alleviated by using a large tail current. The slope in the region II can be increased by reducing the overdrive voltage of the input pair [8], this will also help to satisfy (2) to maintain the tail current source in saturation, as is illustrated in Fig. 7 (b).

$$V_{pmin} = V_{cm} - V_{gs,M_{R,L}}|_{\frac{I}{2}} > V_{dsat,Ms} \tag{2}$$

B. MZM Driver Design

Open-drain CML with single termination of 50 Ω at the far-end of the TWMZM is chosen for power saving purpose. A headroom of 250 mV is chosen to satisfy the V_{dsat} of Ms. The size of M_s is meant to be large due to the requirement of large bias current. Non-ideal current source dc characteristic with the displacement current spiking induced by the parasitic capacitance during the fast signal transition need to be taken into account. In order to efficiently utilize the tail current to achieve the desired 1.2 V voltage swing across the MZM arms, a minimum 0.4 V single-ended amplitude with a common-mode voltage of 1 V is required for the diff-pair to be switched on and off to steer the current into the resistive load. Sizing the diff-pair is a trade-off between its overdrive voltage and the maximum allowable parasitic capacitance being introduced. In order to carry the desired 24 mA current capability, it would result in a relatively large size for the input pair and the cascoded devices $M3$. This is detrimental to high-speed performance. However, the size of $M3$ can't be too small due to the ESD considerations. Thus, there is a trade-off between TX speed and ESD tolerance. Explicit capacitor is needed for the node V_{cas} to minimize the signal feed-through due to the parasitic capacitance of $C_{dg,M3}$.

Since the MZM driver consumes large current (24mA), the resulting diff-pair size is large, thus exhibiting large input capacitance. A predriver stage is therefore necessary [7] to drive the output stage with the required swing and suitably fast transitions. This requires the supply voltage of the predriver to be 1.4 V. Since the gate capacitance of M_{R2} is about 33 fF and suppose the V_{outp1} node has 15 fF parasitic capacitance, including the drain capacitance of M_{R1}, it requires the load resistance R_L to be smaller than 95 Ω to keep the rise-time

less than 0.125 UI (unit interval). Consequently, a 70 Ω load resistance with 11.4 mA tail current is chosen for the predriver. It also needs a minimum 0.4 V amplitude with a common-mode voltage of 1 V for the predriver diff-pair to be efficiently switched on and off. The size of the prominent n-channel MOSFETs and the resistor values are annotated in Fig. 6.

C. NRZ Simulation Results

For high-speed design, it's customary to use the bond pad made with top metal, which is about 32 fF and 43 fF for CMOS process and photonic process, respectively. Bond wire inductance can be favorably used to absorb a portion of the capacitance at certain frequencies and thus improve the modulator speed. S-parameter based on specific material, dimension and shape of the bond wires are modeled and extracted using Agilent's Advanced Design System (ADS) tool. The S-parameter file has been imported into the n4port cell from the Cadence analogLib library to model the bond wire effects in the Spectre simulation. The driver circuits with the MZM compact model is simulated using 12.5 Gb/s $2^{31}-1$ PRBS data, the optical eye diagram of the system is plotted in Fig. 8. The TX achieves an ER of 5.48 dB, the peak-to-peak jitter (J_{pp}) is about 9.6 ps.

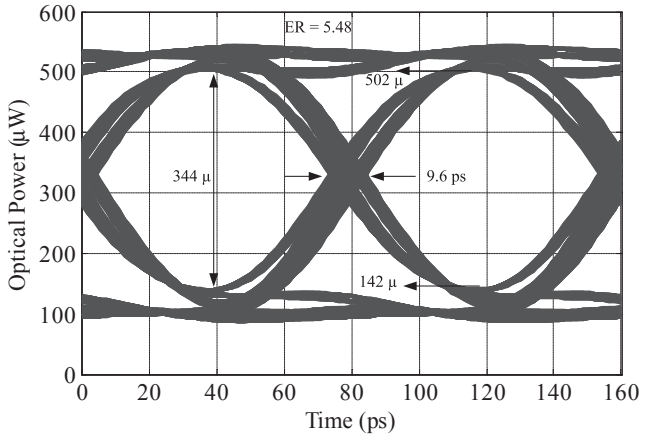

Fig. 8. Optical output eye diagram for 12.5 Gb/s $2^{31}-1$ PRBS NRZ data from post-layout simulation at nominal process corner and $80°C$.

IV. PAM-4 MZM Transmitter Design

If the data rate transmission is doubled up to 25 Gb/s, there is less than 27 ps eye opening for NRZ TX in this process due to the bandwidth-limited channel (pad, bond wire and finite MZM bandwidth). Modulation schemes such as PAM-N can provide improved spectral efficiency to achieve higher data rates. This is conceptually achieved by splitting the MZM into binary-weighted segments [10], [3]. However, a PAM-4 TX with traveling-wave pn junction modulators entails several challenges, which are addressed in this work. PAM-4 TX design flow follows the same methodology as seen in Fig. 5, except that frequency peaking should be watched for linearity and the segment lengths need to be optimized for output level spacing. The PAM-4 TX shown in Fig. 9 essentially operates as a 2-bit DAC that utilizes optical phase-domain summation. The required MZM segment ratio is not exactly 1:2 and we need to consider the fact that the phase change is not a linear function of the voltage, and also the optical transfer function is not a linear function of the phase delay. The cumulative phase shift as a function of drive voltage and segment length follows in (3).

$$\Delta\phi_{DAC} = \frac{2\pi\Delta n_{eff}(V)}{\lambda} Wl \tag{3}$$

where $\Delta n_{eff}(V)$ is 5.5×10^{-5} according to Fig. 3, λ is 1550 nm. W and l are the differential input binary weighting and segmented length in matrix form as shown in (4).

$$W = \begin{bmatrix} -1 & -1 & +1 & +1 \\ -1 & +1 & -1 & +1 \end{bmatrix}^T \; and \; l = \begin{bmatrix} L2 & L1 \end{bmatrix}^T \tag{4}$$

The desired normalized equispaced power levels $p_o = \begin{bmatrix} 0.8 & 0.6 & 0.4 & 0.2 \end{bmatrix}^T$ can be observed from Fig. 2, then p_o is substituted in the inverse optical power transfer function (T_{opt}^{-1}) of (1) for $\Delta\phi_{DAC}$. The length vector l is then determined by using $(\lambda/(2\pi\Delta n_{eff}))(W^TW)^{-1}W^TT_{opt}^{-1}(p_o)$. Optimization for the optimal length vector can be modified to include the voltage dependent optical loss for higher DAC accuracy. For this design, the optimal length of the MZM arm segments $L1$ and $L2$ are 1.1 mm and 1.9 mm, respectively.

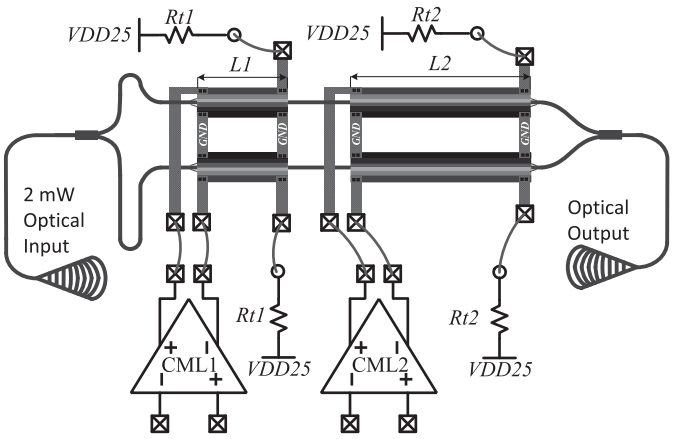

Fig. 9. Schematic of the PAM-4 TX circuit to drive the segmented MZM.

In order to obtain desired performance, PAM-4 requires an equally spaced magnitude between adjacent four optical levels even operating at very high speeds. Spectre simulation with Matlab post processing plots the electro-optical (EO) S21 phase-frequency response for the PAM-4 MZM TX, with different termination resistors is shown in Fig. 10. With 50 Ω termination, MZM segments $L1$ and $L2$ has a 3.04 dB and 0.63 dB peaking, respectively. By increasing the termination to 70 Ω and 55 Ω for $L1$ and $L2$, respectively, and scaling the current accordingly to ensure the same voltage swing, it exhibits 1.71 dB and 0.33 dB peaking. EO phase S21 bandwidth for CML1+$L1$+70 Ω and CML2+$L2$+55 Ω, including bond wire effects, is 14 GHz and 13 GHz, respectively.

Table I
COMPARISON WITH RECENTLY PUBLISHED MZM TRANSMITTERS.

Reference	Modulation	Data rate (Gb/s)	ER (dB)	Power (pJ/bit)	MZM type, length	Driver scheme
Analui [9]	NRZ	10	5.17	> 50	pn junction, 4 mm	CML in 130 nm SOI CMOS
Wu [3]	NRZ	20	-	4.5	MOS capacitor, 0.5 mm	Inverter in 40 nm CMOS
	PAM-4	20	-	0.29		
This work	NRZ	12.5	5.48	5.81	pn junction, 3 mm	CML in 130 nm CMOS
	PAM-4	25	-	5.09		

With an optical input of 2 mW, the minimum horizontal and vertical eye opening from post-layout simulation is 49 ps and 203 μW at 25 Gb/s, respectively, as shown in Fig. 11. Comparison with recently reported MZM TX designs is shown in Table I. A 130 nm SOI CMOS process was used in [9] which can integrate electric and photonic devices. The standalone MOS capacitance-based MZM device used in [3] cannot be found on an openly-available integrated platform. Further, single-ended CMOS inverter based drivers in [3] are ill-suited for driving TWMZM at GHz speed operation due to signal integrity limitations. Distributed driver based PAM-N TX has been mentioned by Luxtera but utilizes a proprietary CMOS photonic process [11].

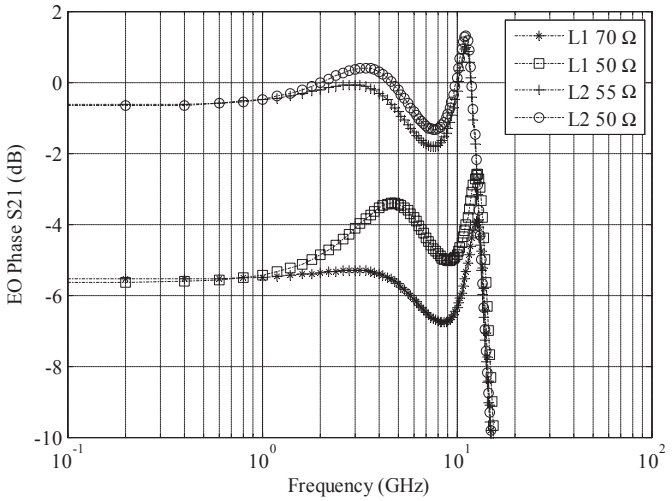

Fig. 10. EO S21 of the PAM-4 MZM TX for the two segments ($L1$ and $L2$) with different termination resistors, bond wire effect is included.

V. CONCLUSION

A systematic design methodology is presented in this brief to accurately characterize hybrid CMOS photonic transmitters comprised of a CMOS driver IC and a silicon photonic modulator, during the early design phase. NRZ and PAM-4 hybrid CMOS photonic transmitters are designed and targeted operating up to 12.5 Gb/s and 25 Gb/s data rates, respectively. The proposed design and simulation methodology is ideal for complex hybrid circuit design and system-level simulations. It can be extended to include other photonic devices as well.

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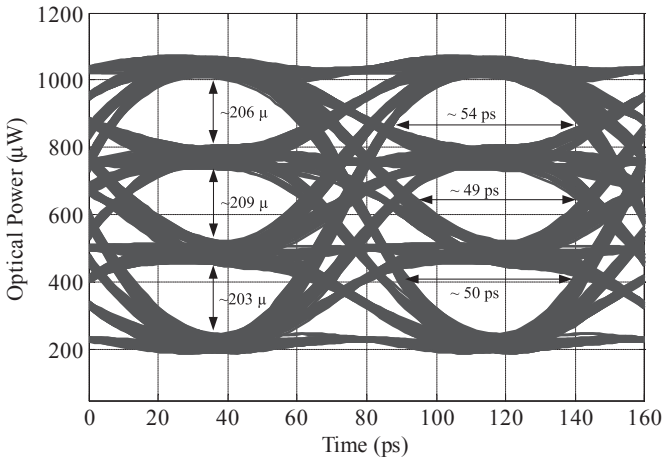

Fig. 11. Optical output eye diagram for 25 Gb/s $2^{31}-1$ PRBS PAM-4 data rate from post-layout simulation at nominal process corner and $80°C$.

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