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Design Analysis of a 12.5 GHz PLL in 130 nm SiGe BiCMOS Process

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***Abstract*—A systematic design method is applied to study and analyze the loop stability and phase noise of a type-II 3^{rd}-order charge pump PLL. The designed PLL outputs at 12.5 GHz, which is intended to provide a clock for a silicon photonic transmitter prototype. The charge pump current and loop filter resistor are made tunable to cover process and temperature variations. The PLL is designed in a 130 nm SiGe BiCMOS process. The rms jitter of the studied PLL output is about 5 ps with a 97.7 MHz reference clock with 4.9 ps rms jitter from a 0.05 to 12.5 GHz signal generator. The total power consumption of the PLL is less than 175 mW from a 2.5 V power supply.**

***Index Terms*—BiCMOS, Charge pump, Jitter, PLL, SiGe, Silicon photonics.**

I. Introduction

HIGH quality clocking is essential for any signal processing systems [1], maneuvering data in either parallel or serial. Today, higher-speed data transfer is desired due to the ever-increasing appetites for bandwidth-hungry applications, like video on-demand, online gaming, cloud computing, etc. High frequency and high precision clocking is indispensable for data generation and synchronization in any transceiver. Silicon photonic interconnects are promising candidates for replacing electrical interconnects used in data centers in the coming future due to their higher-speed and energy efficiency [2][3][4]. This PLL is designed to provide a high speed clock for the > 10 Gb/s pseudo-random binary sequence (PRBS) generator which can provide multichannel uncorrelated pseudo-random sequence for the non-return to zero (NRZ) and the 4-level pulse amplitude modulation (PAM-4) silicon photonic transmitters [4].

As semiconductor technology advances, the channel length of the devices shrink for higher speed and density. On the other hand, the gate leakage of the MOS capacitors in the loop filter is increasing, this will cause system instability with an analog PLL. Low voltage charge pump design also poses challenges in the < 100 nm technologies due to strong device mismatches and the stringent voltage headroom requirement. Digital PLLs adopting a digital loop filter, which can eliminate the use of bulky MOS capacitors and solve the leakage problem, are a hot topic and will replace analog PLLs in the < 100 nm processes [5]. However, in this 130 nm SiGe BiCMOS process, thick gate oxide MOS devices and a 2.5 V power supply are used, so that the above mentioned issues in the analog PLL design won't be a problem.

This paper presents a systematic design approach for loop filter parameters, based on the study of the PLL system's loop stability. This is instead of directly using the loop filter design tools [6] as a black box without understanding. Section II explains the linear model which is used to analyze the loop stability along with LC VCO design. Section III presents the individual noise sources in each block and their PLL output noise transfer functions. Section IV concludes the paper.

II. PLL Architecture and Stability

The proposed type-II 3^{rd}-order PLL architecture is shown in Fig. 1. Design of phase frequency detector (PFD), charge pump and dividers are not discussed in the paper. The corresponding PLL model is illustrated in Fig. 2. Individual noise sources are added in Fig. 2 for later noise analysis.

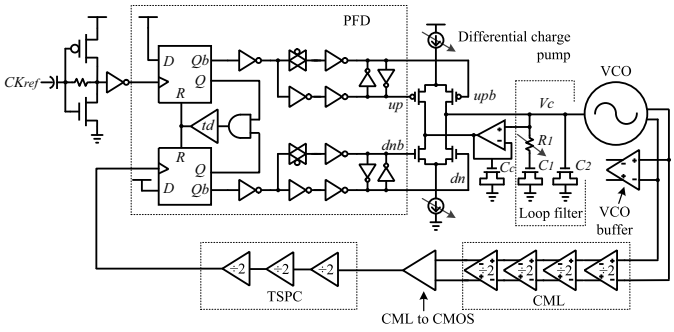

Fig. 1. Schematic of the proposed type-II 3^{rd}-order PLL architecture.

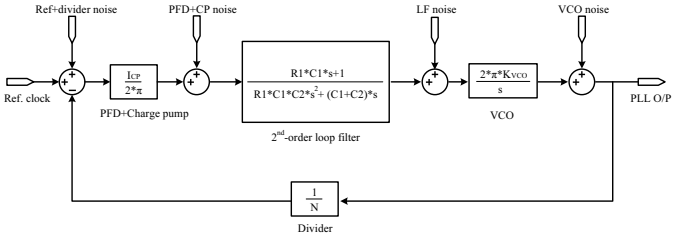

Fig. 2. PLL model with possible noise sources.

A. Loop Stability Analysis

Instead of using the traditional control analysis method of checking the natural frequency and damping ratio of a closed-loop system [7], open-loop analysis is used. According to Fig. 2, the loop transfer function of the PLL is in (1).

$$L(s) = \frac{I_{CP}}{2\pi}\left[\left(R_1+\frac{1}{sC_1}\right)\parallel\frac{1}{sC_2}\right]\frac{2\pi K_{VCO}}{s}\frac{1}{N} = \frac{I_{CP}K_{VCO}}{(C_1+C_2)N}\frac{1+\frac{s}{\omega_Z}}{s^2(1+\frac{s}{\omega_P})} \quad (1)$$

Where $\omega_Z = 1/(R_1C_1)$ and $\omega_P = (C_1+C_2)/(R_1C_1C_2)$. The unit of K_{VCO} is Hz/V. Let $b = C_1/C_2$, then $\omega_P = (1+b)\omega_Z$. In the 3^{rd}-order system, two poles are located at the origin, so that a zero should be placed before the unity loop bandwidth ($\omega_{u,loop}$), thus we have $\omega_Z < \omega_{u,loop} < \omega_P < \omega_{ref}$, where ω_{ref} is the reference clock in radians per second. By letting $c = \omega_{u,loop}/\omega_Z$ and using the trigonometric identity $tan^{-1}A - tan^{-1}B = tan^{-1}(\frac{A-B}{1+AB})$, the phase margin ($\varphi$) is shown in (2).

$$\varphi = tan^{-1}(\frac{\omega_{u,loop}}{\omega_Z}) - tan^{-1}(\frac{\omega_{u,loop}}{\omega_P}) = tan^{-1}(\frac{bc}{1+b+c^2}) \quad (2)$$

It's better to choose a phase margin of 65° when considering that the divider delay is not included in (1) which will introduce extra phase delay in the loop. Unity loop bandwidth over zero (defined as c) versus the capacitor ratio in the loop filter (defined as b) is plotted in Fig. 3 when $\varphi = 65°$. It can be observed that C_1 has to be more than 18 times larger than C_2 to achieve 65° phase margin. Typically, c is set in the range of 6 to 10 [6]. The larger the c value, the better the reference feed-through suppression will be.

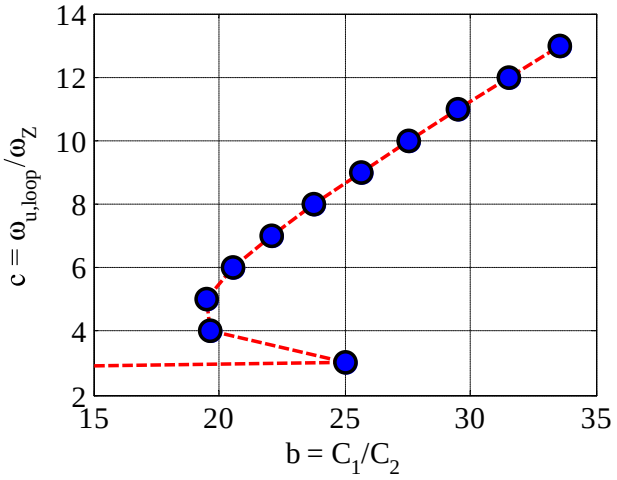

Fig. 3. Plot of unity loop bandwidth over zero versus capacitor ratio in the loop filter for $\varphi = 65°$.

Next, let's define $\omega_{ref} = a\omega_{u,loop}$. Usually a is set between 10 to 20 [7] for the following two reasons: In order to be able to approximate the VCO control voltage (V_C) as continuous time and linearize the PLL model; and to filter out periodic reference disturbance due to reference clock feed-through. However, there is a chance that C_2 will be very small (comparable to the parasitic capacitance) if the reference clock is high, and the noise performance is also sensitive to the loop bandwidth. As a rule of thumb, it's better to set $f_{u,loop}$ less than 1 MHz from a noise perspective. In this design $f_{u,loop}$=500 kHz is chosen with a 97.77 MHz reference signal, so that a=195.54.

C_2 can be solved by substituting $\omega_{u,loop}$ into the loop magnitude function as in (3). Once C_2 is known, C_1 and R_1 can be easily derived from the b coefficient and ω_Z.

$$C_2 = \frac{I_{CP}K_{VCO}}{N}\frac{a^2\sqrt{1+c^2}}{\omega_{ref}^2\sqrt{(1+b)^2+c^2}} \quad (3)$$

Thus far, I_{CP} and K_{VCO} seem to be the most important design variables to set the loop filter parameters. As long as $I_{CP}K_{VCO}$ is kept as a constant, C_2 will be fixed. Resistors and capacitors are characterized at the extreme and nominal corner conditions. It shows that the variations of the resistor, MOS capacitor and MIM capacitor can be as much as 37%, 6.3% and 34%, respectively. MIM capacitors are preferred for use in the LC VCO for its better quality factor and voltage independency. MOS capacitors are better for the loop filter. The resistor should be digitally programmable to cover the large process and temperature variations. However, before calculating the exact value of the loop filter parameters we need to know the value of K_{VCO} from the VCO design and simulation.

B. LC VCO Design

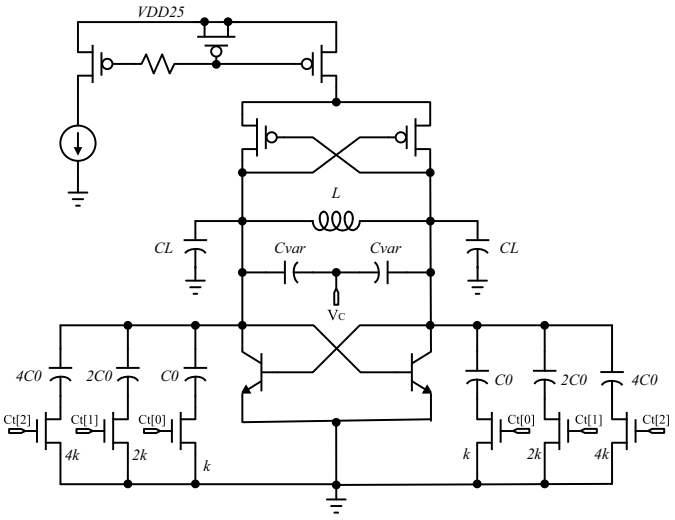

Fig. 4. Schematic of the VCO. Big R and C are added to filter out the noise introduced from the current source and bandgap reference.

The LC VCO topology is chosen for the advantages of high resonance frequency and less noise. It is also suited for the narrow tuning range application which is the case here. The schematic is shown in Fig. 4. Resonance frequency as shown in (4) depends on the inductance and total capacitance. Usually L should be kept small to leave more design freedom for C and for smaller K_{VCO} shown in (5). C_{var} should be larger than or comparable to C_L. However, all these passive devices are not ideal in practice, they have series resistance which needs to be canceled by the negative resistance introduced by the cross-coupled pairs.

$$\omega_0 = \frac{1}{\sqrt{\frac{L}{2}(C_{var} + \sum_{n=0}^{2} C_t[n]2^n C_0 + C_L)}} \quad (4)$$

MOS varactors (C_{var}) which are made by N+ polysilicon gate over n-well using 5.2 nm gate oxide, have a tuning voltage and capacitance range of -0.5 V to 1 V and 2.8:1, respectively. The area capacitance is about 6 $fF/\mu m^2$ at 1.25 V. Low K_{VCO} is desirable to reduce the VCO phase noise due to the spur.

$$K_{VCO} = (2\pi\omega_0)' = -\pi^2 f^3 L \frac{dC_{var}}{dV_C} \ (Hz/V) \quad (5)$$

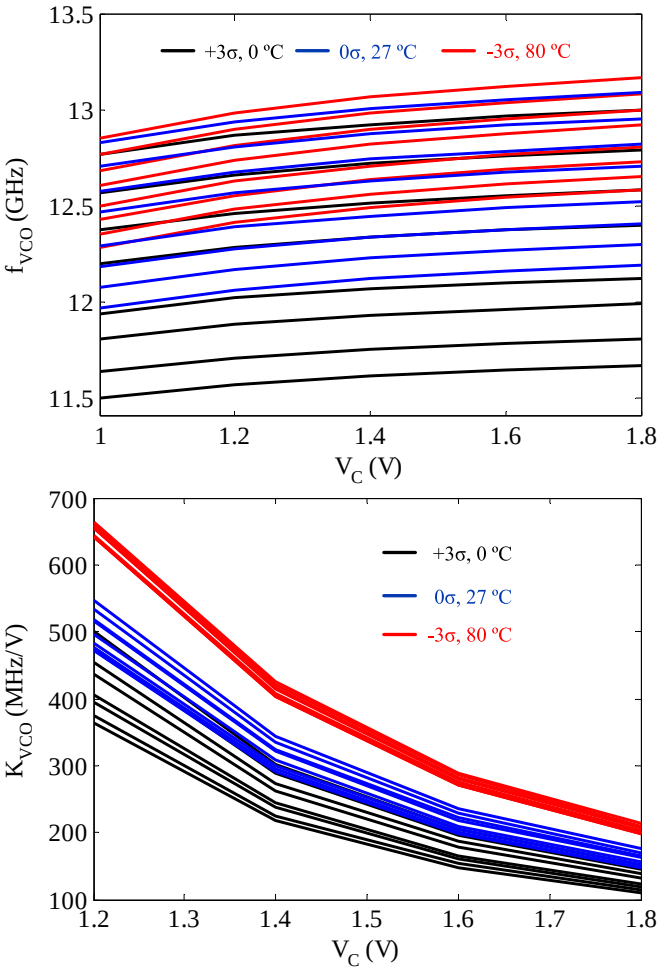

Fig. 5. Layout extracted simulation results of VCO characteristics.

The layout extracted VCO characteristics with two extreme corners and one nominal corner are plotted in Fig. 5. With the known range of the K_{VCO}, charge pump current can be designed digitally programmable to compensate the K_{VCO} variation. A PMOS current mirror with a large resistor and MOS capacitor can achieve better phase noise compared to the NMOS or npn BJT counterpart. Noise analysis will be detailed in the following section.

III. PLL Phase Noise Analysis

Every block in the PLL will add noise to the system. Other than that, the external reference clock and supply voltage also contribute significant noise. In order to find the dominant noise source of the PLL at different noise bands, noise transfer functions of the PLL output with respect to the individual noise sources are studied in a closed-loop form. Finally, the PLL output phase noise contributed by individual phase noise after being filtered by its corresponding noise transfer function is determined. Phase noise due to the device thermal noise and flicker noise in each block is estimated with periodic steady state (pss) analysis and periodic noise (pnoise) analysis in Spectre simulation, from which, the raw noise data is collected and post processed in the Matlab for analysis.

Table I
NOISE TRANSFER FUNCTIONS FROM PLL O/P TO EACH NOISE SOURCES.

$NTF\|_{n_s}^{n_{O/P}}$	Ref+Div	PFD+CP (A^{-1})	LF	VCO
PLL O/P	$\frac{NL(s)}{1+L(s)}$	$\frac{2\pi NL(s)}{I_{CP}(1+L(s))}$	$\frac{2\pi K_{VCO}}{s(1+L(s))}$	$\frac{1}{1+L(s)}$

A. Noise Sources and Noise Transfer Function

Noise transfer functions from PLL output (O/P) to each noise sources as shown in Fig. 2 are listed in Tab. I. The corresponding amplitude frequency response in dB scale is plotted in Fig. 6.

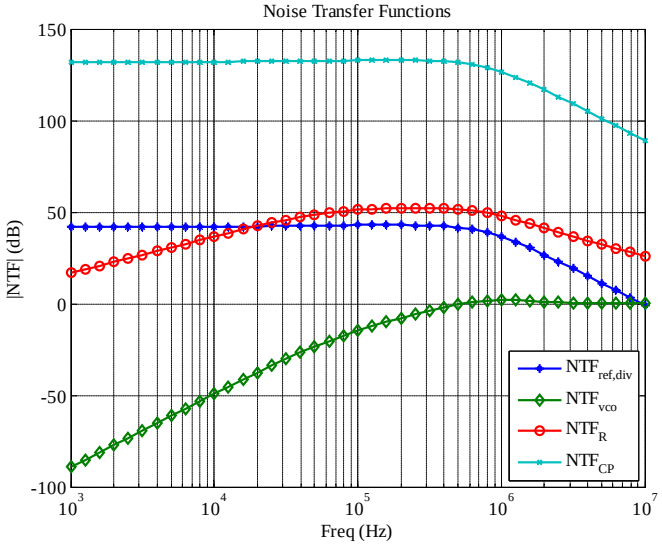

Fig. 6. Plots of PLL noise transfer function for each noise source.

The required reference clock frequency for this design is 97.77 MHz, which will be provided by an Anritsu MP1763C pulse pattern generator (PPG) as the mechanical crystal oscillator does not meet the frequency range. Since the quality of the reference clock is critical to the in-band phase noise of the PLL output, the clock maximum rms jitter is measured to be 4.8 ps as shown in Fig. 7.

B. Phase noise and rms Jitter

Reference clock phase noise is also measured with an Agilent E4411B spectrum analyzer. Phase noise for other blocks are obtained from Spectre simulation. Phase noise of each noise source is plotted on the top of Fig. 8 with an offset

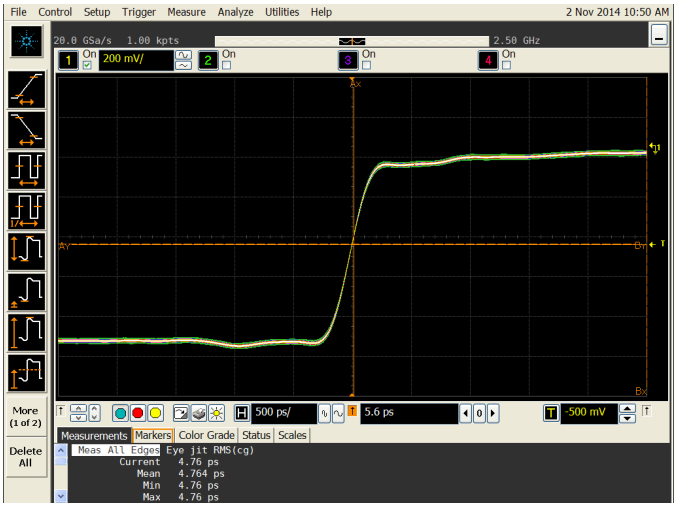

Fig. 7. Measured rms jitter of a 97.77 MHz clock generated from Anritsu PPG with Agilent DSO90254A oscilloscope (signal BW=2.5 GHz, sampling rate=20GSa/s).

frequency range from 1 kHz to 10 MHz. The PLL output total phase noise and phase noise sources introduced by each block seen at the PLL output are plotted at the bottom of Fig. 8. It can be observed that the reference phase noise seen at the output dominates the total output phase noise at lower offset frequency range, and the VCO output phase noise became dominate from 3 MHz out onwards.

(6) is used to calculate the rms jitter (variance) of the phase noise PSD in the time domain [8].

$$\sigma_{rms} = \frac{1}{2\pi f_{VCO}} \sqrt{\int_{f_{start}}^{f_{stop}} S(f) df} \qquad (6)$$

The calculated rms jitter of the reference clock and the VCO from their phase noise profile from 1 kHz to 10 MHz offset frequency range is 4.99 ps and 120.13 ps, respectively. The rms jitter of the PLL output phase noise profile is 5.01 ps. This manifests that most of the VCO noise is filtered out, but the reference clock still contributes significantly.

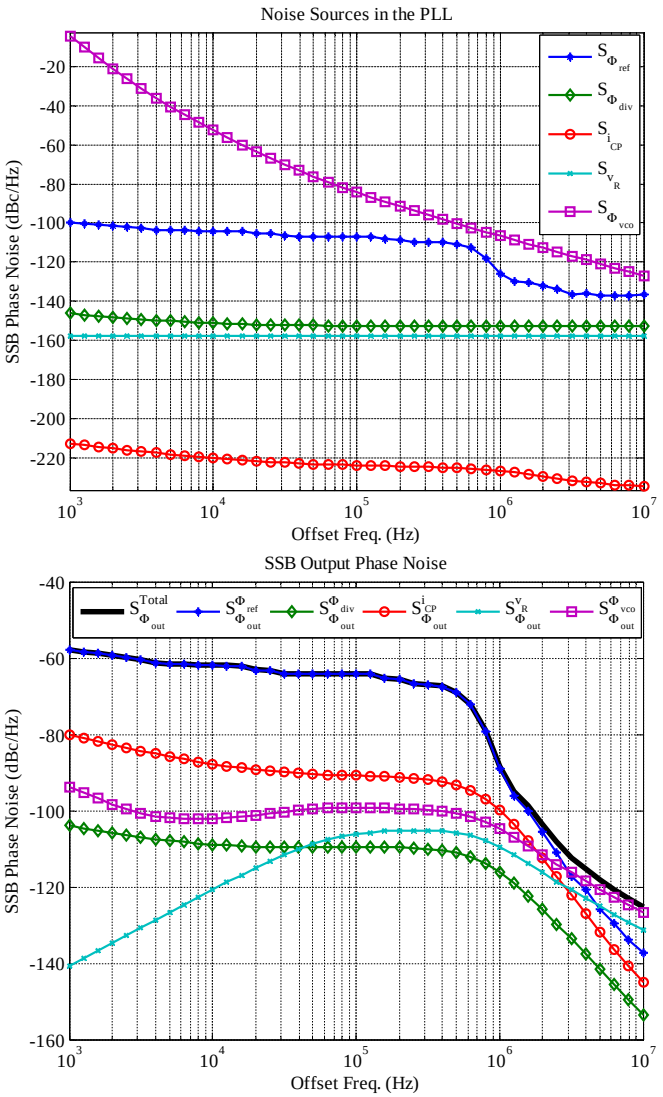

Fig. 8. Phase noise of each noise source introduced into the PLL (top) and PLL output noise due to individual noise sources (bottom). Reference clock phase noise is the measured result. Other phase noise sources are obtained from simulation.

IV. Conclusion

This paper presents a complete loop stability analysis and noise analysis method for a 12.5 GHz charge pump PLL. The design and analysis method is applicable to other PLL designs. The PLL output noise is mostly contributed by the noise introduced from external reference clock and VCO, such that a carefully chosen reference clock and the design a low phase noise VCO becomes important for overall PLL performance.

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