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Systematic Design of 10-Bit 50MS/s Pipelined ADC

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***Abstract*—A systematical design analysis of a 10-bit 50MS/s pipelined ADC is presented. With an opamp-sharing technique, the power consumption is reduced drastically. Simulated in a 130-nm CMOS process, it achieves a 58.9dB signal-to-noise ratio (SNR), a 9.3 effective number of bits (ENOB), 64dB spurious free dynamic range (SFDR) with a sinusoid input of 4.858-MHz 1-V_{pp} at 50MS/s, and consumes less than 24 mW from a 1.2-V supply.**

***Index Terms*—Pipelined ADC, SNR, ENOB, SFDR.**

I. Introduction

PIPELINE is the mainstream topology for high-speed medium-resolution ADCs[1]. ADCs without a digital calibration featuring a 10-bit resolution and a 20~200 MS/s sampling rate can be used in a variety of applications such as communications, video interfacing and image processing. The most efficient way to obtain 10-bit resolution is to use eight 1.5-bit stages and one final 2-bit flash. Each stage contributes two bits but redundancy bits should be canceled in the end to achieve an overall 10-bit resolution.

A sample-hold amplifier (SHA) is recommended to be preserved at the front-end for higher sampling clock frequency even though it's power hungry. However, a SHA-less scheme can be achieved with a trade-off of design complexity, power and performance[2]. Opamp-sharing is the best technique to save power consumption without risking performance degradation. This technique is adopted in this work. When even stages are at amplification mode while odd stages are at sampling mode, opamps in the consecutive Multiplying DACs (MDACs) can be shared[3]. The interleaving feature between odd and even stages can combine the two MDACs into one.

This paper presents a systematic design methodology for a 10-bit 50 MS/s pipelined ADC. It can be generalized for higher speed and higher resolution pipelined ADC design without digital calibration emphasized. Section II describes top-level design analysis, 1.5-bit/stage topology, opamp specifications and capacitor sizing. Section III deals with opamp and switched-capacitor (SC) comparator design. Section IV shows the simulation results. Finally, section V draws the conclusions.

II. Top-Level Analysis

As shown in Figure 1, after the front-end SHA, Stage 1 through Stage 8 adopt 1.5-bit/stage with opamp-sharing for consecutive odd and even stages. The final stage is a 2-bit flash ADC. Each stage has two intermediate output digital bits. The delay array is synchronized by a half clock cycle that is inserted before the redundancy cancellation due to different latencies in each stage, introduced by the pipeline topology. Redundancy bits are then removed by straightforward summation. The 10-bit digital outputs are synchronized in the end.

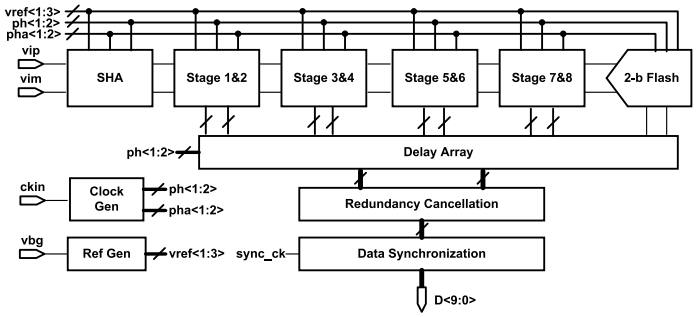

Figure 1. Simplified top-level block diagram of a 10-bit pipelined ADC.

The most stringent design requirement for pipelined ADC is imposed on its first two stages due to the fact that they are the most significant noise contributors in the pipeline chain. The digital bit resolved from the first stage sets the MSB which is critical to SNR performance. High resolution and low noise pose challenges in the opamp design. Problems like gain, speed, noise, as well as power consumption, become more difficult to trade-off. Bootstrapped switches should be used at the front-end for low distortion input sampling. A non-overlapped clock generator with advanced falling edge clocks are needed for SC circuit operation and bottom-plate sampling. A precision clock source with a duty cycle close to 50% for the clock generator circuit is necessary to alleviate the opamp specifications. The opamp current consumption and the capacitors of each stage should be scaled according to the power optimization and noise budget. The timing sequence of subADC and MDAC operations, which sets the function of the whole system, must be clear in the first place.

The performance of the ADC will be limited by noise, offset and mismatch, finite opamp gain and bandwidth, as well as non-linearity. Gain error can cause non-linearity in the transfer characteristic which deteriorates DNL (differential non-linearity) and INL (integral non-linearity), even missing codes. The 1.5-bit/stage topology can tolerate some non-idealities such as the offset introduced by the comparator. A mismatch of critical transistors, resistors and capacitors can be minimized by careful layout with the common-centroid

technique and dummies. Static and dynamic non-idealities will be reflected in DNL/INL and SINAD (signal to noise and distortion)/SFDR, respectively. Finally, opamp slewing should be monitored to assure less distortion and good linearity.

A. 1.5-bit/stage Topology

The amount of resolution per stage will directly set the gain and bandwidth requirements for the MDAC opamp. To ease opamp design, lower resolution per stage is preferred[3]. The residue voltage after amplification maybe out of range for the next stage input due to the comparator offset if a 2-bit/stage is used. A 1.5-bit/stage could tolerate a comparator offset from $-V_{ref}/4$ to $+V_{ref}/4$ (from $-125mV$ to $+125mV$ for differential signal with$1V$ peak-to-peak amplitude) and ensure the input signal for the next stage is always within the range.

A block diagram of an opamp-shared scheme for odd and even stages is shown in Figure 2. The 1.5-bit/stage needs two comparators for each subADC. The decoder and encoder are embedded in the subADC blocks which translate the thermo-code (outputs of the comparators) into binary-code (digital outputs of the subADCs) and encode a 3-bit one-shot selection signal to control one of the three reference voltages for the MDAC, respectively. MDAC has two sets of SCs (SC 1 and SC 2 for odd stage and even stage, respectively) and one opamp. The opamp will be at amplification mode in both phases.

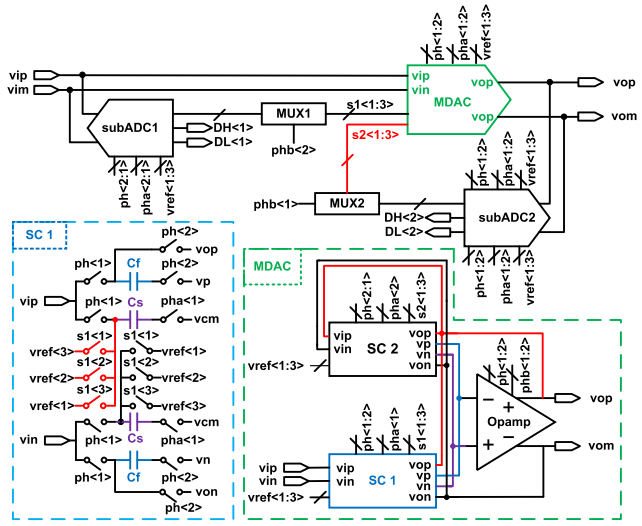

Figure 2. Block diagram of opamp-shared two-stage.

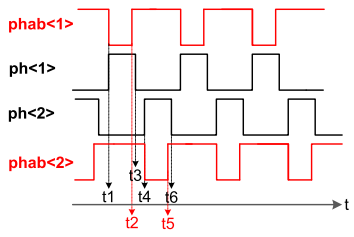

Figure 3. Non-overlapped clocks for stage operation.

The timing analysis of the non-overlapped clocks illustrated in Figure 3 is described below. The clock phab denotes the inverted clock of pha which is the advanced falling edge clock comparing to clock ph.

- t_1: SC 1 in MDAC tracks input; SC 2 in MDAC is configured at opamp amplification mode for even stage; subADC 1 tracks input and subtracts reference voltage being sampled at the previous phase ph<2> ; Latch in subADC 1 at reset mode; subADC 2 samples reference voltage; Latch in subADC 2 must finish regeneration.
- t_2: Latch in subADC 1 starts to regenerate before ph<1> falling to minimize effects of clock feed-through and charge injection caused by ph<1>.
- t_3: SC 1 in MDAC samples input and waits for opamp being configured at a multiplying-by-2 mode for the odd stage until t_4; subADC 1 samples the input and substracts reference voltage.
- t_4: SC 2 in MDAC tracks output of the odd stage; Opamp configured at the amplification mode with SC 1 for the odd stage; subADC 2 tracks output of the odd stage and subtracts reference voltage being sampled at previous ph<1> phase; Latch in subADC 2 at reset mode. subADC 2 samples reference voltage; Latch in subADC 1 must finish regeneration.
- t_5: Latch in subADC 1 starts to regenerate.
- t_6: SC 2 in MDAC samples output of the odd stage and ready for opamp multiplying-by-2 configuration; subADC 2 samples the output of the odd stage and substracts reference voltage.

B. Opamp Specifications

The minimum gain (A_v) and unity bandwidth (f_u) requirement of the opamps can be derived from the relative static gain error (ε_s) and dynamic settling error (ε_d), respectively.

$$A_v \geq \frac{1}{\beta \cdot \varepsilon_s} \; and \; f_u \geq \frac{f_s \cdot ln(1/\varepsilon_d)}{2\pi\beta\alpha \cdot D_{fs}} \tag{1}$$

β is the feedback factor in the application. f_s is the frequency of the sampling clock. α is a constant, less than 1, depending on how fast the opamp needs to be settled. D_{fs} is the duty cycle of the sampling clock.

The slew rate (SR) is another critical specification for the opamp which may experience a large steep step signal. The tail current (I_{ss}) of the opamp's input diff-pair is then steered to one side and the bias currents of the cascode branches charge and discharge the effective load capacitance (C_{Leff}) seen at the outputs[4].

$$SR = \frac{I_{ss}/2}{C_{Leff}} \geq 500V/\mu s \tag{2}$$

For noise budget analysis, the input-referred thermal noise of the system is equal to the quantization noise defined in Equation (3). The quantization noise is $(280\mu V_{rms})^2$ when differential peak-to-peak signal amplitude is 1V.

$$N_{quant} = \frac{LSB^2}{12} = \frac{(V_{pp}/2^{10})^2}{12} \tag{3}$$

A reasonable first cut partitioning of the noise is to let SHA and Stage 1 contribute a half and a quarter of the input-referred thermal noise, respectively. The quarter remaining is distributed to all remaining stages[5]. The maximum rms output noise voltage, together with minimum gain and bandwidth calculated with 40% duty cycle for each opamp are listed in Table I. β for SHA is larger for a flip-around topology is chosen.

Table I
OPAMP SPECIFICATIONS FOR SHA AND MDACS WITH A 40% DUTY CYCLE SAMPLING CLOCK.

Opamp specifications	SHA	Stage 1&2	Stage 3&4	Stage 5~8
$\varepsilon_s = \varepsilon_d$	$0.25/2^{10}$	$0.25/2^{10}$	$0.25/2^{8}$	$0.25/2^{6}$
β	0.8	0.4	0.4	0.4
$A_v\ (dB)$	74	80	68	56
$f_u\ (MHz)$	184	368	306	245
$V_{out,rms}^{noise}\ (\mu V)$	198	280	501	501

C. Capacitor Sizing

Capacitor sizing is directly driven by the noise specifications with Equation (4) and Equation (5) derived by noise partitioning mentioned previously, capacitors for each stage in the MDAC are estimated in Table II. Capacitors of $200fF$ and $600fF$ are used for all subADC's SCs.

$$\overline{V_{od,SHA}^2} = 18 \cdot \frac{kT}{C_{s,1} - (1-\beta)\cdot C_{s0}} + 2 \cdot \frac{kT}{C_{s0}} \quad (4)$$

$$\overline{V_{od,stage_i}^2} = \frac{4}{\beta} \cdot \frac{kT}{C_{s,i+1} + 0.5 \cdot (1-\beta)\cdot C_{s,i}} \quad (5)$$

Table II
CAPACITOR SIZING FOR EACH STAGE.

Capacitor in each stage	Capacitance
C_{s0}in SHA	$1.5pF$
$C_{s,1} = C_{f,1}$ in stage 1	$750fF$
$C_{s,2} = C_{f,2}$ in stage 2	$375fF$
$C_{s,3} = C_{f,3}$ in stage 3	$250fF$
$C_{s,4} = C_{f,4}$ in stage 4	$125fF$
$C_s = C_f$ in left stages	$100fF$

III. CIRCUIT DESIGN

The main analog building blocks in a pipelined ADC consist of a non-overlapped clock generator, voltage reference generators, bootstrapped switches, SC-opamps, SC-comparators. SC networks with a regenerative latch are used for comparator design in the subADC. The most challenging sub-block circuit design is fully differential opamp for SHA and MDAC.

A. Opamp Design

A folded cascode gain-boosted opamp topology, as shown in Figure 4, is chosen for easy-to-achieve stability. To minimize flicker noise, a PMOS input diff-pair is used, and its overdrive voltage should be optimized to about 10% to 30% of the power supply for speed consideration. The bias must be tuned to have enough swing headroom. For differential amplitude of 1-V_{pp} , the sum of the V_{dsat} for the upper PMOS and lower NMOS transistors (M3~M6) should be kept within 300mV. The most significant noise contributors are displayed in red. In order to minimize the input-referred noise, we have to increase $g_{m1,2}$, reduce $g_{m3,4}$ and $g_{m5,6}$. The SC CMFB is used for high speed and good linearity. In order to obtain higher common mode gain, the CMFB feedback node is connected to a portion of the tail current source.

Gain-boosting opamps (G_1 and G_2 in Figure 4) with a compact CMFB scheme are shown in Figure 5[6]. It uses transistors (MP1 and MP2)/(MN1 and MN2) to detect common-mode voltage and sinks/sources a portion of the current from the tail current of the main opamp.

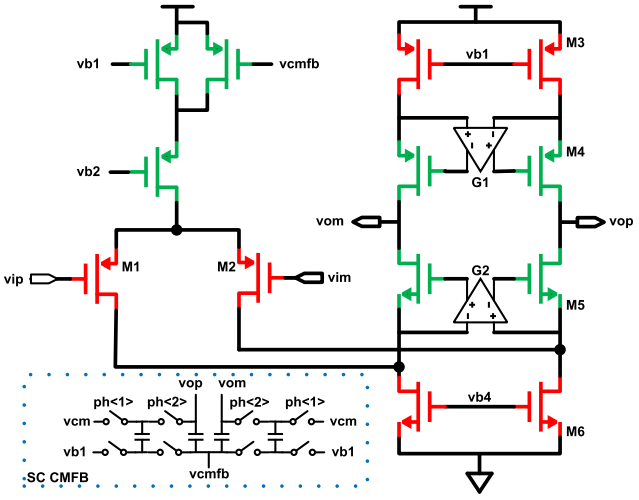

Figure 4. Folded cascode gain-boosted opamp.

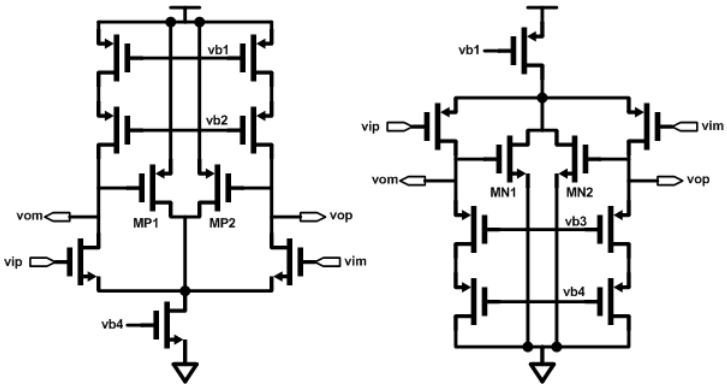

Figure 5. Schematics of upper and lower gain-boosting opamps.

B. Comparator Design

The schematic of the SC comparator consists of switched-capacitors and a cross-coupled regenerative latch (see Figure 6). With the non-overlapped clocks described previously, the switched-capacitors sample reference voltages at ph<1>. At ph<2>, the switched-capacitors subtract reference voltage from input and make comparisons at the rising edge of phab<2>. At the phase phab<2> , MP1 and MP2 reset the outputs to VDD[7]. MN0 is added to reduce static power when the latch

is at reset mode. The differential voltage (V_{dLatch}) at the inputs of the latch, ready for regeneration, is given by Equation (6).

$$V_{dLatch} = (V_{ip} - V_{im}) - \frac{C_1}{C_1 + C_2} \cdot (V_{refp} - V_{refm}) \quad (6)$$

By setting $C_2/C_1 = 3$, the threshold voltage for the comparator is set to $V_{ref}/4$. Here we define $V_{ref} = V_{refp} - V_{refm}$. Threshold voltage can be set to $-V_{ref}/4$ by swapping positions of V_{refp} and V_{refm}. By setting $C_2/C_1 = 1$, the threshold voltage for comparator can be flexibly changed to $V_{ref}/2$ for the last stage 2-bit flash ADC.

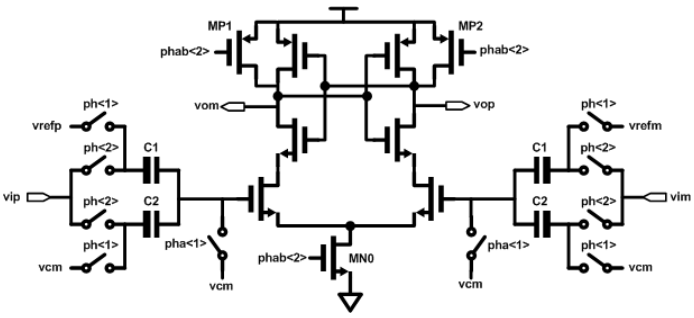

Figure 6. Schematic of the SC Comparator.

Due to offset, finite resolution and kick-back noise, preamp is often added before the latch to desensitize these non-idealities for high speed comparator design. The dynamic offset due to clock feed-through and charge injection can be compensated by reducing the regeneration time (τ) and increasing the gain (g_m). Larger regeneration gain can be obtained by increasing the sizing of the input pair and cross-coupled devices but more parasitic capacitance will be introduced. In turn, the regeneration time constant ($\tau = C/g_m$) may not be reduced. Static offset which is built in the device mismatch and threshold mismatch have not been considered yet. Overall offset can easily be up to 100mV.

We can use moderate or low gain (A_{pre}) preamp, for speed trade-off, to reduce the offset of the latch. However, the preamp itself has an offset of $V_{os,pre}$, so that the input-referred offset is:

$$V_{os,in} = V_{os.pre} + \frac{V_{os,latch}}{A_{pre}} \quad (7)$$

We can use a relatively large overdrive voltage and device sizes to reduce $V_{os,pre}$, but if it still cannot meet the specifications, we have to use input offset cancellation or auto-zeroing technique, since the preamp is like an opamp (no positive feedback)[8]. The overall input-referred offset after auto-zeroing is shown in Equation (8).

$$V_{os,in} = \frac{V_{os.pre}}{A_{pre}} + \frac{V_{os,latch}}{A_{pre}} \quad (8)$$

IV. Simulation Results

With a coherent sampling setup and a noise option enabled in transient analysis, simulated data for characterizing dynamic linearity of the ADC was obtained by analyzing a fast Fourier transform (FFT) of the output codes with a single-tone input. Post-processed with the Matlab code by using the Hanning window, the power spectrum from 2,048 samples is plotted in Figure 7. The peak SINAD reaches 57.74 dB with a 4.858-MHz input, equivalent to 9.3 effective number of bits. Under the same condition, the total harmonic distortion (THD) and the SFDR are -64.03 dB and 64.35 dB, respectively (the THD corresponds to the power sum of the first 9 harmonics).

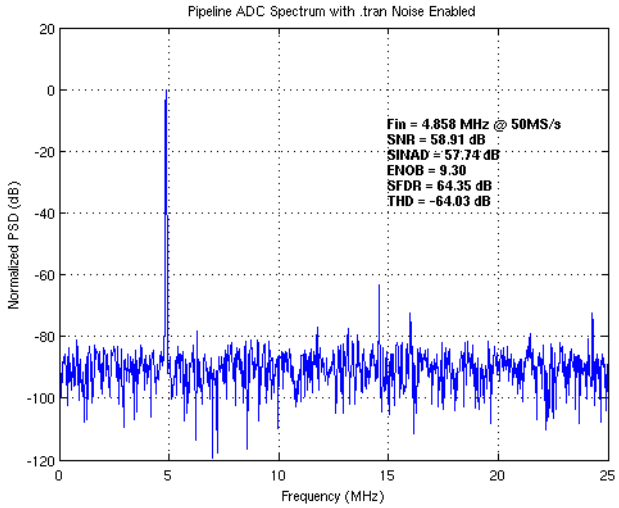

Figure 7. Simulated output spectrum with noise option enabled.

V. Conclusions

A systematic design analysis of a 10-bit $50MS/s$ pipeline ADC in a 130-nm CMOS process is presented in this paper. The methodology can be used in the design of higher speed and higher resolution pipelined ADC without digital calibration. Simulated results show that an effective resolution of 9.3-bit and 64dB SFDR are obtained when the input sinusoid frequency is at 4.858-MHz. And it consumes less than 24 mW from a 1.2-V supply.

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