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A 1 GS/s, 31 MHz BW, 76.3 dB Dynamic Range, 34 mW CT-$\triangle\Sigma$ ADC with 1.5 Cycle Quantizer Delay and Improved STF

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***Abstract*—A 1 GS/s Continuous-time Delta-Sigma modulator (CT-$\triangle\Sigma$M) with 31 MHz bandwidth, 76.3 dB dynamic range and 72.5 dB signal-to-noise is reported in a 0.13 μm CMOS technology. The design employs an excess loop delay (ELD) of more than one clock cycle for achieving higher sampling rate. The ELD is compensated using a fast-loop formed around the last integrator by using a sample-and-hold. Further, the effect of this ELD compensation scheme on the signal transfer function (STF) of a feedforward CT-$\triangle\Sigma$ architecture has been analyzed and reported. In this work, an improved STF is achieved by using a combination of feed-forward, feed-back and feed-in paths and power consumption is reduced by eliminating the adder opamp. This CT-$\triangle\Sigma$M has a conversion bandwidth of 31 MHz and consumes 34 mW from the 1.2V power supply. The relevant design trade-offs have been investigated and presented along with simulation results.**

***Index Terms*—Analog-digital (A/D) conversion, continuous-time (CT), delta-sigma ($\triangle\Sigma$), excess loop delay (ELD), feedforward, signal transfer function (STF).**

I. Introduction

In recent years, rapid development of wireless broadband communication systems has necessitated the development of power-efficient, higher signal bandwidth (BW) and higher dynamic range analog-to-digital data converter (ADCs). Continuous-time delta-sigma (CT-$\Delta\Sigma$) ADCs have recently been explored for wideband data conversion and high dynamic range (DR) due to their lower power consumption and inherent anti-alias filtering (AAF), when compared to their discrete-time counterparts [1]. Several CT-$\triangle\Sigma$ modulators targeting 10-12 bits resolution with a signal bandwidth ranging from 5-20 MHz have been reported [2], [3], [4]. The inherent AAF suppresses the out-of-band signals, e.g. blockers and interferers. This feature eliminates the necessity of an additional analog filter resulting in higher on-chip integration and lower power consumption [1].

To design a power-efficient CT-$\triangle\Sigma$ ADC, the feed-forward architecture is preferred [3], as it processes only the quantization noise and not the input signal and requires only a single feedback DAC. This results in relaxed requirements on the opamps resulting in reduced power consumption when compared to feedback architecture [3]. However, feedforward modulators exhibit out-of-band peaking in the signal transfer function (STF) magnitude response[5]. Few CT-$\triangle\Sigma$ modulators have been reported in the past with a low-pass STF, without any out of band peaking, by increasing the circuit complexity [5], [6], [7].

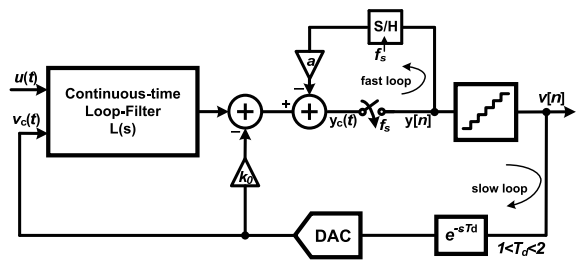

Figure 1. General block diagram of a CT-$\triangle\Sigma$ modulator with an S/H [8].

In this work, in order to achieve a higher conversion bandwidth (BW), a quantizer with an excess loop delay (ELD) of $1.5\,T_s$ is used which enables higher sampling rate (f_s) for a given oversampling ratio ($OSR = \frac{f_s}{2 \cdot BW}$). To compensate for the loop instability caused by an ELD of 1.5, a sample-and-hold (S/H) based excess-loop-delay (ELD) compensation presented in [8], is employed. Also, the impact of this ELD compensation on the increased out-of-band peaking in STF of the FF CT-$\triangle\Sigma$ modulator is analyzed. A CT-$\triangle\Sigma$ architecture has been proposed, validated with simulation results, which results in significant reduction in STF peaking making it suitable for wideband wireless applications.

The architecture and implementation details of the proposed CT-$\triangle\Sigma$ ADC form the discussion of rest of the paper. Section II briefly illustrates design of the required CT-$\triangle\Sigma$ noise transfer function (NTF), the impact of $ELD > 1$ on the STF and the system-level design procedure for the proposed ADC. Section III demonstrates circuit level implementation of the design blocks. Section IV presents the simulation results of the proposed modulator. Finally, section V draws conclusions about the work.

II. System Architecture

A. NTF Response of CT-$\triangle\Sigma$M Compensated for $ELD > 1$

Fig. 1 shows the modified CT-$\triangle\Sigma$ modulator block diagram, incorporating an ELD compensation technique of more than one clock cycle [8]. Here, the ELD compensation is achieved by using an additional feedback path around the sampler using a sample-and-hold (S/H) with a gain ***'a'***. The purpose of

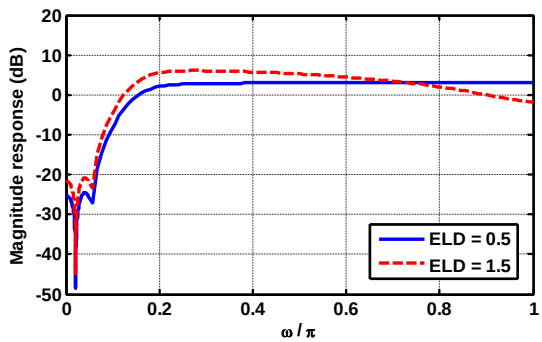

Figure 2. Comparison of $NTF(e^{j\omega})$ and $NTF_{new}(e^{j\omega})$.

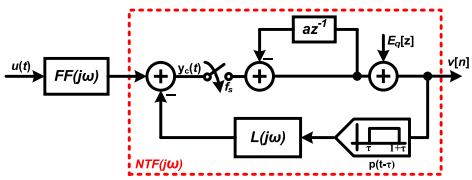

Figure 3. Linear model used in the derivation of $STF_{new}(j\omega)$.

this fast-loop is to restore the second sample of the open-loop response, $l[n]$. Due to this additional loop formed by the S/H, an extra zero appears in the resulting noise-transfer function (NTF) of the modulator. Therefore, the resulting noise-transfer function, $NTF_{new}(z)$, is of the form[8]

$$NTF_{new}(z) = (1 + az^{-1}).NTF(z) \tag{1}$$

, where $NTF(z)$ is the originally desired NTF without the S/H based short-loop. Even though the ability to tolerate ELD in the range of 1 to 1.5, increases the achievable sampling rate (f_s) by a factor of 2, there are few drawbacks with this technique. The resultant larger out-of-band gain (OBG) of the NTF_{new}, with increased in-band noise floor, results in larger 'wiggling' of the quantizer output sequence, $v[n]$. As a consequence, the signal variation at the input of the quantizer ($y_c(t)$) is increased by large extent and thus overloading the quantizer more often, which significantly reduces the maximum stable amplitude (MSA), and degrades the modulator performance. Fig. 2(a) shows the comparison of the desired $NTF(z)$ with $NTF_{new}(z)$ achieved through the design.

B. STF Response of CT-△ΣM Compensated for $ELD > 1$

Fig. 3 illustrates the equivalent linear model used to derive STF of the CT-ΔΣM compensated for ELD > 1. The resulting STF is given by the expression

$$STF_{new}(j\omega) = FF_{new}(j\omega).\frac{1}{1 + az^{-1} + k_0 z^{-1} + L_1(z)}|_{z=e^{j\omega T_s}} \tag{2}$$

where $FF_{new}(j\omega)$ is the pre-filter transfer function, and $L_1(z)$ is the open-loop response of the CT-△ΣM compensated for $ELD > 1$. The general form of $FF(j\omega)$ is given by [7]

$$FF(j\omega) = \frac{\gamma_N s^N + \gamma_{N-1} s^{N-1} + \ldots \gamma_1 s + \gamma_0}{s^N + \alpha_{N-1} s^{N-1} + \ldots \alpha_1 s + \alpha_0} \tag{3}$$

where $\gamma_N, \gamma_{N-1} \ldots \gamma_1$ are the numerator coefficients controlling the anti-alias filtering performance of the CT-ΔΣM. Fig.

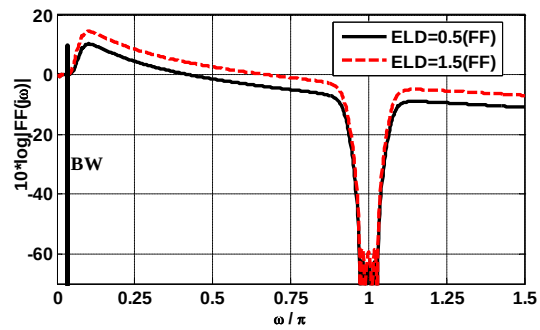

Figure 4. Comparison of $|STF(j\omega)|$ and $|STF_{new}(j\omega)|$.

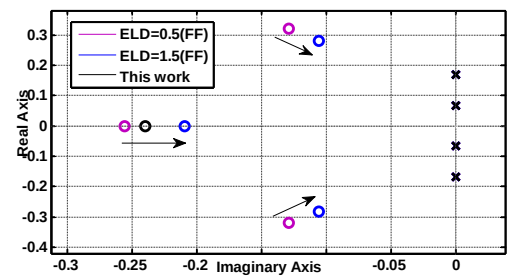

Figure 5. Pole-zero plot of $FF(j\omega)$ and $FF_{new}(j\omega)$ for CT-△ΣM compensated for ELD = 0.5 and 1.5.

4 shows the STF's of a 4^{th}order CT-△ΣM with OSR = 16, compensated for ELD = 0.5 and 1.5 respectively. The figure clearly reveals that the out-of-band peaking in the CT-△ΣM compensated for 1.5 is increased by at least $6\,dB$, (i.e) almost doubled, when compared to ELD = 0.5. As the OSR decreases (OSR < 16), there is signficant increase in STF peaking. For low-OSR designs (OSR < 16), the aggravated peaking appears closer to signal BW of the modulator. This peaking translates into degradation in the dynamic range (DR) of the modulator due to the increased signal content in $y_c(t)$ which overloads the quantizer. Also, an amplified blocker in this frequency range will significantly degrade the modulator DR.

In order to understand the increased peaking in STF, consider the pole-zero plots for $FF(j\omega)$ and $FF_{new}(j\omega)$ shown in the Fig. 5. In literature, for an nth-order loop-filter, the coefficients $K = [k_0\, k_1\, k_2 \ldots k_n]$ are typically obtained by least-square fitting the impulse response ($l[n] = [0\; l_1\; l_2\; l_3 \ldots]$) of discrete-time loop filter, $L(z) = 1 - NTF^{-1}(z)$, to the continuous-time loop-filter,$L_c(s)$, using the impulse invariance transformation (IIT) for the selected feedback DAC pulse

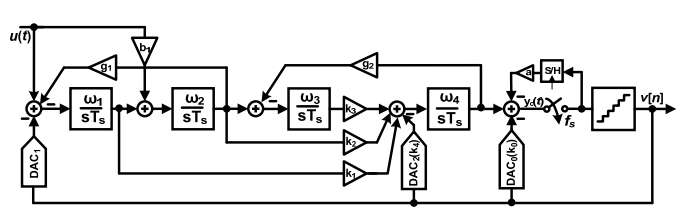

Figure 6. Porposed CT-ΔΣ modulator architecture with reduced STF peaking.

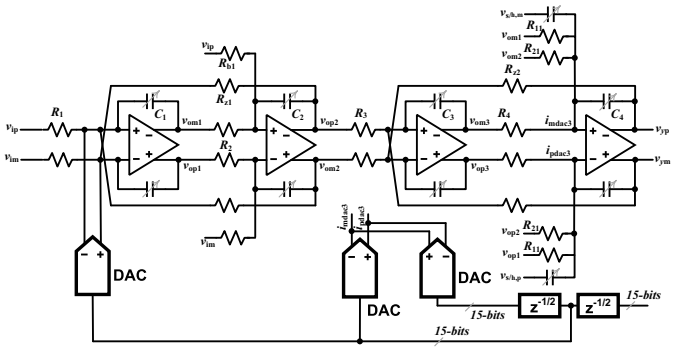

Figure 7. CT–ΔΣ modulator architecture.

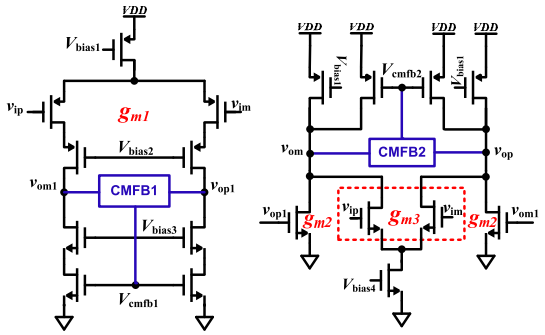

Figure 8. Two-stage feed-forward compensated opamp with CMFB circuit used in first three integrators.

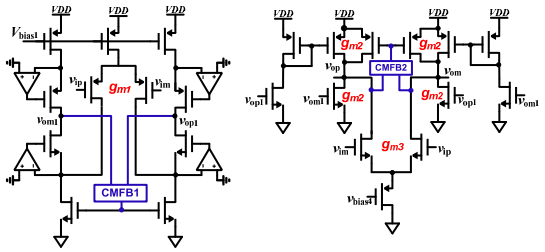

Figure 9. Two-stage feed-forward compensated opamp with CMFB circuit used in the fourth integrator (implicit adder) and the S/H.

shape [1]. Now, since the fast-loop using the S/H restores the second sample (l_1) of the open-loop response, the remaining samples ($l_{new}[n] = [0\ l_2\ l_3 \ldots]$) are restored by appropriately choosing loop-filter coefficients $K = [k_0\, k_1\, k_2 \ldots k_n]$ by least-squares fitting. Due to the increase in magnitude of samples in $l_{new}[n]$, when compared to $l[n]$, the loop-filter co-efficients K have to be large enough to fit the $l_{new}[n]$ to the continuous-time loop-filter response,$L_c(s)$. The increase in the values of K proportionally increases the magnitude of the coefficients $\gamma_N, \gamma_{N-1} \ldots \gamma_1$ of $FF(j\omega)$, which results in pushing the zeros of $FF_{new}(j\omega)$ closer to the $j\omega$- axis This results in aggravated peaking in the STF. Despite of the fact that higher BW is achieved through this ELD compensation method, the resultant peaking in the STF considerably affects the AAF performance of the CT-△ΣM (see Fig. 4).

C. CT-△Σ Modulator Architecture and Design Procedure

Fig. 6 shows the proposed CT-ΔΣM architecture with reduce STF peaking and hence improved anti-alias performance. The modulator employs a 4-bit quantizer, with a sample rate of $1\,GHz$ and an OSR of 16 to achieve a signal bandwidth of $30MHz$, suitable for next-generation wireless applications. A 4th-order NTF is chosen to compensate for the SQNR reduction due to the additional zero in $NTF_{new}(z)$ and to suppress the quantization noise sufficiently such that at least 13-bit ENOB performance is achieved. A combination of feed-forward (k_4), feedback (k_1,k_2,k_3) and feed-in (b_1) with NRZ feedback DACs (to implement k_0 path) are used in this design. Here, the quantizer delay is $1.5T_s$ to enable the higher sampling rate in the selected technology. This delay is compensated by a fast-path using the sample and hold and a slow-path using an additional feedback DAC (k_0). The NTF out-of-band gain (OBG) is set to 2 (or $6\,dB$) which corresponds to an OBG of $13\,dB$ in the resulting $NTF_{new}(z)$ (refer to Fig. 2). Fig. 7 shows the active-RC implementation of the proposed CT-ΔΣM architecture seen in Fig. 6. In order to optimize power in the design, the last integrator is used as an adder along with analog differentiation using an NRZ DAC, similar to [2], [5]. Adding a direct feed-in path from the modulator input $u(t)$ to the quantizer input $y_c(t)$, results in a degraded STF, but helps reduce the signal content at $y_c(t)$, and is thus avoided in this design. A simple opamp-based sample and hold is used in the fast-path. The design procedure is as follows: First, a desired $NTF(z)$ is selected for the target SQNR. Then, by using the *impL*1 command in the Schreier's Toolbox [1], the value of second sample '**a**' is found. Then, after removing the second sample and advancing the remaining samples (i.e. $[0\ l_2\ l_3 \ldots]$), the equivalent IIR transfer function ($L_1(z)$) is found by using the $prony$ fitting function in MATLAB. Using the resultant transfer function $NTF_1(z) = 1/(1 + L_1(z))$ is obtained. Then, *realizeNTF_ct* command uses NTF_1 and the DAC pulse shape to compute $L(s)$ and consequently the loop-filter coefficients K.

III. Circuit Implementation

A. Operational Amplifier

Figs. 8& 9 show the schematic of the feed-forward compensated opamps used in the CT-△Σ modulator. Low-V_t devices are used for the input diff-pairs in all the opamps to achieve a wider input range. The opamp topology shown in Fig. 8 is used for the first three active-RC stages, with a gradual reduction in bias currents from the first to third stage. These opamps employ a telescopic first stage with PMOS diff-pair followed by a class-A second stage. Since g_{m3} shares the bias current with g_{m2}, the topology results in lower power dissipation. To ensure that the opamp common mode output voltage is held at V_{cm}, separate common mode feedback (CMFB) loops are used in both of the op-amp stages. The total current drawn by the first opamp, including the CMFB circuitry, is $3.4\,mA$ from the $1.2\,V$ supply. The performance requirements on the opamps used for the last integrator and the sample-and-hold are high. To achieve high gain/speed opamp, a gain-boosted folded-cascade first stage is used as shown in Fig. 9. To provide sufficient current at the loop-filter output ($y_c(t)$), a class-AB second stage is employed. The total current consumed

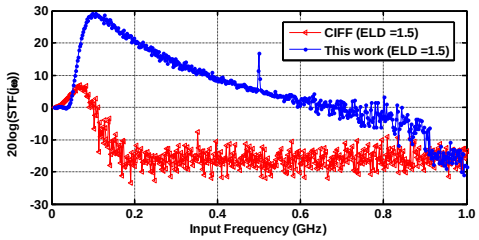

Figure 10. Simulated STF response for the conventional feedforward and the proposed modulator with ELD=1.5.

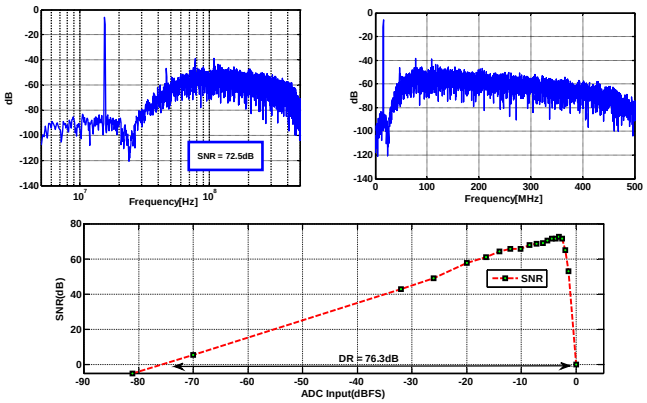

Figure 11. Simulated performance of the proposed CT-△ΣM at 1GS/s and $BW = 31\,MHz$ ($OSR = 16$).

by this opamp is $6.1\,mA$. Since feed-forward compensated opamps exhibit higher slew-rate performance [3], their usage in the loop-filter leads to significant improvement in the overall modulator linearity.

B. Quantizer and DACs

A 4-bit Flash quantizer with an input range of $1.6\,V_{pp}$ is employed in the proposed CT-△Σ modulator. A high-speed comparator similar to [2] is employed in the quantizer. The comparator uses a differential differential amplifier as the first stage followed by a latch to provide a large regenerative gain. A trimming current DAC is required for the comparators to compensate for the mismatch in the diff-pairs and the tail current sources [2]. Three current-steering DACs are employed in the modulator with bias currents of ($I_{DAC0} = 4.7\mu A$, $I_{DAC1} = 1\mu A$ and $I_{DAC2} = 10\mu A$) [1]. Standard dynamic weighted averaging (DWA) is employed in the design for DAC mismatch error shaping[1]. The DWA digital block is implemented using synthesized Verilog.

IV. Simulation Results

The 4^{th}order CT-△Σ ADC has been implemented in the $0.13\,\mu m$ IBM CMOS process. Transistor-level simulations of the CT-△Σ modulator were performed using Spectre and the results were post-processed using MATLAB. Fig. 10 shows the simulated STFs of feedforward ($ELD = 0.5$) and the proposed modulator architecture ($ELD = 1.5$). It can be observed that the STF out-of-band peaking is substantially reduced (by 24 dB). 11 shows the PSD of the modulator output

Table I
Performance Summary

	This work	[2]	[4]	[3]
Process	0.13 μm	0.13 μm	0.13 μm	0.18 μm
Supply Voltage	1.2 V	1.2 V	1.5 V	1.8 V
Sampling rate (MHz)	1000	640	900	300
BW (MHz)	31	20	20	15
Power Dissp. (mW)	34	20	87	20.7
DR(dB)	76.3	80	80	70
SNR_{max}(dB)	72.5	76	81.2	67.2
$SNDR_{max}$(dB)	72.5	74	78.1	63.2
STF peaking (dB)	9dB	-	-	-
FoM (pJ/conv.)	0.189	0.122	0.330	0.37

for a $15.5\,MHz$ input tone with $-2.5\,dBFS$ amplitude, and the simulated SNR/SNDR and DR respectively. A $8K$-point FFT with Hann window is used for spectral estimation. The peak simulated SNR of the modulator is $72.5\,dB$ and the DR is $76.3\,dB$. The modulator dissipates around $34\,mW$ power from a 1.2V supply and achieves a figure of merit ($FoM = \frac{P_d}{2^{ENOB} \cdot 2 \cdot BW}$) of $0.189\,pJ/level$.

V. Conclusion

A 1GS/s CT-△ΣM, using a quantizer with 1.5 clock cycle delay, is designed in $0.13\mu m$ CMOS technology to achieve 31 MHz conversion bandwidth. The total power consumption of the modulator is $34\,mW$. Also, the effect of 1.5 clock-cycle excess loop-delay compensation on the STF of feedforward architecture has been analyzed. A method to improve the STF performance of the modulator is presented which results in 24dB reduction in out-of-band peaking. The transistor-level simulation results of the proposed CT-△ΣM exhibit a peak SNR of $72.5dB$, a dynamic range of $76.3dB$ with a MSA of $-2.5dBFS$.

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