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Design of Wideband Continuous-Time $\triangle\Sigma$ ADCs Using Two-Step Quantizers

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***Abstract*—Continuous-time delta sigma (CT-$\triangle\Sigma$) ADCs are established as the data conversion architecture of choice for the next-generation wireless applications. Several efforts have been made to simultaneously improve the bandwidth and dynamic range of $\triangle\Sigma$ ADCs. We proposed using two-step quantizer in a single-loop CT-$\triangle\Sigma$ modulator to achieve higher conversion bandwidth. This paper presents a tutorial for employing the design technique through a 130n CMOS implementation. The proposed 640 MS/s, 4^{th}order continuous-time delta sigma modulator (CT-$\triangle\Sigma$M) incorporates a two-step 5-bit quantizer, consisting of only 13 comparators. The CT-$\triangle\Sigma$M achieves a dynamic range of 70 dB, peak SNDR of 65.3 dB with 32 MHz bandwidth (OSR = 10) while consuming only 30 mW from the 1.2 V supply. The relevant design trade offs have been discussed and presented with simulation results.**

***Index Terms*—Analog-digital (A/D) conversion, two-step flash ADC, continuous-time (CT), feedforward, sigma-delta ($\Sigma\triangle$).**

I. Introduction

CONTINUOUS-TIME delta-Sigma (CT-$\triangle\Sigma$) analog to digital converters (ADCs) are an attractive choice for next-generation wireless applications due to several desirable features like inherent anti-aliasing filtering (AAF), relaxed bandwidth requirements for the opamps resulting in lower power consumption when compared to their discrete-time counterparts. However, the rapid evolution of wireless data communication standards, in recent years, has demanded higher conversion bandwidth (BW) and dynamic range (DR) from the CT-$\triangle\Sigma$ ADCs. To achieve a wider conversion bandwidth in CT-$\triangle\Sigma$ ADCs, the designers are limited by the lower oversampling ratio (OSR) for the maximum achievable clock rate in a given technology. Furthermore, any limitation on oversampling ratio limits the highest achievable DR. In order to compensate for the SNR degradation due to lower OSR, higher resolution, i.e. multi-bit quantizers are often used [1], [2], [3]. Several CT-$\triangle\Sigma$ modulator achieving 10-12 bits resolution with a signal bandwidth ranging from 5-20 MHz have been recently reported [2], [3].

There are several advantages of using a multi-bit quantizer, which include a lower quantization noise floor and higher dynamic range, and relaxed slew-rate requirements in the loop-filer opamps. A lower LSB size allows a higher out-of-band gain (OBG) which allows aggressive noise shaping with higher maximum stable amplitude (MSA) [2], [4]. Increasing the resolution above 4-bits results in an exponential increase in circuit complexity, as increase in 1-bit in the quantizer requires a doubling of the number of comparators. Also, in a given technology, the maximum achievable sampling frequency, $f_{s,max}$ is primarily constrained by the tolerable excess loop delay (ELD) in the CT-$\triangle\Sigma$ loop. ELD is primarily contributed by the finite regeneration time of the comparator latches in the quantizer and the delay from the DAC mismatch shaping logic in the feedback DAC. We introduced the first 500MS/s, 25MHz BW CT-$\triangle\Sigma$M in $0.18\mu m$ CMOS, which employed a two-step quantizer with 5-bit resolution [5]. In this paper, we provide a tutorial review for this technique and present a higher-speed (640 MS/s) implementation in 130n CMOS. Architectural and circuit level improvements are presented for higher performance with power optimization, and an improved quantizer employing 1-bit error correction in the first stage.

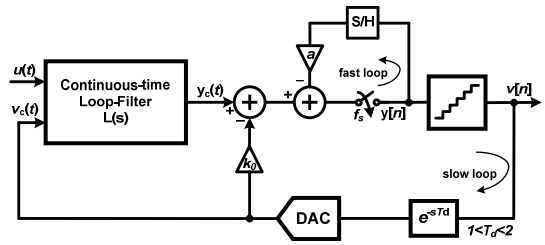

Figure 1. Block diagram of the CT- $\triangle\Sigma$ modulator with a S/H based fast-loop.

The architecture and circuit details of the proposed CT-$\triangle\Sigma$ form the discussion of rest of the paper. Section II illustrates the technique for ELD compensation greater than one clock cycle. Section III demonstrates the system level design of CT-$\triangle\Sigma$ using the two-step quantizer. Section IV discusses the circuit level implementation of the proposed CT-$\triangle\Sigma$ modulator. Section V presents the simulated performance of the proposed modulator. Finally, section VI draws conclusions about the work.

II. Systematic Design with ELD >1 Clock Cycle

Fig. 1 shows the CT-$\triangle\Sigma$M block diagram, incorporating a quantizer with conversion delay more than one clock cycle. In this figure, $L(s)$ is the continuous-time loop-filter, implemented using feed-forward architecture, whose output is sampled and quantized at frequency, f_s. Here, the ELD compensation is achieved by using an additional feedback path around the sampler using a sample-and-hold (S/H) with a gain

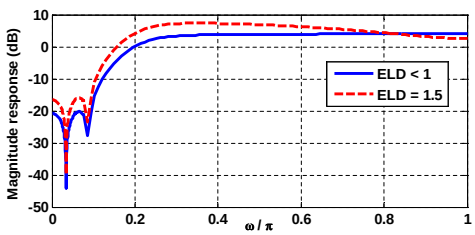

Figure 2. $|NTF_{new}(e^{j\omega})|$ showing the effect of $(1 + az^{-1})$.

a. The purpose of this fast loop is to restore the second sample (l_1) of the open-loop response, $l[n]$. A direct path with gain k_0 is introduced to restore the third sample (l_2). Due to the additional fast-loop formed by the S/H, an extra zero appears in the resulting noise-transfer function (NTF), $NTF_{new}(z)$, given by

$$NTF_{new}(z) = (1 + az^{-1}) \cdot NTF_{orig}(z) \tag{1}$$

where $NTF_{orig}(z)$ is the originally desired NTF [6]. The remaining samples of $l[n]$ are restored by appropriately choosing loop-filter coefficients $K = [k_0\, k_1\, k_2 \ldots k_n]$ by least squares fitting the following equation [5]

$$[h_0\, h_1\, h_2 \ldots h_n]\mathbf{K} = f[n] - h[n] \otimes f[n] \tag{2}$$

where $h[n]$ and $f[n]$ are the impulse response of the $NTF_{orig}(z)$ and $(1 + az^{-1})$ respectively. Further, $h_0[n] = l_0[n] \otimes h[n]$, $h_1[n] = l_1[n] \otimes h[n]$, ..., where $l_0[n]$ and $l_i[n]$ represent the sampled DAC pulse response of direct path and at the output of ith integrator.

The systematic method of obtaining the loop-filter coefficients using Eq.2 is more robust, as it considers the effect the integrator non-idealities including finite op-amp gain (A_{OL}) and the presence of additional poles and zeros. Even though, the ability to tolerate and ELD in the range of 1 to 1.5 increases the achievable sampling rate (f_s) by a factor of 2, there are few drawbacks. The larger OBG_{new} of the NTF_{new} results in increased 'wiggling' of the quantizer output sequence. As a consequence, the signal variation at the input of the quantizer ($y_c(t)$) is increased by a larger extent which significantly reduces the maximum stable amplitude (MSA) as well as the DR. Therefore, in order to design a stable modulator with $ELD > 1$, either a lower OBG should be used ($OBG \leq 2$) or a higher resolution quantizer (resolution > 4) with lower LSB size must be used to achieve a desirable MSA around $-1.9\, dBFS$. In this design, the 5-bit quantizer allows for an aggressive OBG_{orig} of 2.5 in NTF_{orig}, while achieving an MSA of $-1.938\, dBFS$.

III. System Level Design of the CT-△Σ Modulator

This section briefly discusses the architectural choices made in the presented CT-△Σ modulator.

A. Architectural Choices

For low-OSR △Σ designs, increasing the order above three, does not provide significant improvement in SQNR [2].

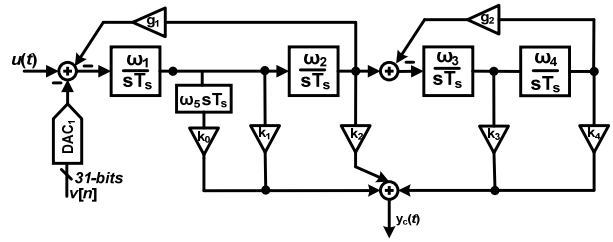

Figure 3. The 4th-order loop-filter employed in the CT-△Σ modulator without k_0 DAC[7].

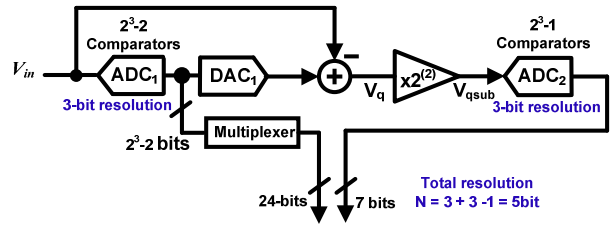

Figure 4. Block diagram representation of two-step Flash quantizer.

However, to compensate for the increase in the in-band noise floor due to the additional zero $NTF_{new}(z)$, a $4^{th}-$order loop-filter is required. Further, for robust stability and desirable MSA with a 5-bit quantizer, the OBG_{orig} is selected to be 2.5 (corresponding OBG_{new} is 6). Fig. 2 illustrates the magnitude responses of $NTF_{orig}(e^{j\omega})$ and $NTF_{new}(e^{j\omega})$ before and after the ELD compensation respectively.

B. Loop-Filter Design

A 4th-order feedforward loop-filter architecture is employed in the design. The direct path from the quantizer output (k_0) is implemented by tapping the output from the first integrator in the loop filter, and then differentiated using a capacitive input to the adder [7]. This avoids an additional feedback DAC in the topology. The loop-filter coefficients are computed by incorporating the opamp non-idealities using the systematic design procedure described in Section II. Due to the use of 5-bit quantizer, the slew rate requirements on the first integrator in the loop filter are greatly relaxed. The performance specifications for each of the opamps were obtained through behavioral simulations performed using the SIMSIDES Toolbox in Simulink [8].

C. Quantizer Design

A 5-bit, 640MS/s two-step Flash ADC is employed as the quantizer. Fig. 4 shows the block diagram representation of two-step flash quantizer used in CT-ΔΣM. V_{refn} and V_{refp} are common high and low reference voltages for the$1^{st}$and 2^{nd}stage. To accommodate a $0.5\, LSB$ error at V_q (output of the Subtractor), an offset of $0.5\, LSB$ is added to the resistor string (i.e) to V_{refn}. Similarly, to always keep V_q lesser than V_{refp}, the last reference voltage from the resistor string has been removed. Thus, the resistor string reference voltages for course stage are given by $V_{refn} + 1.5LSB$, $V_{refn} + 2.5LSB \ldots V_{refn} + 6.5LSB$. This results in $2^3 - 2 = 6$ comparators for the course-stage. The first stage is followed

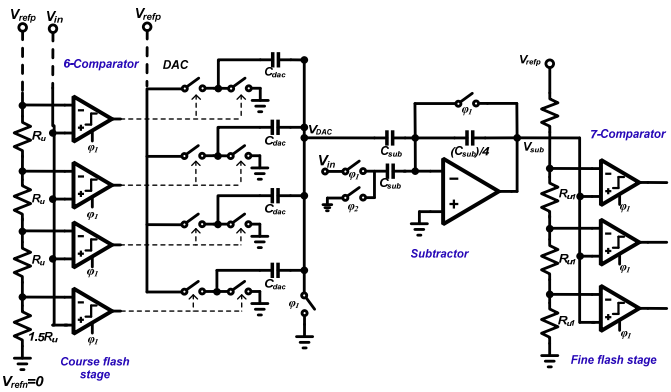

Figure 5. Simplified single-ended function diagram of ADC [9].

by a 3-bit segmented capacitor DAC. The output of a DAC is directly coupled to the switch-capacitor residue amplifier or Subtractor which subtracts and generates the amplified version of V_q by a gain of 4. The residue amplifier drives the 7 comparators in the fine-stage. Thus, the total resolution of the quantizer is $5\,bits$. The quantizer full-scale range is set to $1.6\,V_{pp}$, which results in a LSB size of 100 mV in the coarse/fine flash stage. The chosen full-scale range relaxes the offset requirement on comparator in the two-step flash ADC.

Fig. 5 shows the system-level schematic of the 5-bit two-step flash ADC. During the phase ϕ_1, the coarse flash stage estimates the two most significant bits (MSBs) of the sampled signal and provides an equivalent thermometer code output. The resultant code drives highly linear segmented capacitive DAC to decode the signal back to a 3-bit resolution analog signal. Then, during the clock phase ϕ_2, residue V_q is estimated by the residue amplifier with a gain by subtracting V_{dac} from V_{in}. Finally, the fine stage digitizes the residue V_{sub} to encode the three least significant bits of the ADC. Further, during ϕ_1 clock phase, all the capacitors in the circuit are reset or discharged to ground. The time delay assigned to the first flash stage, DAC and the Subtractor combined together is $0.8T_s$and, the time delay assigned to the second flash stage and current DAC combined is $0.7T_s$. Thus, the net delay introduced by the 5-bit quantizer including the DWA logic is $1.5T_s$.

IV. Circuit design

In this section, the circuit level blocks, used in the CT-$\triangle\Sigma$ modulator, are described. The proposed CT-$\triangle\Sigma$ modulator was implemented in a $0.13\,\mu m$ CMOS technology.

A. Operational Amplifier

Fig. 6 shows the schematic of the feed-forward compensated opamps used in the CT-$\triangle\Sigma$ modulator. Low-V_t devices are used for the input diff-pairs in all the opamps to achieve a wider input range. The opamp topology seen in Fig. 6 is used for all the four active-RC stages, with a gradual reduction in bias currents from the first to the fourth stage. These opamps employ a telescopic first stage with PMOS diff-pair followed by a class-A second stage. Since g_{m3} reuses the bias current from g_{m2}, the topology results in lower power dissipation. To

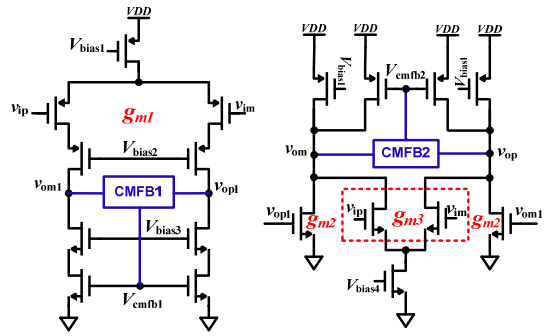

Figure 6. The Feedforward compensated opamp employed in the loop-filter.

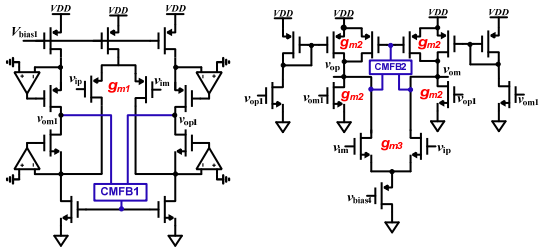

Figure 7. Two-stage feed-forward compensated opamp with CMFB circuit used in the adder.

ensure that the opamp common mode output voltage is held at V_{cm}, separate common mode feedback (CMFB) loops are used in both of the op-amp stages. The total current drawn by the four opamps, including the CMFB circuitry, are 3.1, 2.1, 1.8 and 1.8 mA respectively from the $1.2\,V$ supply. A class-AB output opamp, shown in Fig. 7, is employed to meet the higher performance requirement of the adder. The total current consumed by this opamp is $5.5\,mA$. Since feed-forward compensated opamps exhibit higher slew-rate performance, their usage in the loop-filter leads to significant improvement in the overall modulator linearity.

B. Comparator

The comparators, used in the quantizer, should be able to provide sufficient regenerative gain to mitigate the effects of metastability at 640 MHz sampling rate. Fig. 8 shows the high-speed comparator used in the modulator, similar to [3]. Here, the first stage uses a differential difference amplifier for reference subtraction. The amplifier is loaded with cross-coupled PMOS latches to provide initial regeneration followed by a clocked latch. The second stage latch provides a large regenerative gain and resolves the outputs to full logic level. The latch is disconnected from the input to avoid kickback noise. A reset phase is used to remove memory in the latches.

C. Sample-and-Hold

A simple sample-and-hold based on inverter based buffer, as shown in Fig. 9, is used to implement the fast-path around the quantizer. The transconductor is designed using a simple diff-amp.

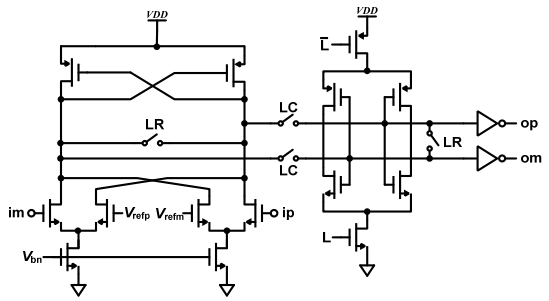

Figure 8. The high-speed comparator used in the quantizer[3].

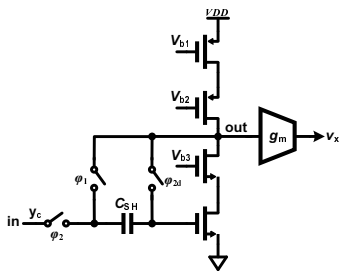

Figure 9. Single-ended schematic of the S/H circuit.

V. Simulation Results

The 4^{th}order CT-$\triangle\Sigma$ ADC, with a two-step quantizer, was implemented in the $0.13\,\mu m$ IBM CMOS process. Transistor-level simulations of the CT-$\triangle\Sigma$ modulator were performed using Spectre and the results were post-processed using MATLAB. Fig. 10 shows the PSD of the modulator output for a $32\,MHz$ input tone with $-1.938\,dBFS$ amplitude, and the simulated SNR/SNDR and DR respectively. A $8K$-point FFT with Hann window is used for spectral estimation. The peak simulated SNR of the modulator is $72.5\,dB$ and the DR is $76.3\,dB$. The modulator dissipates around $30\,mW$ power from a 1.2V supply and achieves a FoM of $0.323\,pJ/level$.

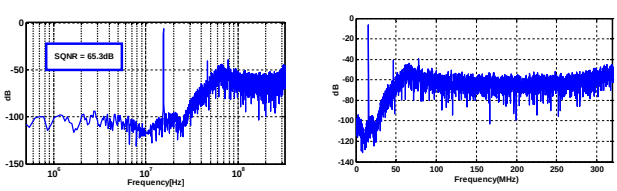

Figure 10. PSD of the modulator for a $15.3MHz$ input tone at the maximum stable amplitude.

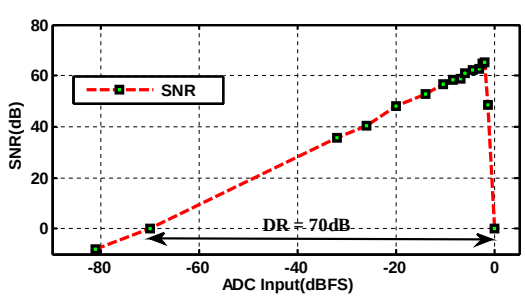

Figure 11. Simulated SNR and dynamic range.

Table I
Modulator Performance Summary

	This work	[3]	[7]	[2]
Process	0.13 μm	0.13 μm	0.18 μm	0.18 μm
Supply Voltage	1.2 V	1.2 V	1.8 V	1.8 V
Sampling rate (MHz)	640	640	800	300
BW (MHz)	32	20	32	15
OSR	10	16	12.5	10
Quantizer resolution	5-bit	4-bit	4-bit	4-bit
Power Dissp. (mW)	30	20	47.6	20.7
DR(dB)	70	80	64	70
SNR_{max}(dB)	65.3	76	57	67.2
$SNDR_{max}$(dB)	65.3	74	57	63.2
FoM (pJ/conv.)	0.323	0.122	1.29	0.37

VI. Conclusion

A wideband CT-$\triangle\Sigma$M using a two-step quantizer is proposed and designed in a $0.13\mu m$ CMOS technology. The proposed modulator achieves a high dynamic range with very wide conversion bandwidth using a 5-bit two-step quantizer. The excess loop-delay due to the two-step conversion process was successfully compensated using a fast loop around the quantizer. The CT loop-filter coefficients are systematically computed by incorporating the opamp non-idealities. The simulation results of the proposed CT-$\triangle\Sigma$M exhibit a peak SNR of $65.3\,dB$, a dynamic range of $70\,dB$ with a MSA of $-1938\,dBFS$. The successfully demonstrated concept paves the path for the development of CT-$\triangle\Sigma$ADCs incorporating multi-step and pipelined quantizers.

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