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# Multi-bit Continuous-time Delta-Sigma Modulator for Audio Application

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Abstract—The design considerations for low-power continuoustime (CT) delta-sigma ( $\Delta\Sigma$ ) modulators is studied and circuit design details for a 13.5 bit modulator are given. The converter has been designed in a 0.5 um C5FN AMI CMOS technology and achieves a maximum signal-to-noise ratio (SNR) of 85 dB in a 48 kHz bandwidth and dissipates 5.4 mW from a 5 V supply when clocked at 6.144 MHz. It features a third-order active-RC loop filter, a 4-bit flash quantizer along with a Data Weighted averaging (DWA). The loop filter architecture and its coefficients have been targeted for the minimum power dissipation. The DWA also has been implemented by standard cell based synthesis to further optimize power. The figure of merit (FoM) of the CT- $\Delta\Sigma$ modulator is 3.71 pJ/bit. The fabricated chip of the modulator occupies an area of 4.5  $mm^2$ .

Index Terms—Analog to digital converter (ADC), Digital to analog converter (DAC), delta-sigma modulation, noise-shaping.

#### I. INTRODUCTION

I N recent years, due to an increasing demand for high resolution, low band width data converter systems for digital audio and voice applications (see [1] and references therein). The delta-sigma ( $\Delta\Sigma$ ) converters [2] are well suited because of the over sampling rate (OSR), hence useful for low frequency and use noise shaping to achieve high resolution [3]. More specifically, a CT- $\Delta\Sigma$  modulator [4] [5] is preferred due to the advantages like low power consumption, inherent antialiasing, fixed resistive impedance and relaxed performance of the integrators [3].

A CT- $\Delta\Sigma$  modulator is characterized by the number of levels or number of bits of the internal quantizer. A singlebit CT- $\Delta\Sigma$  modulator is highly linear. But, as the order of the modulator gets higher i.e., the higher order noise transfer function (NTF) suffers from the signal dependent stability limitation. And, as out-of-band gain (OBG) increases the variance of noise gets higher, the quantizer overloads more often. Further, the maximum stable amplitude (MSA) falls rapidly. However a multi-bit CT- $\Delta\Sigma$  modulator enhances the stability by impressive margins for a third or higher order NTF. With a multi-bit modulator the least significant bit (LSB) size reduces, and hence lower the probability of the quantizer overload [3] and thus enhancing the stability of the system. And the quantization noise power at the output is reduced significantly and the signal-to-noise-plus-distortion ratio (SNDR) increases at the rate of 6 dB per bit of the internal quantizer used [2]. And from the system point of view a multi-bit modulator would relax the constraints on the ensuing decimation filter [6]. Figure 1 shows the block diagram of CT- $\Delta\Sigma$  modulator.

CT  $\Delta\Sigma$  Modulator



Figure 1. Block diagram of a Continuous-time Delta-Sigma ADC Modulator.

However, the dynamic range improvement of a multibit quantizer is not quite realized due to the high linearity requirement of feedback DAC [7]. The non-linearity in a multibit feedback DAC increases the noise floor in the signal output spectrum of the modulator and reduce the dynamic range. This noise added is due to the mismatch error introduced by the uneven spacing of DAC levels. Certain noise shaping techniques [8] have been used to reduce this non-linearity. These techniques make use of noise filtering mechanism in the signal band and move the noise power to out-of-band frequencies [9]. Several Element matching techniques like [10] [11] have been proposed to reduce the DAC non-linearity. But, they suffer from aliasing of DAC distortion errors in to signal band [7]. Though other techniques like Individual Level averaging (ILA) [12] and bi-DWA [13] are also available but results in increased noise floor in the signal band of the output spectrum. The dynamic element matching technique which address the problems suffered by the above techniques is DWA [7]. The modulator system has been designed by systematic design centering method [14] for obtaining the loop-filter coefficients, by including the effect of the integrator non-idealities.

This paper presents the design and implementation of a  $3^{rd}$  order CT- $\Delta\Sigma$  ADC with a 4-bit quantizer targeted for audio applications. To correct the non-linearity of the DAC in the system a 4-bit DWA has been implemented using the standard cell based layout to optimize power. To achieve low power implementation loop filter architecture having minimum power consumption has been chosen.

The paper is organized as follows. We present the  $CT-\Delta\Sigma$  modulator in Section II. The circuit design is described in Section III. Simulation results along with fabricated chip is presented in Section IV, followed by the conclusion.

## II. MODULATOR SYSTEM DESIGN

Figure 2 shows the  $CT-\Delta\Sigma$  modulator with cascade of resonator in feed-forward (CRFF) [3] summation to implement third order loop filter with a multi-bit quantizer. The main advantages of feed-forward architecture is that the cascaded integrators handle only a part of the input signal. And the integrators can have a relaxed dynamic range and scaling requirements. The poles of the loop filter H(s), which are the zeros of the NTF are placed at dc. The NTF high pass response as shown in figure 3. And by adding the local feed back loops (g) around pair of integrators, NTF zeros are moved away from dc and spread over the signal band. As a result both the in band noise and dynamic range of the modulator is improved [15].



Figure 2. Block diagram of the CT  $\Delta\Sigma$  modulator employing a third-order loop-filter.



Figure 3. Noise Transfer function.

In CT- $\Delta\Sigma$  modulator, more than 70% of the power is consumed by the operational amplifier (op-amp), which is a key design block in the loop-filter. In order to ensure low power operation of the modulator, bias currents in the op-amp need to be minimized for the given specification. Any decrease in the op-amp bias currents decreases the unity-gain frequency  $f_{un}$ , which in turn adds excess loop-delay in the integrator. Especially, in a multiple-feedback design, it is necessary to make sure that the extra poles in the op-amp does not affect the normal operation of CT- $\Delta\Sigma$  modulator. In addition, the finite DC gain and  $f_{un}$  of the op-amp impairs the characteristics of the loop-filter and thus modifies the resulting NTF [16], [17] . In this paper, a systematic design centering method explained in [17], [16] has been used for obtaining the loopfilter coefficients by including the effect of the integrator nonidealities.

## III. CIRCUIT DESIGN

In this section, a detailed description of circuit level blocks used in the CT- $\Delta\Sigma$  modulator is described.

#### A. Loop Filter

A third-order loop filter has been implemented with an oversampling ratio (OSR) of 64 and an achievable signal bandwidth of 48 kHz sampled at 6.144 MHz with an OBG of 3. A complete loop-filter schematic is shown in figure 4. The



Figure 4. Loop Filter of the designed third-order CT  $\Delta\Sigma$  modulator.

feed-forward co-efficient's  $(k_0, k_1, k_2, k_3)$  and summation are implemented using  $R_{11}, R_{21}, R_{31}, R_f$  resistors and a summing amplifier respectively. The input-referred noise of the loop filter is significantly dominated by the thermal noise from the input resistors and input differential pair of the first opamp [3]. In order to mitigate the thermal noise effect from input resistor  $(R_1)$ , the large value (80 K $\Omega$ ) has been chosen. Also, an appropriate  $g_m$  is chosen to mitigate the thermal noise contribution from input transistors. Further, to achieve a low  $\frac{1}{f}$  noise, PMOS input stage is used in first integrator of an op-amp whose design is discussed in section III-B [16].

#### B. Operational Amplifier

Figure 5 shows the schematic of the miller compensated two-stage op-amp. A PMOS differential pair is used as the first stage and class-AB buffer is used as the second stage. M1 to M6 are long length devices to mitigate the input referred flicker noise [16]. Here,  $C_c$  and  $R_c$  are the miller compensation capacitor and zero-nulling resistor whose values are chosen as 200 fF and 10  $K\Omega$  respectively. The first stage is biased to draw 10  $\mu A$  from the supply. To ensure the opamp common mode output voltage is held at  $V_{CM}$ , a common mode feedback (CMFB) loop is used in both stages of the opamp (See figs. 6(a), (b)). The total current drawn by the first

operational amplifier including the CMFB circuitry is 556 uA. The output of first stage ( $V_{o1p}$  and  $V_{o1m}$ ) in figure 5 is fed to the input transistors M7 and M10 in figure 6(a), which averages and compares the resultant voltage with the  $V_{ref}$  to tune the voltage ( $V_{CMFB1}$ ). The CMFB circuit shown in the figure 6(b) adds current to keep the output node ( $V_{outp}$  and  $V_{outm}$ ) at VCM.



Figure 5. Operational amplifier used in integrator.



Figure 6. (A) CMFB circuit for the first stage and (B) second stage CMFB circuit.

#### C. Comparator

The comparator used in the quantizer is shown in the figure 7. The comparator [18] is designed to provide sufficient regenerative gain and to avoid the effects of metastability. Here, the first stage uses a differential amplifier for reference subtraction. The amplifier is loaded with cross-coupled PMOS



Figure 7. Comparator circuit

latches to provide initial regeneration followed by a clocked latch. The second stage latch provides a large regenerative gain and also resolves the outputs to full logic level. The latch is disconnected from the input to avoid kickback noise. A reset phase is used to remove memory in the latches. The comparator has a resolution of 1  $\mu V$  and a delay of 2 ns. The comparator is biased with a 26 uA current and approximately dissipates 2.080 mW power at a clock rate of 6.144 MHz.

#### D. DAC and DWA

Though a number of implementations of DAC like resistive DAC and switched-capacitor DAC are possible. However, a current steering DAC [19] shown in figure 8 greatly reduces the slew requirement of first op-amp in the loop-filter which improves the stability of the system [17] has been designed for a current of  $1 \ uA$ . The DWA has been implemented by a 4 layer barrel shifter method [20].



Figure 8. Current steering DAC

#### **IV. SIMULATION AND EXPERIMENTAL RESULTS**

The third-order CT- $\Delta\Sigma$  ADC has been designed and taped out for fabrication in the 0.5  $\mu m$  C5FN-AMI CMOS process. Figure 9 shows the fabricated chip of the design with  $4.5 mm^2$ . The measured SNDR is using a 2.3 kHz input tone is 85 dB. Table I summarizes the performance of the modulator.

Table I MODULATOR PERFORMANCE SUMMARY

	This work
Process	$0.5 \mu m$
Supply Voltage	5 V
Sampling rate $(MHz)$	6.144
BW $(kHz)$	48
OSR	64
Quantizer resolution	4 - bit
Power Dissp. $(mW)$	5.44
$SNR_{max}(dB)$	85
FoM(pJ/conv.)	3.73



Figure 9. CTDSM fabricated chip picture.

## V. CONCLUSION

A low-power,  $CT-\Delta\Sigma$  modulator was designed in a 0.5  $\mu m$ C5 AMI CMOS process for data conversion employed in audio applications. The CT loop-filter coefficients were systematically obtained by incorporating the op-amp non-idealities. This method resulted in robust modulator NTF and lower static currents in the op-amps. The simulation results of the  $CT-\Delta\Sigma$ exhibit a peak SNDR of 85 dB, with a maximum stable input (MSA) of  $-2.14 \ dBFS$ . The modulator dissipates around 5.44 mW power from a 5 V supply and achieves a FoM of 3.731 pJ/bit.

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Figure 10. Simulated Output spectrum

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