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Efficient Design and Synthesis of Decimation Filters for Wideband Delta-Sigma ADCs

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Efficient Design and Synthesis of Decimation Filters for Wideband Delta-Sigma ADCs

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***Abstract*—A design methodology for synthesizing power-optimized decimation filters for wideband Delta Sigma ($\triangle\Sigma$) analog-to-digital converters (ADCs) for next-generation wireless standards is presented. The decimation filter is designed to filter the out-of-band quantization noise from a fifth-order continuous-time $\triangle\Sigma$ modulator, with 20 MHz signal bandwidth and 14-bits resolution. The modulator employs an oversampling ratio (OSR) of 16 with a clock rate of 640 MHz. Retiming, pipelining, Canonical Signed Digits (CSD) encoding has been utilized along with an optimized halfband filter to realize the power savings in the overall decimation filter. A process flow to rapidly design the optimized filters in MATLAB, generate the hardware description language (HDL) code and then automatically synthesize the design using standard cells has been presented. The decimation filter is implemented using standard cells in a 45nm CMOS technology occupies a layout area of $0.12\,mm^2$ and consumes 8 mW power from the 1.1V supply.**

***Index Terms*—Analog to digital converter, decimation filters, delta-sigma modulation, noise-shaping.**

I. Introduction

Delta-Sigma ($\triangle\Sigma$) Analog to digital converters (ADCs) are being increasingly used in wireless applications. The $\triangle\Sigma$ ADC, shown in in Fig. 1, is comprised of an analog modulator followed by a digital decimation filter. The $\triangle\Sigma$ modulator internally employs a lower resolution ADC and shapes the quantization noise, effectively pushing it to higher frequencies outside the signal band. Due to the oversampled nature of the $\triangle\Sigma$ ADCs this high-pass quantization noise can be digitally filtered out, and thus increasing the overall resolution of the ADC. The digital filter, following the modulator, filters out the out-of-band quantization noise and also reduces the sampling rate to the Nyquist rate of the ADC [1], [2], [3].

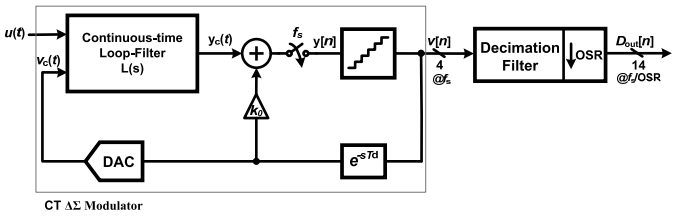

Figure 1. Block diagram of a Continuous-time Delta-Sigma ADC.

There has been a growing interest in employing continuous-time (CT) $\triangle\Sigma$ ADCs in next-generation radios [4]. Applications include CDMA2000, W-CDMA, multicarrier GSM, 802.16x, and LTE, RADARs. Recently, CT $\triangle\Sigma$ ADCs have attracted interest in Software-Defined Radio (SDR) and multi-standard communication platforms, which benefit from reconfigurable digital intensive ADC architectures [4], [5]. Thus, a rapid design and synthesis method is needed for design of $\triangle\Sigma$ decimation filters which not only consume less power, but are also reconfigurable and adaptable.

Traditionally, decimation filters have employed multirate and multistage architectures resulting in simple hardware which minimize filter word-lengths, eliminate the need of multipliers and reduce the number of registers required. Since the decimation filter operates at very high sampling rate, the multistage filter chain uses simpler filtering blocks in the initial stages to reduce power. The simplest possible decimation filter is realized using sinc filters ($sinc^K$), which are realized as a cascade of simple accumulators and differentiators. These filters are also called as CIC filters, i.e. cascades of comb and integrators, and can be implemented in a number of ways by employing polyphase structures[6], [7]. Even though these filters are simple to realize, the passband response of these filters presents significant amount of droop which may be too low to meet the passband edge ripple specifications. A second class of filter, called half-band filters (HBF), are used for a decimation factor of 2 and provides a sharp passband to stopband transition. In the early days of $\triangle\Sigma$ ADCs employed in audio codecs, a cascaded combination of CIC and HBF filters was judiciously employed to achieve a large decimation factor and high out of band quantization noise suppression[8]. Here, a finite impulse response (FIR) filter is used at the end of decimation chain to compensate for the droop in the signal band. Later, when $\triangle\Sigma$ ADCs were developed for wireless applications, this architecture has been modified to optimize for area and power[9], [10], [11], [12], [13]. Several techniques borrowed from the digital signal processor (DSP) architectures have been borrowed to optimized the custom designed decimation filters. These eclectic techniques include multirate filtering, pipelining, retiming, and employing power efficient number systems e.g. canonical signed digits (CSD)[14]. Several optimizations are also made during the synthesis of digital logic. Even though these techniques have been used in literature to design decimation filters, a systematic design flow for rapid prototyping is needed to bridge the gap between the filter design and transistor-level implementation.

This paper presents a design and synthesis flow for a digital decimation filter for a 5^{th}-order $\Delta\Sigma$ ADC, targeted for next-generation wireless networks. Low power, optimized filter topologies are investigated in this work and a process

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flow is presented for their automated synthesis and layout generation. The decimation filter is designed using a 45 nm CMOS technology using the standard cell based synthesis. The novelty of this work lies in the compilation of a process flow for rapid design of low-power decimation filters using the latest design tools. The process flow is intended towards rapid prototyping of decimation filters for reconfigurable $\Delta\Sigma$ ADCs employed in Software-Defined Radios.

The paper is organized as follows. We present the decimation filter chain architecture in Section III. The individual filter stages are described in Sections IV-VI, along with the hardware optimization techniques incorporated in the designs. Simulation results and design characterization is presented in Section VIII, followed by the conclusion.

II. $\triangle\Sigma$ ADC Architecture

A typical$\Delta\Sigma$ ADC for wireless applications has been used to demonstrate the decimation filter design flow. The specifications for the modulator and the decimation filter design are detailed in Table I. The CT $\triangle\Sigma$ modulator was designed to the satisfy the specifications of the next-generation wireless applications by incorporating a 5^{th}-order loop-filter and a 4-bit quantizer. Figure 2 shows the block diagram of the the modulator employing a 5^{th}-order, feed-forward, continuous-time loop-filter.

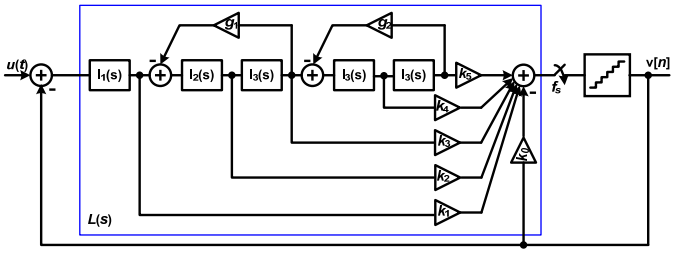

Figure 2. Block diagram of the CT $\Delta\Sigma$ modulator employing a fifth-order loop-filter.

The modulator is implemented using Active-RC stages (see Fig. 2) with two resonators to create noise-transfer function (NTF) zeros in the signal band.

The modulator's simulated spectrum is illustrated in Fig. 4. The achievable signal to quantization noise ratio (SQNR) for this design is 102 dB which corresponds to 16.7 bits. The quantization noise outside the signal band needs to be digitally filtered and decimated to the Nyquist rate of 40 MHz. Finally, the resolution of the $\triangle\Sigma$ ADC will be limited by the in-band thermal noise and the aliased quantization noise after decimation.

III. Decimation Filter Architecture

The designed decimator block diagram is shown in Fig. 5. The decimation filter is realized as a cascade of decimate-by-2 stages followed by an FIR equalizer. The multistage architecture allows most of the filter hardware to operate at a lower clock frequency, and have lower hardware complexity when compared to a single state decimator. Three Sinc filters are used for initial filtering, and for initial suppression of

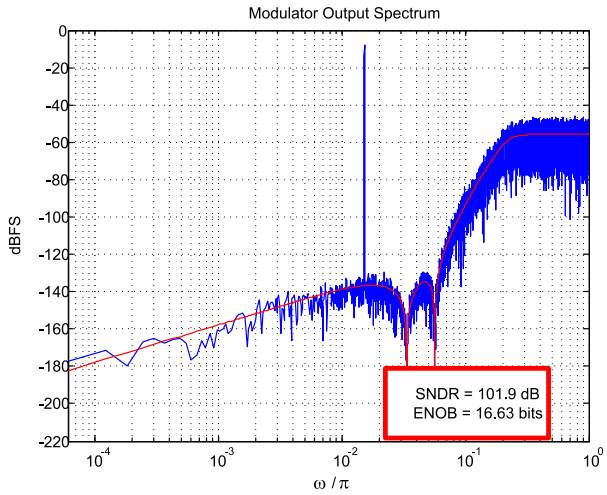

Figure 4. Simulated spectrum of the designed fifth-order CT $\Delta\Sigma$ modulator.

Table I
Modulator Performance and Decimator Requirements

Modulator		Decimation Filter	
Order	5	Input no. of bits	4
OBG	3	Passband ripple	<1 dB
Bandwidth	20 MHz	Passband transition	20-23 MHz
Sampling rate (f_s)	640 MHz	Stop-band attenuation	>85 dB
OSR	16	Decimated rate	40 MHz
MSA	0.81	Output rate	40 MHz
SNR	86 dB	SNR	86 dB (14 bit)

majority of the quantization noise. The Sinc filter cascade provides a clock rate decimation factor of 8. A halfband filter decimates the resultant signal to the Nyquist frequency of the ADC. The scaling block restores the filtered signal amplitude to full scale in order to maximize the dynamic range (DR) of the digital ADC output. A finite impulse response (FIR) equalizer is used to compensate for the droop in the Sinc decimation stages. All the filter stages have symmetric impulse response which ensures a linear phase response.

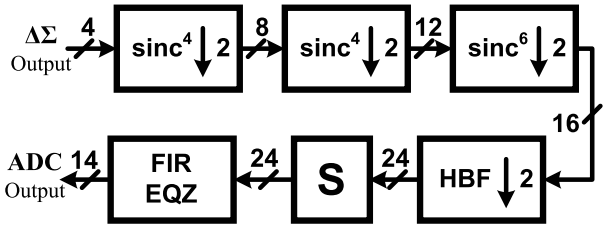

Figure 5. Delta-Sigma ADC decimation filter architecture.

A sample rate converter is ofter used after the decimation filter for allowing flexibility in the output sample rate for a direct interface to the digital receiver blocks [13].

IV. Sinc Filters

Three $Sinc^K$ filter stages are employed for initial quantization noise filtering and decimation. $Sinc^K$ filters offer an attractive choice for hardware implementation as they preclude the use of a digital multiplier. The filters use wrap-around

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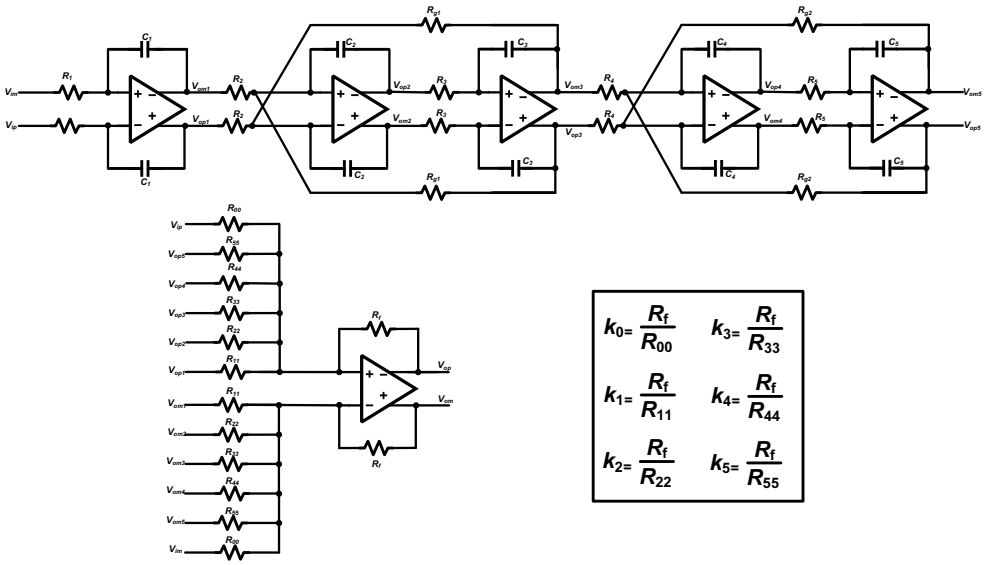

Figure 3. The a fifth-order loop-filter, employed in the ADC, with Active-RC implementation.

$2's$-complement binary arithmetic and are inherently stable. The multirate $Sinc^K$ filters are implemented as a Hogenauer structure as show in Fig. 6 [15]. The filter comprises of a cascade of K accumulators operating at the input clock frequency (f_s), followed by K differentiators in series clocked at $f_s/2$ frequency [2]. The transfer function of the $Sinc^K$ filter is given by

$$H_{sinc^K} = \left[\frac{1}{M} \cdot \frac{1 - z^{-M}}{1 - z^{-1}}\right]^K \tag{1}$$

where K is the number of stages and M is the decimation factor.

In order to reduce power consumption, the accumulators are implemented using *retiming* technique[14], i.e. the register in the forward path which checks propagation of the glitches in the combinatorial adder logic to the next stage. This reduces the glitching power in the accumulators. Moreover, a pipelining register, clocked at $f_s/2$, is used after the accumulator cascade to prevent the data at f_s clock rate from entering the slower differentiation stages [3]. The register widths (B_{max}) in the filters are selected according to the equation

$$B_{max} = K \cdot log_2\,(M) + B_{in} - 1 \tag{2}$$

where B_{in} is the input word length.

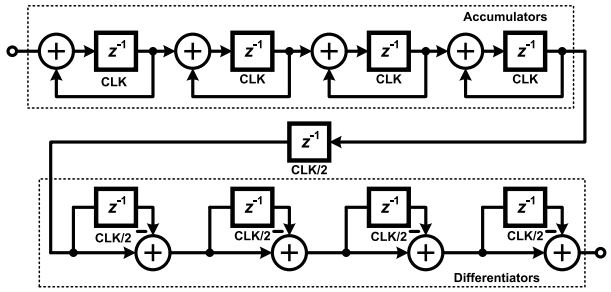

Figure 6. A multirate $Sinc^4$ decimation-by-2 filter.

The aliasing bands for the $Sinc^K$ filter lie between $\frac{mf_s}{M} - f_B$ and $\frac{mf_s}{M} + f_B$, where $m = 1, \ldots, (M-1)$ and f_B is the signal bandwidth. The attenuation in the aliasing bands is governed by the number of stages (K). The filters are designed so as to ensure the required 85 dB alias-band suppression at every stage. However, a larger value of K leads to a droop in the baseband response. Two $Sinc^4$ decimation-by-2 stages are followed by a $Sinc^6$ stage to effectively suppress the quantization noise shaped by the 5^{th}-order noise transfer function (NTF) of the modulator. The word lengths for the Sinc stages are 4, 8 and 12 respectively.

V. Halfband Filter

Halfband filters (HBF) are a class of filters which have their transition band centered around $f_s/4$ and exhibit a symmetric response (i.e. linear phase response). The HBF have odd tap weights equal to zero except for $n = 0$ and thus allowing these filters are implemented with half the number of multiplications than the usual filters. They can be designed to provide a sharp transition band and are well-suited for decimation by a fixed factor of two [2]. A non-deterministic search procedure based HBF design methodology, proposed by Saramaki has been employed [16]. The 110^{th} order filter achieves 90 dB stop-band attenuation and uses only 124 adders (no true multiplications). The designed halfband filter architecture is shown in Fig. 7. The filter employs five identical sub-filters (F_2), designed using adders and unit delay (z^{-1}) elements. The search procedure, encoded in the **designHBF** function in the $\Delta\Sigma$ Toolbox [17], determines the additional tap coefficients (F_1) such that the frequency response of the composite halfband filter is better than that of the sub-filter itself.

The tap coefficients of the filter are encoded using the Canonical Signed Digits (CSD) to reduce the number of computations [18]. CSD arithmetic minimize the number of addition operations required for multiplication by representing binary numbers with a minimum count of nonzero digits.

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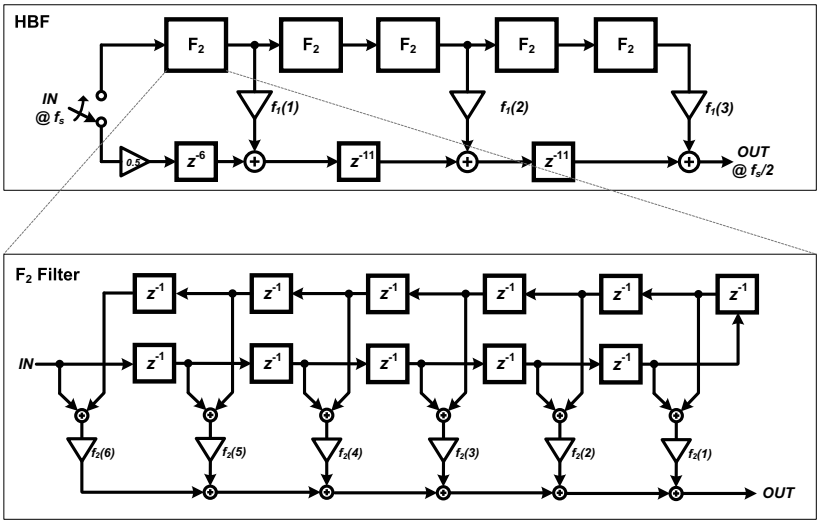

Figure 7. The Saramaki Half Band Filter [1], [16]

This decreases the power consumption and the area used by the filter while maintaining or increasing clock speed. The optimum coefficient word length equal to 24 bits was employed in the HBF. The additional 10 bits (on top of the 14 bit resolution) ensure that the aliased quantization noise is further attenuated by 60 dB with respect to the signal noise floor. This ensures that the desired in-band SNR is preserved [3].

VI. Scaling and Equalization

If the $\Delta\Sigma$ modulator input is large enough so that the internal states increase monotonically without being bounded, the loop will become unstable. This also sets a limit on the maximum input amplitude which can be accommodated by the $\Delta\Sigma$ modulator and is called the maximum stable amplitude (MSA). The MSA is less than the full scale range of the feedback DAC at in the front, and it decreases as the order of the modulator is increased. For the targeted fifth-order $\Delta\Sigma$ modulator, MSA is 81% of the full scale. The digital output of the $\Delta\Sigma$ modulator will be the four bit representation of the input signal with shaped quantization noise wiggling around it. After the out-of-band quantization noise has been sufficiently attenuated by the decimation stages below the noise floor level in the signal band, the signal is scaled to cover the full dynamic range provided by the digital representation. A scaling factor of $S = \frac{1}{0.825}$, slightly lower than $1/MSA$, is employed to prevent overflow in the subsequent filter stages. The scaling coefficient is CSD encoded and is implemented using nested Horner's rule to minimize power and area [3], [14].

The passband droop due to the Sinc filter cascade is equalized by a linear phase FIR filter. The filter operates at the Nyquist rate frequency (40 MHz). The FIR filter coefficients, to cancel the magnitude response of the Sinc filters, are obtained using the *Parks McClellan* algorithm (**firpm** function in MATLAB)[19]. A 64^{th}-order symmetric FIR filter equalizes the resulting passband response to 0 dB in the signal band. Again, the filter tap coefficients are encoded using CSD and implemented using Horner's rule.

VII. Simulation and Experimental Results

Each of the decimation filter stages were individually designed, simulated and optimized using MATLAB and Delta-Sigma Toolbox. Detailed simulations were performed to achieve the required ADC resolution with lowest possible power consumption. The frequency response of the Sinc filter stage is shown in Fig. 8. It can be observed that the resulting response of the the Sinc filter cascade exhibits over 100 dB attenuation in the alias bands. The signal

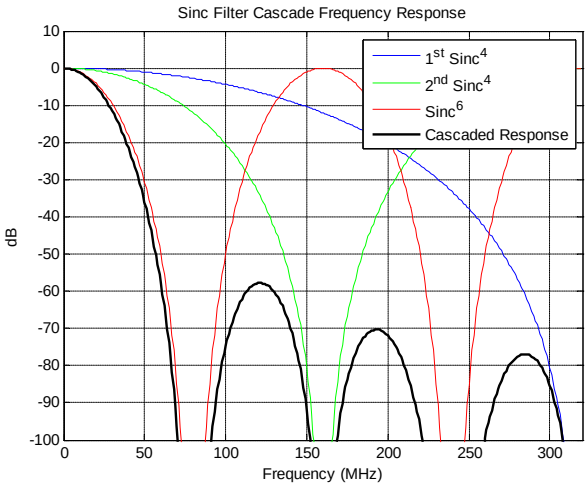

Figure 8. Frequency response of the individual Sinc filter stages and the cascaded Sinc response.

Fig. 9 shows the frequency response of the HBF seen in Fig. 7. Here, the alias band rejection of the HBF is greater than 90 dB which satisfies the 85 dB attenuation specification for the decimation filter.

An equalizer is employed to compensate for the droop in the signal band. Fig. 10 shows the equalizer (an FIR filter) frequency response which compensates for the droop in the decimation filter. The resulting passband ripple is less than 0.5 dB.

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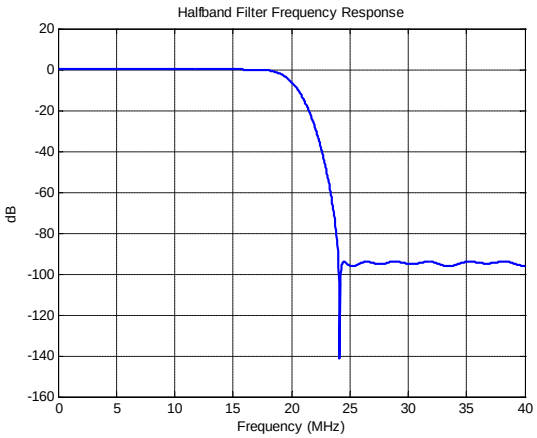

Figure 9. Frequency response of the designed Saramaki halfband filter.

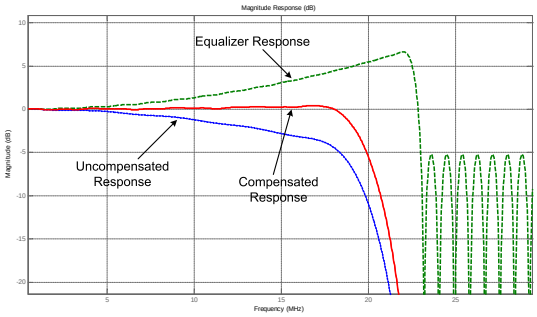

Figure 10. Decimation filter frequency response: Uncompensated response with droop, Equalizer response, and droop compensated response.

Fig. 11 illustrates the resulting frequency response of the cascaded decimation filters with quantized coefficients. It can be observed that the filter response meets the specifications outlined in Table I.

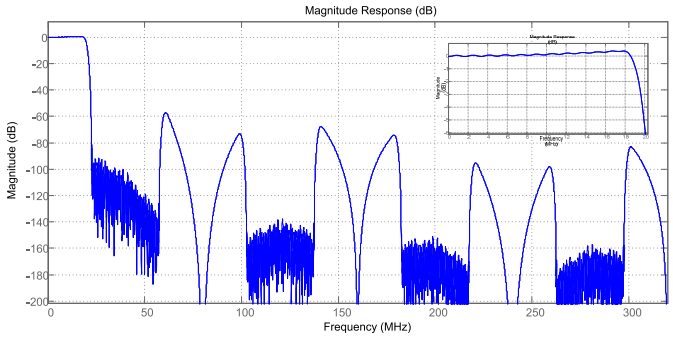

Figure 11. Cascaded decimation filter response. The passband response is shown in the inset.

VIII. Synthesis Results

The filters were translated into the optimized Verilog code using the MATLAB Filter HDL Coder toolbox [20]. Test benches were auto-generated and run in *Synopsys VCS* tool to verify the filter functionality. The generated verilog code was synthesized in 1.1V, 45 nm CMOS technology using the *Synopsis IC Compiler* tool, with power optimization options[21]. The synthesized design was placed and routed using the *Cadence Encounter* tool[22]. The power consumption of the decimation filter was estimated using the *PrimeTime-Px* tool[23], which estimated the dynamic power based on the switching activity corresponding to an applied stimulus. The filter power consumption was estimated using a sinusoidal tone equal to the MSA, and with a frequency of 5 MHz. The estimated power profile for the filter is listed in Table II. The synthesized decimation filter layout, shown in Fig. 12, occupies chip area equal to $0.12\,mm^2$.

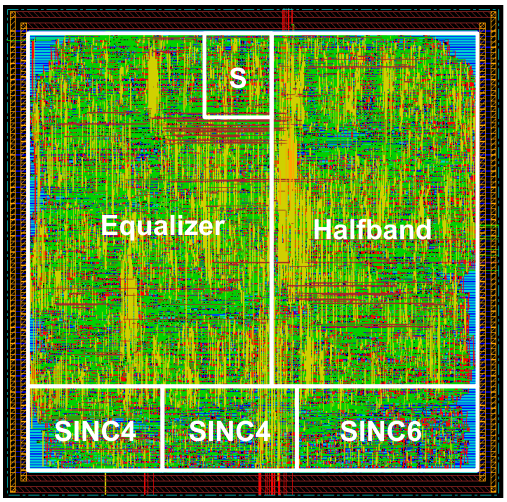

Figure 12. Layout of the chip generated using the automatic place and route tool.

Table II
Power Profile for the Decimation Filter, $V_{DD} = 1.1V$

Filter Stage	Dynamic Power (mW)	Leakage Power (μW)
$Sinc^4$ one	2.36	19.41
$Sinc^4$ two	1.13	22.34
$Sinc^6$	1.16	47.26
Halfband	1.28	152.44
Scaling Stage	0.38	11.13
Equalizer	1.73	537.88
Total	**8.04**	**771.10**

The decimation filter synthesis procedure, presented in this paper, relies heavily on the MATLAB filter design and HDL coder toolboxes. As an alternative, the filter design can be performed in any numerical tool like Mathcad or Scilab, and then the filter RTL can be manually coded and optimized for low-power consumption.

Fig. 13 shows the distribution of the dynamic power consumption in the decimation filter stages. It can be observed that the majority of the power dissipation is contributed by the first Sinc stage (operating at 640 MHz clock rate) and the equalizer FIR filter (operating at the decimated Nyquist rate of 40 MHz). The halfband filter power consumption has been optimized by using the techniques discussed earlier and contributes only 16% of the total power dissipation.

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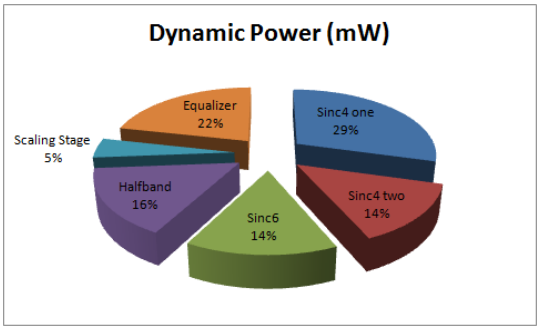

Figure 13. Pie chart distribution of the dynamic power consumption in the decimation filter stages.

IX. Conclusion

A systematic design procedure for the design of power optimized decimation filters for wideband CT $\triangle\Sigma$ ADCs has been presented. Several architectural techniques have been used to minimize power consumption in the decimation filter. The filters have been further optimized using MATLAB tools and synthesized using automated CAD tools. Simulation results have been presented to verify the decimation filter functionality. The presented design flow facilitates the design of low-power, fully-integrated CT $\triangle\Sigma$ ADCs for next-generation wireless applications.

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