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A *K*-Delta-1-Sigma Modulator for Wideband Analog to Digital Conversion

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***Abstract*— As CMOS technology shrinks, the transistor speed increases enabling higher speed communications and more complex systems. These benefits come at the cost of decreasing inherent device gain, increased transistor leakage currents, and additional mismatches due to process variations. All of these drawbacks affect the design of high-resolution analog-to-digital converters (ADCs) in nano-CMOS processes. To move towards an ADC topology useful in these small processes the *K*-Delta-1-Sigma (KD1S) modulator-based ADC was proposed. The KD1S topology employs inherent time-interleaving with a shared op-amp and *K*-quantizing paths and can achieve significantly higher conversion bandwidths when compared to the traditional delta-sigma ADCs. The 8-path KD1S modulator achieves an SNR of 58 dB (or 9.4-bits resolution) when clocked at 100 MHz for a conversion bandwidth of 6.25 MHz and an effective sampling rate equal to 800 MHz. The KD1S modulator has been fabricated in a 500 nm CMOS process and the experimental results are reported. Deficiencies in the first test chip performance are discussed along with their alleviation to achieve theoretical performance.**

***Index Terms*— Analog to digital converter, delta-sigma modulation, interleaved data converters, noise shaping, parallel delta-sigma, wideband ADC.**

I. Introduction

Continued CMOS scaling has enabled ever increasing device speeds leading to numerous standards and applications in wireless and optical segments. The integrated circuit technologies used to manufacture analog-to-digital converters (ADCs) are shrinking to enable more system functionality in a smaller chip area. This reduction in size comes at the cost of greater manufacturing variances, including circuit (transistor) characteristics, which limit the availability of precise components often required in an ADC. Further, the large increase in the number of wireless communication standards call for processing of the electromagnetic spectrum from 900 MHz to 10 GHz [1], [2]. The applications include cellular telephony, UWB, Wireless LAN, WiMAX and Cognitive Radio [3].

Nyquist rate ADCs like Flash ADCs have been used for higher-speed data conversion from 100's of MHz to several GHz's at lower resolution (5-8 bits) and pipelined ADCs for moderate resolution (10-14 bits) for 100-500 MHz range [4]. CMOS scaling benefits the Nyquist rate ADCs by realizing increasing higher sampling rates. However, the high speed of scaled CMOS is concomitant with the degrading intrinsic gain of the transistor, pronounced process variations and poor component matching. In order to design high-resolution pipelined ADCs in nano-CMOS with significant device offsets, extensive amount of digital calibration is required at the cost of increased area, latency and power consumption. However, since calibration requires another high-precision ADC or DAC for the calibration of the high-speed ADC, which entails the reference ADC/DAC to operate at a much lower clock frequency during the calibration sequence [5]. This may impair the effectiveness of the calibration at high speeds. This leads to limitations on the efficacy of the digital calibration and adaptive error cancellation methods with increased CMOS scaling. Thus investigating other ADC topologies which are inherently tolerant to device mismatches and nonlinearity is appropriate.

II. Delta-Sigma Analog-to-Digital Converters

It is known that the oversampling or delta-sigma ADCs trade sampling frequency with the signal bandwidth to achieve much higher signal-to-noise ratio (*SNR*). A delta-sigma ADC constitutes of a delta-sigma modulator (DSM) followed by digital filters and decimation stages [6]. The modulator employs oversampling, i.e. the sampling frequency is a multiple of the input signal bandwidth, defined as the oversampling ratio (*OSR*). The DSM loop shapes the quantization noise, Q_e, and moves it to higher frequency away from the baseband signal bandwidth. The noise shaping results in lower quantization noise in the signal bandwidth and the modulated noise can be filtered out digitally leading to a much higher signal-to-noise ratio (*SNR*). Thus, much of the analog signal processing is transferred to the digital domain which is favorable for the continued CMOS scaling [6].

The delta-sigma feedback loop is insensitive to device mismatch and nonlinearity in the forward path due to the high loop gain at the lower frequencies. Due to the feedback desensitization of the loop, simple, low-gain and high-hysteresis comparators can be employed. Also the op-amp's dc gain can be as low as the modest value of *OSR* and its unity gain frequency (f_{un}) can be comparable to the sampling frequency (f_s). However, due to oversampling the delta-sigma ADCs are narrow-band and the signal bandwidth is limited to

$$BW \le f_s / (2 \cdot OSR) \quad (1)$$

Therefore, the conventional delta-sigma ADCs can not achieve Nyquist-rate sampling as desired for wideband data conversion.

III. Time-Interleaved Delta-Sigma Modulators

A straightforward technique to increase the effective sampling rate with higher resolution is to time-interleave multiple high-resolution ADCs. The interleaved ADC consists of K parallel slow paths operating at f_s sampling frequency leading to $K{\cdot}f_s$ effective sampling rate. Many efforts in applying the interleaving or parallel techniques to DSMs have been reported [7]-[11]. However, such schemes, as shown in Fig. 1, achieve a maximum 0.5 bit of gain in resolution (or 3 dB increase in *SNR*) per doubling in the number of paths [11].

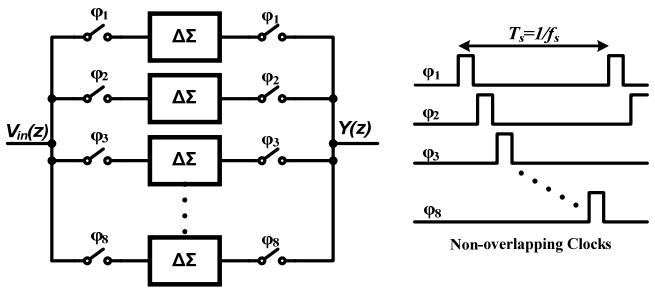

Figure 1 A time-interleaved or parallel delta-sigma modulator.

Time-interleaving of K delta-sigma modulators does not result in *true-noise-shaping* in frequency where the quantization noise is moved all the way to the frequency $K{\cdot}f_S/2$. Instead we observe noise-shaped ripples in the noise transfer function (NTF) of such a modulator with peaks at odd multiples of $f_s/2$ as shown in Fig. 2. This is due to the fact that the feedback signal in the delta-sigma loop arrives to the input only after a delay of T_s $(=1/f_s)$. Thus the time-interleaved or parallel DSMs do not quite stack up like the Nyquist rate ADCs. For a parallel DSM, the K-paths are mutually exclusive and typically require K different set of integrators and comparators. This leads to much higher power consumption. Also the mismatch across the K parallel paths cause signal dependent spurious tones and folding of noise into the baseband and thus lowering the achievable *SNR* [11].

In order to achieve true noise shaping with interleaving of delta-sigma modulators, the output of each modulator must be fed back to the corresponding input summing within a delay equal to T_s/K. This defeats the purpose of interleaving slow DSMs to realize a higher data rate ADC as each of the paths now have to settle within T_s/K time interval.

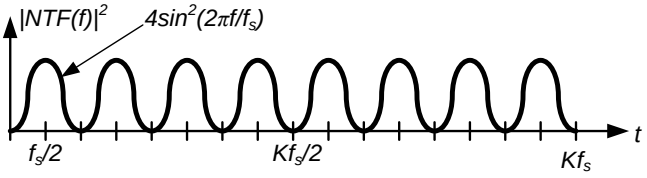

Figure 2 Noise shaping response for a first-order time-interleaved DSM.

IV. The K-Delta-1-Sigma Modulator

A. KD1S Topology

Consider a K-path Delta-Sigma modulator with a shared integrator among the K-paths. This topology termed as K-Delta-1-Sigma (KD1S) modulator is shown in Fig. 3 [6]. Here, the KD1S modulator is clocked by K phases of a clock with rate equal to f_s. The effective sampling rate of the modulator is set by the spacing between the edges of the clock phases and given as

$$f_{s,new} = K \cdot f_s \tag{2}$$

These K non-overlapping clock phases are generated by the circuit shown in Fig. 4. If the phases cane be tapped from a ring oscillator, designed using inverters with 10 ps delay, an effective sampling frequency ($f_{s,new}$) of 100 GHz can be achieved [6]. However, the maximum achievable effective sampling rate is determined by the path settling time in the KD1S modulator. Also, summing of the K-path outputs, $y_k[n]$, k=0,1,..,(K–1), using a fast adder leads to a path filter response of $(1–z^{-K})/(1–z^{-1})$, which acts as a decimation filter. As shown in Fig. 3, the input sampling phase for a path lasts for T_s/K time while the integrating phase has duration equal to $T_s/2$. As we can observe the integrator is connected to $K/2$ distinct paths at any given time, and thus spreading the sampled input signal across $K/2$ paths.

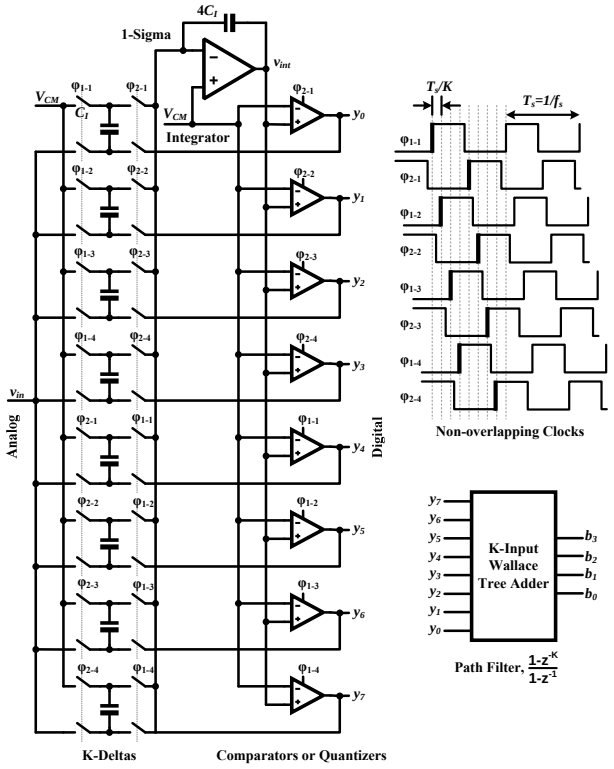

Figure 3 The K-Delta-1-Sigma modulator topology.

Since a single opamp is shared across all the K paths, the forward path mismatches are minimized. The offsets of each of the comparators are desensitized by the large integrator gain. It is also intuited that the spreading of signal across the K-paths will average out the mismatch effects in the feedback paths. The integrator can be designed with an op-amp with a unity gain frequency (f_{un}) equal to a small multiple of f_s, the clock rate. This obviates the need for a high-speed op-amp for ultra high-speed (GHz range) oversampling.

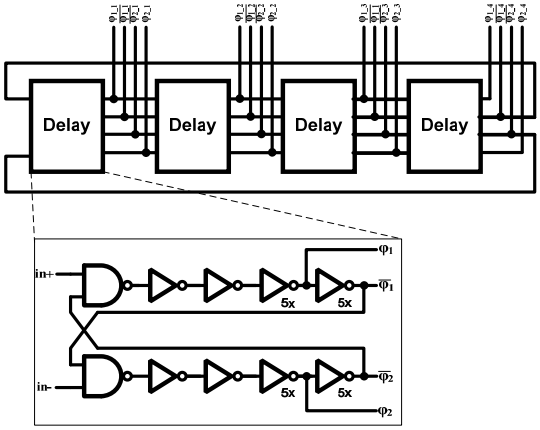

Figure 4 Circuit used to generate 8 non-overlapping clock phases.

In order to achieve true first-order noise shaping, the comparator in each of the path must fully respond to the partial settling of the integrator within $T_s/(2K)$ time interval. In other words, the quantization noise in the modulator is differentiated in every T_s/K *time-slice*. The noise transfer spectrum for the KD1S modulator is shown in Fig. 5 and compared with the noise shaping of a parallel DSM. Here, the quantization noise is pushed out to frequencies as high as $K{\cdot}f_s/2$ and thus achieving noise-shaping similar to a first-order delta-sigma modulator operating with a $K{\cdot}f_s$ clock rate. The noise transfer function for ideal KD1S is

$$NTF(f) = 2\sin\left(2\pi f / Kf_s\right) \tag{3}$$

and the effective number of bits is given as

$$N_{\text{eff}} = N - 0.566 + 1.5{\cdot}\log_2(OSR{\cdot}K) \tag{4}$$

Thus the KD1S topology seen in Fig. 3 achieves a 1.5 bit gain in resolution per doubling in the number of paths. In other words, doubling of the number of paths has the same effect as doubling the *OSR*.

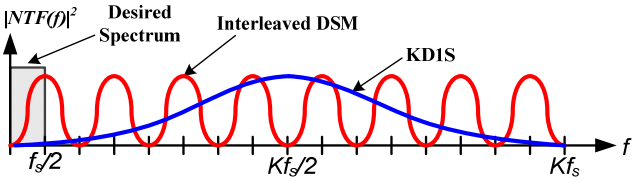

Figure 5 True wideband noise shaping using a *K*-Delta-1-Sigma Modulator.

B. Simulation Results

The simulation result for a KD1S modulator with ideal components is illustrated in Fig. 6.

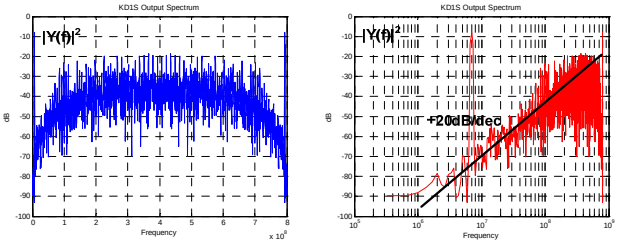

Figure 6 Simulation results (PSD of the output with linear and log frequency axes) for KD1S modulator with ideal components.

Here $K = 8$ paths, each with a clock frequency (f_s) of 100 MHz are employed. The effective sampling rate $f_{s,\text{new}}$ is equal to 800 MHz. The measured (using MATLAB) signal to noise ratio (SNR) for a signal bandwidth of 6.25 MHz (i.e. $K{\cdot}OSR = 8{\times}8 = 64$) is equal to 58 dB or 9.43 bits in resolution. This establishes the true first-order noise shaping in a KD1S modulator.

C. Noise Flow in the KD1S Modulator

Figure 5 illustrates the design intuition behind the first-order noise shaping in a KD1S. Here the during phase $\varphi_{2\text{-}1}$, the first comparator quantizes the integrator output (v_{int}) and passes the output y_1 onto the first delta block within the time interval less than $T_s/(2K)$.

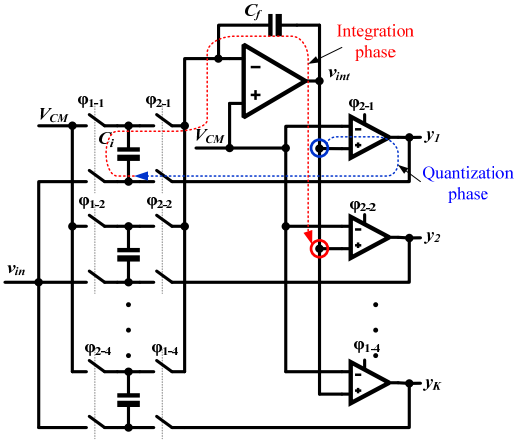

Figure 7 Illustration of the noise-shaping flow in a KD1S modulator.

When the $\varphi_{2\text{-}1}$ switches close, the error signal ($v_{\text{in}}[n]$–$y_1[n]$) is fed back to the integrator. Now the integrator makes an initial push during the next $T_s/2K$ time interval and updates the integrator output v_{int}. This new v_{int} value is now quantized (at phase $\varphi_{2\text{-}2}$) by the second comparator in the following time-slice and the error ($v_{\text{in}}[n{+}1]$–$y_2[n{+}1]$) is fed back to the integrator. This cycle repeats itself for all the paths with an unbroken noise shaping sequence. Also note that for each of the paths, noise differentiation is performed and cycled back to the node v_{int} with a time-slice of T_s/K. Simulations show that if this noise shaping sequence is broken, the *SNR* of the KD1S modulator drops. Thus for optimum performance, the comparators must be clocked on an earlier clock-phase such that the nose v_{int} has the latest information. For example, if the comparator delay (T_{comp}) follows the condition

$$T_s/2K < T_{comp} \le T_s/K\,, \tag{5}$$

then the first comparator should be clocked on the phase $\varphi_{1\text{-}4}$ instead of $\varphi_{2\text{-}1}$, so that v_{int} gets the latest information fed back to it through the integrator.

D. Effects of the Comparator Delay

In a KD1S modulator the comparator is implemented using a simple regenerative latch. Typically in a CMOS process, the cross coupled latch regeneration time (τ_{reg}) is inversely related to the f_T of the transistors and is in the order of several GHz's in nano-CMOS. The comparator delay, T_{comp}, is proportional

to τ_{reg}. Thus the KD1S modulator can be designed to operate at the rates governed by the comparator settling. We can still achieve noise-shaping when the path settling time is larger than T_s/K at the cost of larger in-band noise and reduction in *SNR*. Figure 8 demonstrates the effect of comparator delay on the resulting KD1S *SNR*.

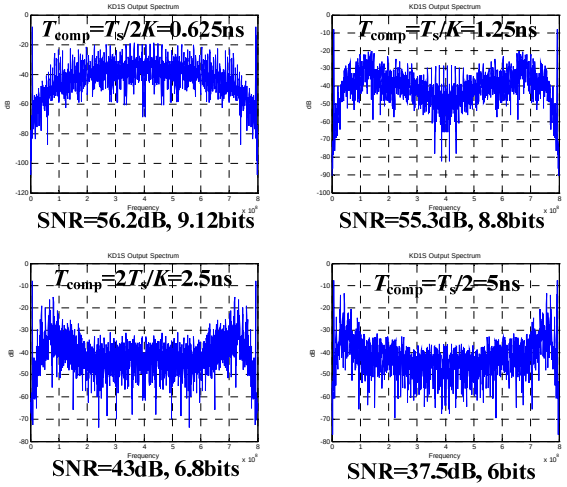

Figure 8 Effects of comparator delay on the SNR of a KD1S modulator.

Here, the bit resolution degrades from 9-bits to 6-bits as we increase the comparator delay from $T_s/2K$ to $T_s/2$. From these results, the optimum operating delay of the comparator is T_s/K.

V. Chip Test Results

The test chip containing a KD1S modulator fabricated in 500 nm, 5V CMOS process is illustrated in Fig. 9. Here, the 8-path outputs are decimated (resampled) at f_s = 100 MHz clock and processed off-chip.

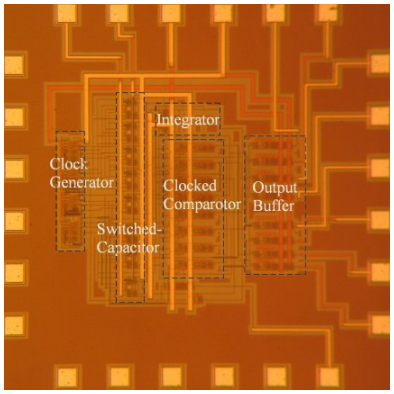

Figure 9 Chip micrograph for the KD1S modulator fabricated in 500 nm CMOS.

The *K*-path output data is acquired using a mixed signal oscilloscope and then post-processed using MATLAB. Figure 10 shows the PSD of the output of the KD1S modulator for a 4 V_{p-p} input tone with a frequency of 2 MHz, with true first-order noise-shaping. The measured SNR for a signal bandwidth of 6.25 MHz ($K{\cdot}OSR$ = 64 with $f_{s,new}$ = 800 MHz) is 30 dB which is equivalent to 5 bits in resolution. The measured chip results fell short of the expected KD1S ADC performance because of a mistake made in the connection of the clock signals. This mistake introduced an inherent $T_s/4$ clock jitter in two of the eight paths, and thus amplitude modulation in the data converter's output spectrum [6]. The clock connections were fixed and the modified designs are currently being fabricated. It should be noted that this mistake wasn't caught prior to fabrication because at the time we didn't have Matlab interfaced with SPICE simulations to determine SNR from the SPICE-generated digital output data. Matlab scripts are now available for anyone to download and use [6].

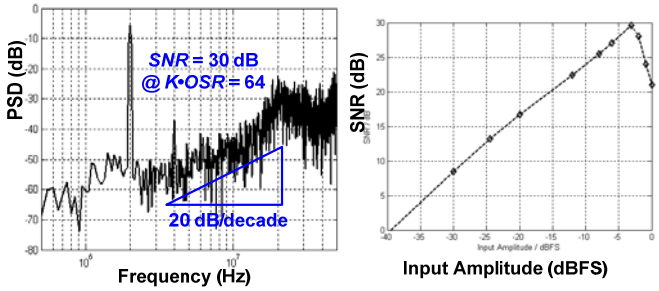

Figure 10 Measured Spectrum and SNR vs. input amplitude plot for the KD1S modulator.

VI. Conclusion

The proposed KD1S modulator exhibits true wideband noise shaping with minimal path mismatches. Simulation results have been presented to corroborate the theory. A preliminary test chip was fabricated to successfully demonstrate the concept. Test results are discussed along with identified improvements for the future designs.

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