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Indirect Compensation Techniques for Three-Stage Fully-Differential Op-amps

Vishal Saxena, *Student Member, IEEE* and R. Jacob Baker, *Senior Member, IEEE*

***Abstract*— As CMOS technology continues to evolve, the supply voltages are decreasing while at the same time the transistor threshold voltages are remaining relatively constant. Making matters worse, the inherent gain available from the nano-CMOS transistors is dropping. Traditional techniques for achieving high-gain by cascoding become less useful in nano-scale CMOS processes. Horizontal cascading (multi-stage) must be used in order to realize high-gain op-amps in low supply voltage processes. This paper discusses indirect compensation techniques for op-amps using split-length devices. A reversed-nested indirect compensated (RNIC) topology, employing double pole-zero cancellation, is illustrated for the design of three-stage op-amps. The RNIC topology is then extended to the design of three-stage fully-differential op-amps. Novel three-stage fully-differential gain-stage cascade structures are presented with efficient common mode feedback (CMFB) stabilization.**

Simulation results are presented for the designed RNIC fully-differential three-stage op-amps. The fully-differential three-stage op-amps, designed in 0.5 µm CMOS, typically exhibit 18 MHz unity-gain frequency, 82 dB open-loop DC gain, nearly 300 ns transient settling and 72° phase-margin for a 500 pF load.

***Index Terms*—CMOS Amplifiers, fully-differential, nano-CMOS, Op-amp compensation, three-stage op-amps.**

I. Introduction

OPERATIONAL Amplifiers are an important building block in the modern integrated systems. They are used in wide variety of circuits including data-converters, analog filters, voltage references, and regulators. However, continued scaling in CMOS processes has continuously challenged the established paradigms for operational amplifier (op-amp) design. As the feature size of CMOS devices shrinks, enabling yet faster speeds, the supply voltage (V_{DD}) is scaled down to enhance device reliability. The higher speed achieved with CMOS scaling is concomitant with a reduction in transistor's inherent open-loop gain ($g_m.r_o$). Further with device scaling, the threshold voltage of transistors doesn't scale well with the supply voltage, resulting in shrinking the voltage headroom for analog designs. In addition to these challenges, the process variations become more pronounced leading to significant offsets in op-amps due to the device mismatches [1], [2].

In order to meet the gain requirements of op-amp in nanoscale CMOS processes and low supply voltage, three or higher stage op-amp topologies have become important. In this paper we review the indirect-feedback compensation method for designing low-voltage three-stage op-amps and extend it to the design of fully-differential, three-stage CMOS op-amps. A novel cascaded fully-differential, three-stage op-amp topology is presented with simulation results, which is tolerant to device mismatches and exhibits superior performance.

II. Indirect Feedback Compensation

Indirect Feedback Compensation is a lucrative method to compensate op-amps for higher speed operation [1]. In this method, the compensation capacitor is connected to an internal low impedance node in the first gain stage, which allows indirect feedback of the compensation current from the output node to the internal high-impedance node. Further, in nano-CMOS processes low-voltage, high-speed op-amps can be designed by employing a split-length composite transistor for indirect compensation instead of using a common-gate device in the cascode stack [3].

Fig. 1 illustrates the splitting of an n-channel MOSFET (NMOS) or a p-channel MOSFET (PMOS) to create a low impedance internal node-A. For an NMOS, the lower device, M1B, will be in cut-off or triode region but never in saturation rendering node-A to be a low impedance node [3].

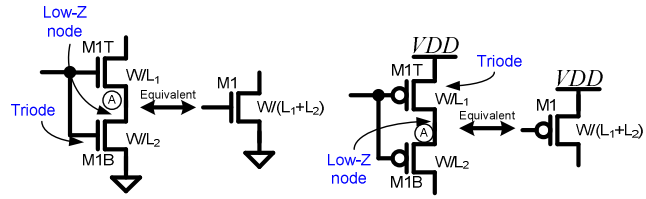

Fig. 1. Illustration of the split-length NMOS and PMOS devices and the low-impedance nodes amenable for indirect compensation [1], [1].

In two-stage op-amps employing indirect compensation, pole splitting is achieved with a lower value of the compensation capacitor (C_C) and with a lower value of second-stage transconductance (g_{m2}). This results in a much larger unity gain frequency (f_{un}) attainable by the op-amp, with lower power consumption and a smaller layout, when compared to the Miller compensated op-amps [1].

III. Indirect Compensation Of Three-Stage Op-Amps

Continued interest in the three-stage op-amp design has seen numerous three-stage op-amp design techniques [4]-[8]. However, they exhibit either complex implementation or larger power consumption when compared to the commonly used two-stage op-amps. This section provides a tutorial on the design techniques, introduced by the authors in [9], which result in high-speed, offset tolerant, and low power three-stage

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op-amps.

A. Multi-Stage Op-amp Biasing

Biasing is an important concern when designing multi-stage op-amps. If all the gain stages of the multi-stage op-amp are not biased properly with the intended overdrive voltages, the bias currents and hence the transconductances (g_m) and gains of the amplifying stages remain undefined. This may worsen the performance of the op-amp, consume larger current and can even push the op-amp towards instability.

Consider the three-stage op-amp topology illustrated in Fig. 3. Here diff-amps are used for the internal gain stages, both of which are biased with the same reference, V_{biasn}. In this topology, the voltage levels of the nodes 1 and 2 are set to be approximately equal to V_{biasp}, due to symmetry in each of the diff-amps. Thus the bias currents in all the three gain stage branches are well defined, and their g_m's and the DC gains are precisely fixed. A diff-amp is not used in the last stage due to its limited output swing. Alternatively, if we had a common-source gain stage as the second stage in the op-amp, the drain voltage of transistors in second stage (node-2) will be set by the contention between the PMOS current source and the NMOS current sink. In this scenario, the voltage at node-2 will not bias correctly in the presence of large device mismatches.

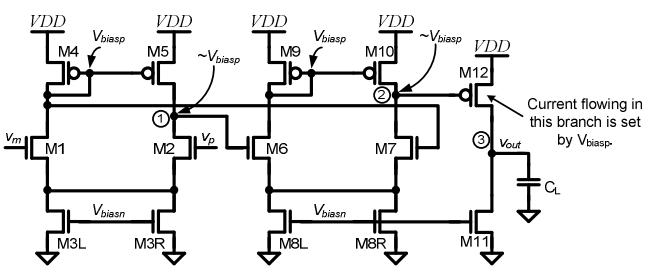

Fig. 3. Biasing scheme for the three-stage op-amp, where all gain stages are biased properly with known bias currents flowing in all branches.

B. Three-Stage Op-amp Compensation

The indirect compensation technique, employing split-length devices, is applied to three-stage op-amp design. A reversed nested compensation topology is used so that the output is not loaded by both of the compensation capacitors, which results in larger unity gain frequency (f_{un}). Fig. 4 shows a reverse-nested indirect-compensated (RNIC), pseudo class-AB, three-stage op-amp. A stack of maximum three transistors is used to realize the low-V_{DD} gain stages.

In this topology an NMOS diff-amp is cascaded with a PMOS diff-amp which is followed by a PMOS common-source gain stage. The PMOS diff-pair in second stage employs wider devices to increase the input common-mode range of the second stage. A split-length diff-pair (SLDP) is used for indirect compensation in order to achieve higher PSRR [9]. A diff-amp is used in the second stage to ensure that the third stage is correctly biased. The compensation capacitor C_{C1} is used to indirectly feedback the compensation current i_{C1} from the output of the second stage (node-2) to the output of the first stage (node-1). Similarly, capacitor C_{C2} is used to indirectly feedback current i_{C2} from node-3 to node-1. The compensation capacitance must be connected across two nodes which are moving in opposite direction [9].

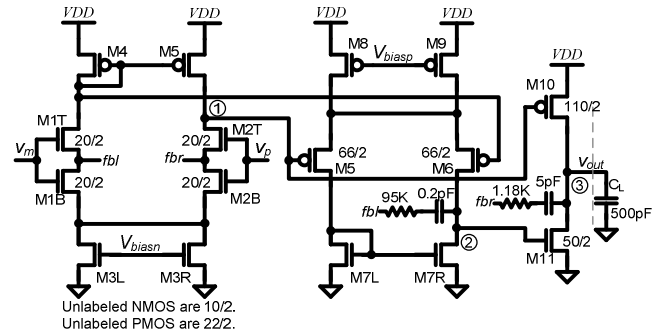

Fig. 4. A low-power, pole-zero cancelled, pseudo class-AB, RNIC, three-stage op-amp driving 500pF load.

C. Small Signal Analysis

The small signal model for the RNIC three-stage op-amp is shown in Fig. 5. Here, g_{mc1} and g_{mc2} are the transconductances of transistor M2T and M1T respectively. R_{C1} and R_{C2} are the impedance attached to the nodes *fbr* and *fbl* respectively, which are both roughly equal to $1/\sqrt{2}g_{m1}$. Here, g_{mk} is the transconductance of the kth gain stage while R_k and C_k are the resistance and capacitance respectively, attached to the node-k in the op-amps (k =1, 2, 3). After applying nodal analysis to the small signal model shown in Fig. 5, the resulting transfer function can be written as [9]

$$H(s) \approx \frac{A_{OL}\left(1+b_1 s+b_2 s^2\right)}{\left(1+\frac{a_0}{a_1}s\right)\left(1+\frac{a_2}{a_1}s+\frac{a_3}{a_1}s^2\right)\left(1+\frac{a_4}{a_3}s+\frac{a_5}{a_3}s^2\right)} \quad (1)$$

The dc gain A_{OL} is equal to $-g_{m1}R_1 g_{m2}R_2 g_{m3}R_3$ and the unity gain frequency is given as

$$f_{un} = g_{m1}/\left(2\pi C_{C2}\right) \quad (2)$$

and the dominant pole is located at

$$p_1 \approx -1/\left(g_{m3}R_3 g_{m2}R_2 R_1 C_{C2}\right) \quad (3)$$

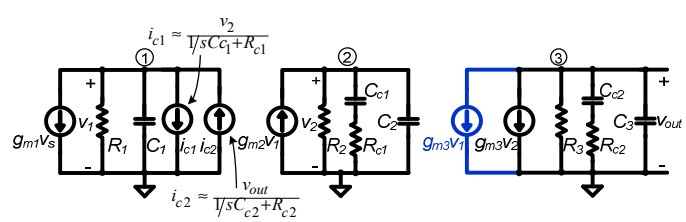

Fig. 5. Small signal analytical model for the RNIC three-stage op-amp. The highlighted $g_{m3}v_1$ path is added for the class-AB topology.

D. Pole-Zero Cancelation

From the small-signal transfer function seen in Eq. 1, the LHP zeros can be cancelled with the non-dominant poles $p_{2,3}$. This is achieved by equating the respective quadratic terms:

$$1+b_1 s+b_2 s^2 = 1+\left(a_2/a_1\right)s+\left(a_2/a_1\right)s^2 \quad (4)$$

The pole-zero cancellation leads to the following design

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criterions:

$$R_{C1} \approx \frac{C_L}{g_{m3}C_{C2}}, R_{C2} \approx \frac{C_{C1}}{g_{m3}C_{C2}^2}\left(C_L + C_{C2}\right) \approx \frac{C_{C1}}{C_{C2}}R_{C1} \quad (5)$$

Note that the design criterions are independent of the parasitic nodal resistance and capacitance values. The pole-zero cancellation leads to real pole-zero doublets located at [9]

$$p_2 = z_1 \approx \frac{-1}{R_{C1}C_{C1}} = \frac{-g_{m3}C_{C2}}{C_{C1}C_3} \quad (6)$$

$$p_3 = z_2 \approx \frac{-1}{R_{C2}C_{C2}} = \frac{-g_{m3}C_{C2}}{C_{C1}\left(C_3 + C_{C2}\right)} = \frac{p_2}{1 + C_{C2}/C_3} \quad (7)$$

From Eq. 6 and 7, we can see that the non-dominant pole-zero doublets appear close together in the frequency domain. The pole-zero doublets should be placed at a frequency higher than the f_{un} of the op-amp, which results in the upper bound on f_{un} [9]

$$f_{un} \le \frac{1}{2\pi}\sqrt{\frac{g_{m1}g_{m3}}{C_{C1}C_3}} \quad (8)$$

IV. Fully-Differential Three-Stage Op-Amps

Fully-differential (FD), three-stage op-amps can be implemented by extending the design techniques presented in Section III. A FD op-amp requires the output common mode level to be balanced by a common-mode feedback (CMFB) loop. The first topology in the logical sequence is the one with a single CMFB loop around all the three stages. Topologies based upon this block diagram have been proposed in [10], [11] and [12]. However, it is observed through simulations that the CMFB loop disturbs the biasing of the second and third stages as the common mode levels at node-1 and node-2 vary widely. This variation affects the stability of the three stage opamp as g_{m2} and g_{m3} keep varying with the common mode feedback voltage (V_{CMFB}). Also when pole-zero cancellation is employed to stabilize the op-amp, a large variation in g_m's may lead to the degradation of the compensation scheme.

Thus instead of using a CMFB loop across all the gain stages, it can be employed in the last two stages or just in the last gain stage. This design approach is demonstrated through the block diagram in Fig. 6 (a). Alternatively, the output common-mode level can also be adjusted by controlling the current only in the output buffer. This design approach, depicted in Fig. 6 (b), is simple to implement and consumes lowest power of all possible FD, three-stage topologies.

A robust, fully-differential, three-stage op-amp topology is presented in Fig. 7. Here, two single-ended differential amplifiers are used symmetrically to construct the second gain stage. One of the inputs of the second stage diff-amps are connected to the PMOS bias generated by the first stage, which should be same as V_{biasp}. The other inputs are connected to the differential outputs of the first stage. Because of the symmetry in the diff-amps, the bias levels for second and third gain stages are precisely set.

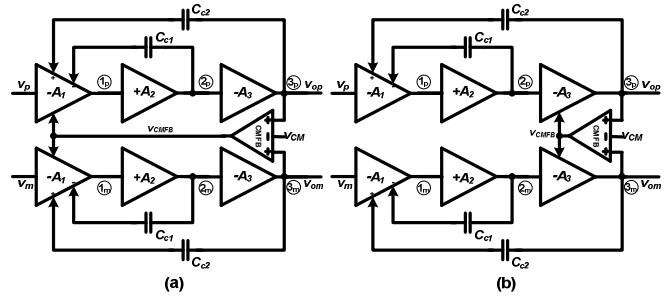

Fig. 6. Block diagrams of three-stage fully-differential op-amp topologies employing indirect compensation.

This scheme works well even in the presence of large offsets. Here, CMFB is implemented only in the output buffer. The CMFB loop uses transistors in triode region, in the source of the output buffer NMOS, to control the output common-mode level and set it to V_{CM} [1].

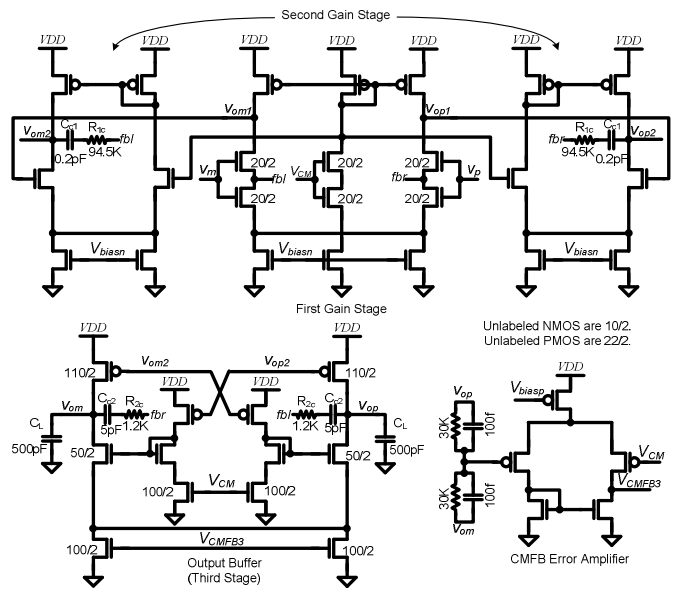

Fig. 7. A low-power, pole-zero cancelled, class-AB RNIC, three-stage op-amp driving 500pF load.

V. Simulation Results And Performance Comparison

The FD three-stage op-amp topology, seen in Fig. 7, was implemented in a 0.5 µm CMOS process to drive a 500 pF off-chip load. The simulated frequency response for the proposed FD op-amp is shown in Fig. 8.

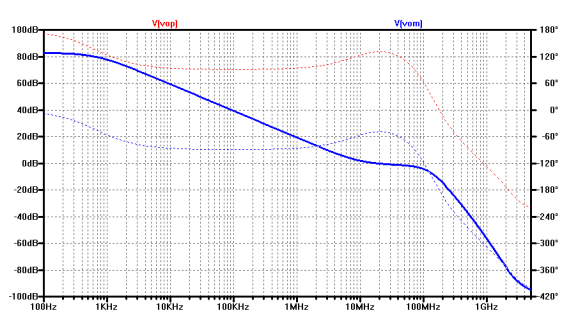

Fig. 8. Simulated frequency response of the three-stage fully-differential op-amp seen in Fig. 8. Here A_{OL}=82 dB, f_{un}=18 MHz and PM≈72°.

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Fig. 9 displays the DC sweep for the FD three-stage op-amp exhibiting a 82 dB DC gain.

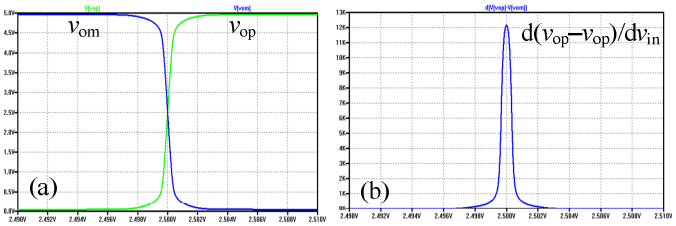

Fig. 9. Simulated DC behavior of the three-stage fully-differential op-amp seen in Fig. 8. Here, the DC gain (A_{OL}) is 12,000 or 82 dB.

Fig. 10 shows the step input (small and large) transient response of the op-amp. For the transient simulations, the fully-differential op-amp is driven single-ended with external resistors in a negative unity-gain configuration.

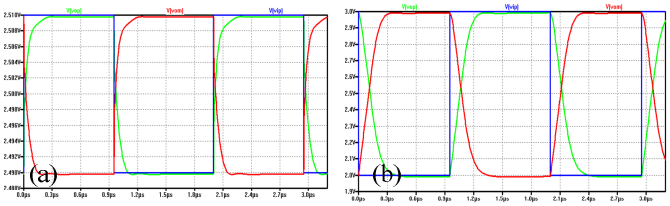

Fig. 10. Simulated small (20 mV) and large input (1 V) step response for the three-stage fully-differential op-amp, seen in Fig. 8, in the negative unity-gain configuration. The 99% settling time (t_S) is 300ns for a 20mV input step.

A performance comparison of the presented FD op-amp topology designed with the previously reported three-stage designs is presented in Table I. The figure of merit metrics, $FoMs = f_{un}C_L/V_{DD}I_{DD}$ and $FoM_L=SR.C_L/V_{DD}I_{DD}$, are used to compare the performance of the op-amps as in [8]. The proposed RNIC fully-differential op-amps display higher *FoM*s, faster transient settling and desirable phase margins. The presented op-amps can be further optimized for power by using smaller bias currents in the second stage. Even though in this work, the simulations are shown for a 0.5 µm CMOS technology, the RNIC FD op-amps should scale well in a nano-CMOS process. This is due to the fact that the biasing of these op-amps is expected to tolerate large device mismatches and that the gain stages are low-voltage by design.

VI. Conclusion

The proposed RNIC, fully-differential, three-stage op-amps exhibit desired performance at high as well low load capacitances. The op-amps exhibit large dc gain, and settling as fast as a corresponding two-stage amplifier, with minimal excess power consumption and smaller layout area. The fully-differential, three-stage, RNIC op-amps presented in this work are elegant, low-voltage, offset tolerant and hence manufacturable in a nano-CMOS processes.

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TABLE I
THREE-STAGE OP-AMP PERFORMANCE COMPARISON

	C_L (pF)	V_{DD} (V)	I_{DD} (mA)	Power (mW)	f_{un} (MHz)	<SR> (V/µs)	C_{C1}, C_{C2} (pF)	A_{OL} (dB)	<t_S> (ns)	PM	FoM_S	FoM_L
AFFC [4]	100	1.5	0.17	0.25	5.5	0.36	5.4,4	100	510	61°	2157	1413
TCFC [5]	150	1.5	0.03	0.045	2.85	1.04	1.1, 0.92	100	2000	59°	9500	3450
RNMC VB NR [6]	15	3	0.48	1.44	19.5	13.8	3, 0.7	83	75	56°	209	149
RNMCFNR [7]	500	3	0.085	0.255	2.4	1.8	11, 0.35	109	780	58°	4706	3529
RAFFC [8]	500	3	0.105	0.315	2.4	1.95	11, 0.35	112	530	58°	3810	3095
RAFFC LP [8]	500	3	0.03	0.105	1.1	1.29	11, 0.35	113	1000	56°	5238	6143
SMCNR [8]	150	1.5	0.014	0.021	1.6	0.65	2.2, 0	113	1300	57°	11429	4643
Buffered RNMC [12]	100	3	0.285	0.342	8.9	5.5	2, 0.65		2400		2602	1608
RNIC-FD (this work)	**30**	**3**	**0.4**	**1.2**	**12**	**10**	**4,4**	**82**	**275**	**85°**	**300**	**250**
RNIC-FD (this work)	**500**	**3**	**0.4**	**1.2**	**20**	**8**	**5, 0.2**	**82**	**300**	**72°**	**8333**	**3333**