ELECTRICAL SWITCHING PROPERTIES OF TERNARY AND LAYERED CHALCOGENIDE PHASE-CHANGE MEMORY DEVICES

by

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ABSTRACT

Due to the increasing demand for products which use Non-Volatile Memory (NVM) and the near realization of the scaling limits of Flash [1, 2], a large research effort is underway. This effort is to develop new forms of NVM capable of replacing Flash [3]. At the forefront of this research is Phase-Change Random Access Memory (PCRAM). Chalcogenide based PCRAM is one of the most promising non-volatile memories for the next generation of portable electronics, due to its excellent scalability, large sensing margin, fast switching speed, and possible multi-bit per cell operation [3]. It is desirable for a phase-change random access memory (PCRAM) device to achieve multiple resistance states in order to find application in analog logic circuits and reconfigurable electronics, as well as in radiation hardened high-density memories. To explore the possibility of achieving multiple resistance states in a PCRAM device, we have performed electrical measurements on devices comprised of at least two layers of chalcogenide material. One of the layers is either SnSe or SnTe and the other layer is either GeTe or Ge_2Se_3. We compare the room temperature operation of the Layered devices to the devices fabricated with single layered Ternary samples consisting of the following compositions: $(Ge_2Se_3)_{97}Sn_3$, $(Ge_2Se_3)_{97}Zn_3$, $(Ge_2Se_3)_{97}Sb_3$, or $(Ge_2Se_3)_{97}In_3$.

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CHAPTER 1: INTRODUCTION

1.1 Introduction and Motivation

Due to an increasing demand for products such as MP3 players, digital cameras, cell phones, and solid state drives for laptop computers, the worldwide average annual growth rate (AAGR) for semiconductor Non-Volatile Memory (NVM) is projected to rise at a rate of 31.8% from 2005 to reach an AAGR of 69.1% in 2010 [1], as shown in Figure 1.1. Among existing semiconductor NVM technologies, the market for Flash has grown rapidly, and in 2005 it comprised almost 90% of the total semiconductor NVM market [1].

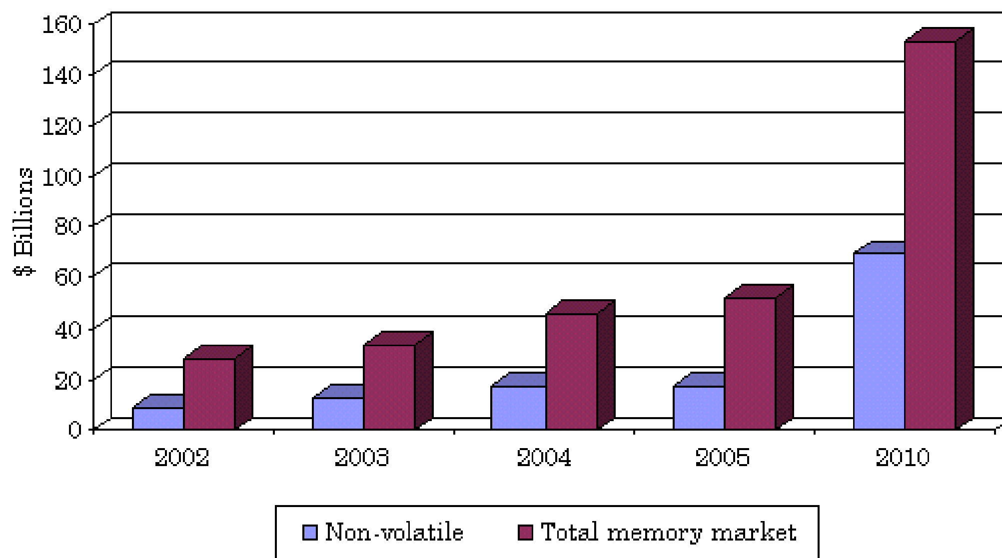


Figure 1.1: Projected growth of Total Memory Market vs Non-Volatile Memory Market [1].

However, with each generation of Flash memory, new difficulties are being encountered as devices continue to be scaled down [2]. These scaling difficulties are

primarily due to high electric fields, required for the program /erase operations and the stringent leakage requirements for long term charge storage [2]. In keeping up with the market demands, a large research effort is underway to develop new forms of NVM capable of replacing Flash.

1.2 Phase-Change Random Access Memory (PCRAM)

Chalcogenide based PCRAM is one of the most promising non-volatile memories for the next generation of portable electronics, due to its excellent scalability, large sensing margin, fast switching speed, and possible multi-bit per cell operation [3].

1.2.1 History

Chalcogenide glasses are a class of materials which contain Sulfur (S), Selenium (Se) and/or Tellurium (Te), or combinations thereof. These materials are attracting much attention due to their potential use in Non-Volatile Memory (NVM) technology, and the high demand for portable media, which use this type of memory [3]. One of the most intriguing phenomena in the conduction characteristic of chalcogenide materials is the threshold switching which was first published in 1968 by Stanford Ovshinsky using a 500 nm thick film composed of Tellurium, Arsenic, Silicon, and Germanium [4]. Ovshinsky reported that certain glasses exhibit a reversible change in resistivity upon a change in the phase of the material [4]. Later, in 1969 Ovshinsky reported a corresponding change in reflectivity that could be induced by laser for optical storage [5], laying the path for future development for applications such as optical data storage devices (CD-RW, DVD-RW) and Phase-Change Random Access Memory (PCRAM) [6].

1.2.2 Operation

PCRAM is a resistance based non-volatile memory, where the state of the memory bit is defined by the resistance of the chalcogenide material [7]; the resistance state depending on the microstructure of the material. A typical cross-section of a $Ge_2Se_2Te_5$ (GST) phase-change device cell is shown in Figure 1.2. Although there are a number of possible geometries for PCRAM cells [8], the standard geometry is the so-called “mushroom” structure shown (amorphous region marked by the * in Figure 1.2, left) [9].

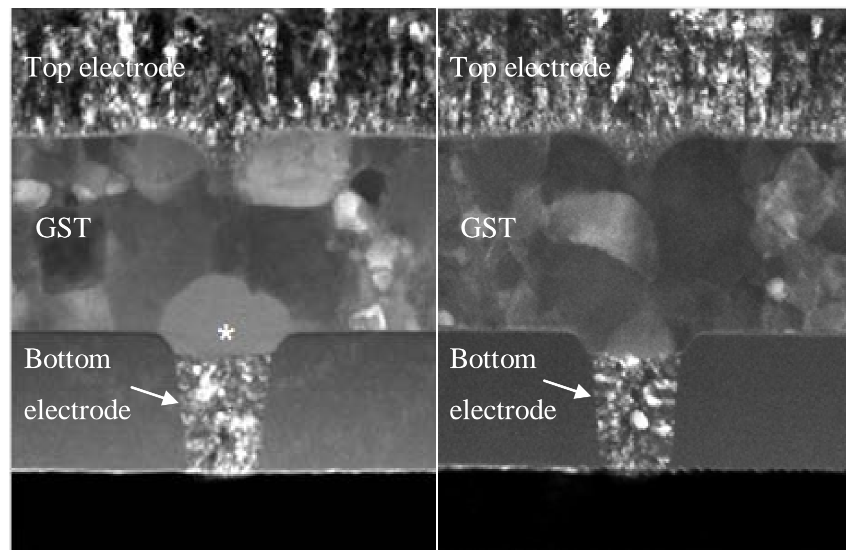


Figure 1.2: Representation of a cross-section for a GST phase change device: Left - after RESET (mushroom structure); Right - after SET. Amorphous GST region marked by * in RESET image (Left image). TEM images courtesy of Micron Technology.

In this geometry the phase-change material is sandwiched between two electrodes: (1) a bottom electrode, - often called a “heater element” with a small contact area, and (2) a top electrode, - which typically has a larger contact area than the bottom electrode [9]. Due to the contact area asymmetry, the current is confined near the bottom

electrode causing the region around the bottom electrode to reach the highest temperature during operation. This region is sometimes referred to as the “active” or “melt” region of the PCRAM cell [9]. The phase-change of the PCRAM device to a highly resistive amorphous chalcogenide material is accomplished when a voltage higher than the threshold voltage is applied across the bit driving a brief, intense current pulse through the device. This raises the temperature of the chalcogenide material above the melting temperature through Joule heating. Once the melting temperature is achieved, the rapidly falling edge of the current pulse quenches the temperature of the material. This places the chalcogenide film in an amorphous (high-resistance/high-reflectivity) state, which is a “RESET” state for the device [7]. The reset operation creates the amorphous dome-shaped region (marked by the * in Figure 1.2, left) with a resistivity several orders of magnitude higher than that of the poly-crystalline region of the device; placing the device in a RESET state. To “SET” the device or return it to a SET state, an extended (longer duration), lower intensity, current pulse is applied to the phase-change material, heating the device above the glass transition temperature but below the melting temperature [7]. Once the material is in this temperature region, the device is cooled more slowly changing the phase of the material to a poly-crystalline (low-resistance/low-reflectivity) state [7]. The final physical structure of the device material is determined by the amplitude and duration of the heating pulse (as shown in Figure 1.3).

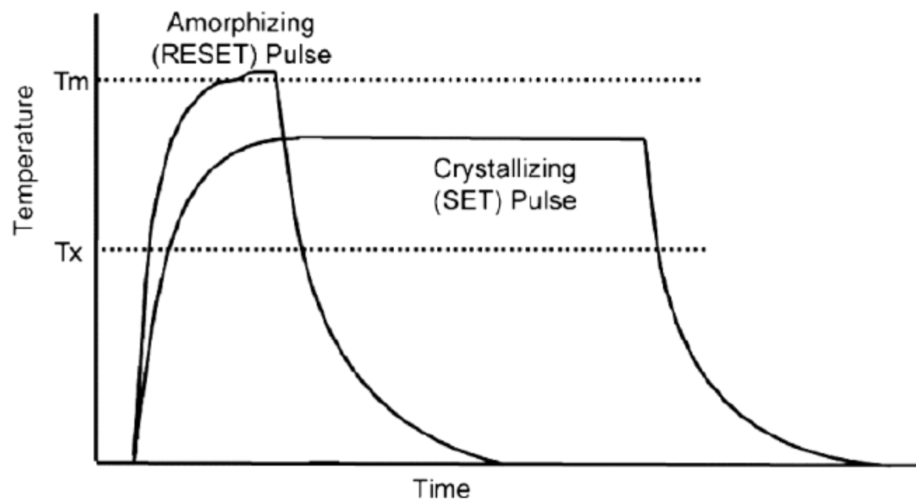


Figure 1.3: Overlay of Temperature vs Time for RESET and SET pulses [10].

During the SET operation, there is a point where the resistance of the phase-change material drops suddenly. This phenomenon takes place at the threshold voltage of the material and is often referred to as the “snap-back” region of the device, due to the shape of the IV trace. A typical IV trace for the snap-back region is shown in Figure 1.4 below.

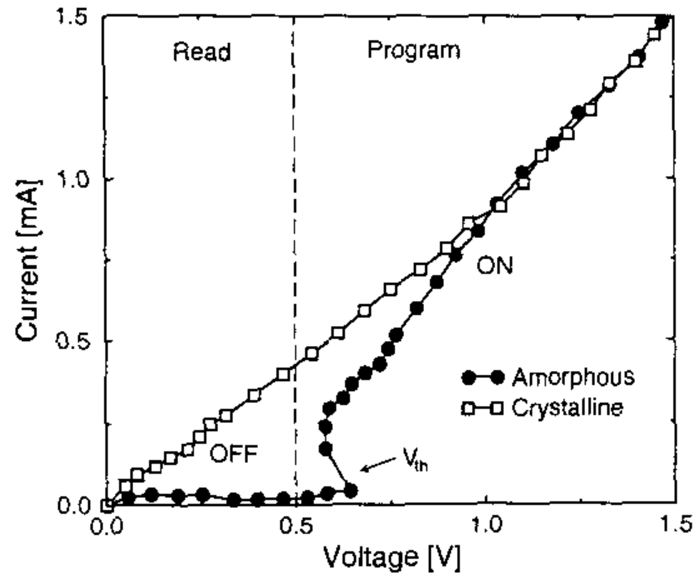


Figure 1.4: Typical IV traces for a phase-change device [11].

Depending on the composition of the chalcogenide material the sudden conductive state can be adjusted, allowing the device to reach the threshold voltage at lower potentials and/or allowing multiple switching states [3]. Switching the material with a lower threshold voltage may allow the device to change phases at a faster rate, from an amorphous state to a polycrystalline phase, increasing the switching speed of the material [3]. Understanding the threshold switching mechanism is an essential task not only in view of the industrial applications, but also in the fundamental study of band structure and transport properties of amorphous semiconductors [3].

1.3 Proposed Improvement

This thesis is a compilation of current-voltage (IV) characteristics and pulse testing performed on alternative phase change materials and device structures, fabricated at Boise State University and Micron Technology. Samples fabricated at Boise State

consist of four separate Ternary chalcogenide materials, based from compositions of $(Ge_2Se_3)_{97}M_3$ where M is one of the following elements: Tin (Sn), Zinc (Zn), Antimony (Sb), and Indium (In). These are referred to as the Ternary samples throughout the remainder of the thesis. The intent for the alternative Ternary materials is to find new forms of possible multi-state memory devices. The Differential Scanning Calorimetry (DSC) measurements discussed in the next chapter (Chapter 2) show multiple crystallization regions on the Ternary samples tested. In this work, electrical characterization of devices comprised of these Ternary materials is performed to determine if the multiple crystallization regions present multiple resistance states. As the multiple crystallization regions are stable in the bulk material, it is possible that these would lead to stable memory states [12].

Layered structures created at Micron Technology, consist of two chalcogenide layers (shown in Figure 1.5) instead of a single chalcogenide alloy layer. There are three separate Layered devices, each one fabricated with a slightly different stack. The Layered materials studied are GeTe/SnTe, Ge_2Se_3/SnTe, and Ge_2Se_3/SnSe, which we will refer to as the Layered structures/devices throughout the remainder of the thesis. The objective of the Layered structures is that by using two chalcogenide layers, one a Ge-chalcogenide (the memory layer), and the other a Sn-chalcogenide (the metal-chalcogenide layer), we hope to improve adhesion between the active switching chalcogenide layer and the top electrode, as well as to reduce the voltages, currents, and switching speeds needed for phase-change memory operation without the need for a complicated physical device structure [7].

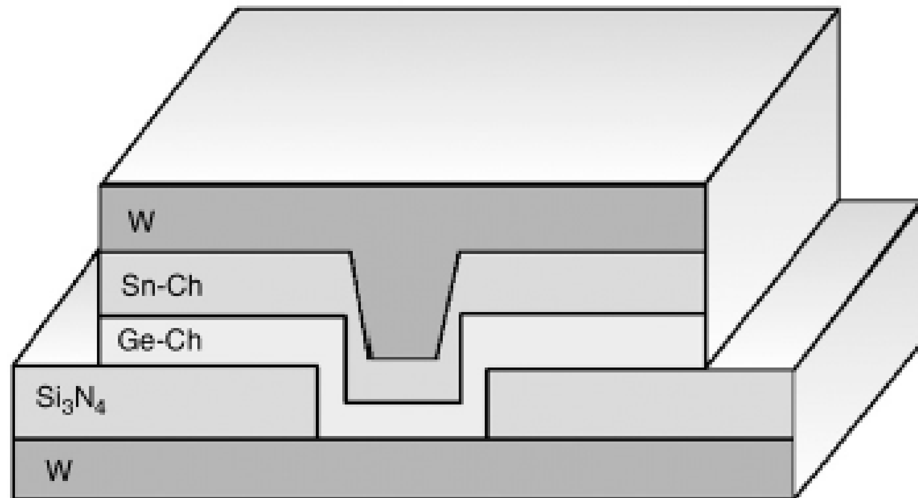


Figure 1.5: Representation of the cross-section for the Layered device [7].

Additional information on the processing of these materials, the layout of the device structures, and benefits of the materials/structures will be provided in Chapters 2 and 3.

1.4 Conclusions

In view of the need for new forms of non-volatile memory and an understanding of PCRAM, we investigate the alternative Ternary materials fabricated at Boise State University and Layered structures fabricated at Micron Technology. In Chapter 2 the discussion begins with the desirable properties of the Ternary and Layered devices. In the following chapter (Chapter 3), the fabrication process is covered as well as proposed future process modifications due to problems that could not be overcome with the present structure. From there, the device performance of the Ternary structures is investigated

(see Chapter 4) and Layered devices (see Chapter 5). This work then concludes with a summary of the benefits of the Ternary and Layered devices as well as future work.

CHAPTER 2: MATERIALS CHARACTERIZATION

2.1 Introduction

In this chapter we present background information on the Ternary materials ($(Ge_2Se_3)_{97}Sn_3$, $(Ge_2Se_3)_{97}Zn_3$, $(Ge_2Se_3)_{97}Sb_3$, $(Ge_2Se_3)_{97}In_3$) and Layered chalcogenide structures (GeTe/SnTe, Ge_2Se_3/SnTe, and Ge_2Se_3/SnSe). We discuss why these materials may be viable candidates for multi-bit storage based upon prior work performed on these structures [7, 12].

2.2 Desirable Properties: Ternary Samples

Traditional methods to achieve multi-state behavior in PCRAM have focused on partial crystallization to achieve multiple states [11, 14], which has proven to be unstable and often unrepeatable [15]. To ensure that a PCRAM material is capable of multi-state behavior, a device must exhibit stable, distinct, non-overlapping, resistance distributions for each resistance state defined for the bit, as illustrated in Figure 2.1 [14]. These resistance states are determined by applying current and/or voltage pulses to the sample to see if more than one resistance drop is present [16, 17]. It should be noted that the number of resistance groups or bits stored in a cell is dependent on the number of crystalline phases available in the chalcogenide material [14].

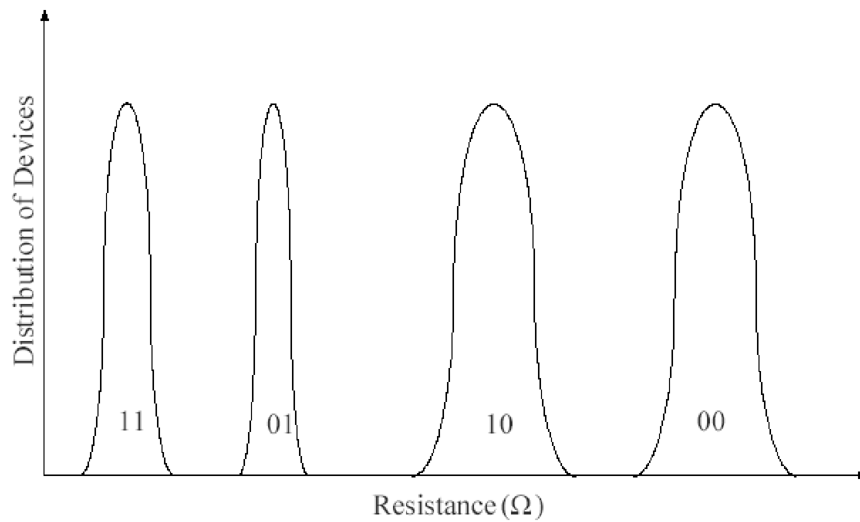


Figure 2.1: Representation of the resistance distribution for a multi-state device [14].

2.2.1 Ternary Samples: Potential for Multi-State Programming

The Ternary structures fabricated at Boise State University were developed with the intent of producing a multi-resistance material with low-power operation and reliability after multiple cycles. Differential Scanning Calorimetry (DSC) traces were collected on the Ternary alloys comprised of a Ge_2Se_3 composition with the addition of 1% to 3% of Sn, Zn, Sb, and In. Different concentrations of Sn, Zn, Sb, and In were tested [7].

To study the phase transitions, DSC measurements were performed on each of the Ternary bulk samples. From the DSC trace, the glass transition, crystallization, and melting temperature were found for each of the Ternary samples. In Figure 2.2, DSC traces are shown for all samples but the antimony-containing sample; the glass transition temperature is marked by the * in the DSC traces. The glass transition temperature is the

temperature where the Ternary samples begin to become viscous [18]. As the temperature increases the amorphous material reaches a state where the molecules may obtain enough freedom of motion to spontaneously arrange themselves into a crystalline form. It is at these crystallization regions that upward peaks are seen in the DSC trace (labeled “A”, “B”, and “C” on the 3% Zn). Finally, with the additional increase in temperature the samples reach the melting temperature of the material (labeled “Tm”), which is seen as a dropping off or declining peak in reference to the heat flow as expected.

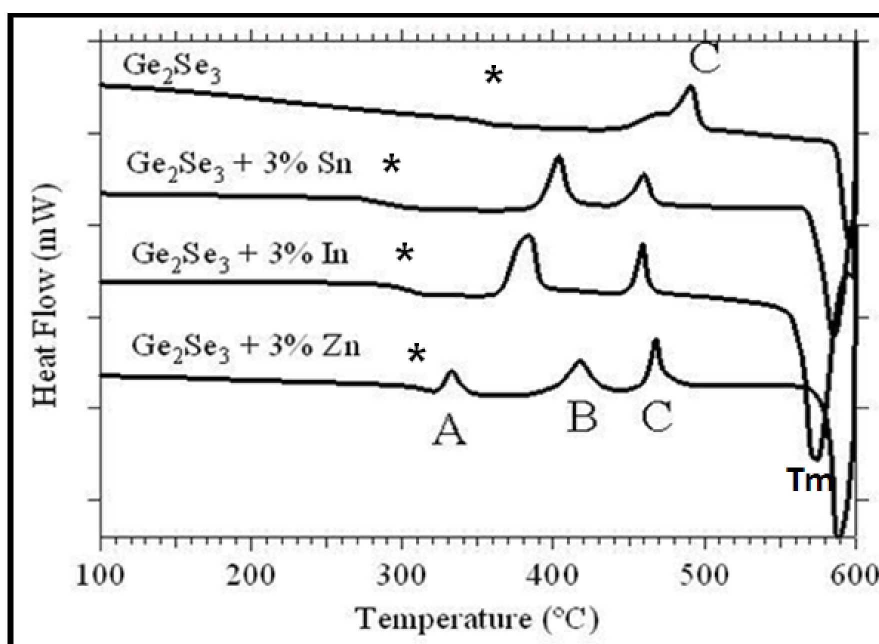


Figure 2.2: Representative DSC trace overlay of the ternary devices [12].

From the overlaid DSC plots in Figure 2.2, it was found that all three Ternary structures containing 3% Sn, In, and Zn show more than one crystallization region with 3% Zn showing three distinct crystallization regions. It is commonly believed that

crystallization peaks that are sharp arise from fast transitions that are less stable than the peaks corresponding to broader, slower transitions [19]. Following this line of reasoning, when reviewing the 3% Zn DSC trace, the peak labeled "A" would most likely be more stable than the peak labeled "C". Moreover, it is possible that the 3% Sn and Zn samples probably have two stable multi-resistance states. As a confirmation of the DSC traces temperature dependent XRD scans were performed finding differing XRD peaks with transitions that matched the DSC traces, confirming the results of the DSC data [20]. Due to the presence of more than one crystallization region for each of the 3% samples, each of the materials is a strong candidate for multi-state programming.

Of note, the 3% Zn sample has an initial crystallization peak at a lower temperature than the other films (see the peak labeled A). Due to the location of the initial peak when compared to the other Ternary films, it is possible that the 3% Zn Ternary device will operate with less power, as it does not need as much heat before reaching the initial crystallization region. More detail on the stability of the crystallization regions will be given in Chapter 4.

2.3 Desirable Properties of Layered Materials

In designing a phase-change device, two major factors must be considered. These factors are reliability and low-power operation [10]. To accomplish this, the material should retain its initial properties even after repeated SET and RESET cycles [10]. This is extremely difficult to accomplish. Generally, the phase transition process does not take place uniformly inside the phase change memory cell [16]. This is expected as a result of the temperature gradient inside the cell during programming. In an attempt to improve the

reliability of the phase-change device and reduce the power consumption, Layered structures were fabricated to create a more stable temperature gradient, improve the adhesion to the electrodes during volume contraction/expansion, and reduce the contact potential [7].

2.3.1 Layered Devices: Potential for Multi-State Programming

In a previously published work on the Layered structures fabricated at Micron Technology, it was shown that chalcogenide devices fabricated with three types of stack structures, GeTe/SnTe, Ge_2Se_3/SnTe, and Ge_2Se_3/SnSe (Figure. 1.5), exhibit consistent electronic switching [7]. For the GeTe/SnTe stack structure it was reported that with a positive potential applied on the top electrode adjacent to the SeTe layer, at least two snap-back regions were observed on multiple bits as seen in Figure 2.3; indicating potential multi-bit behavior for the device [7].

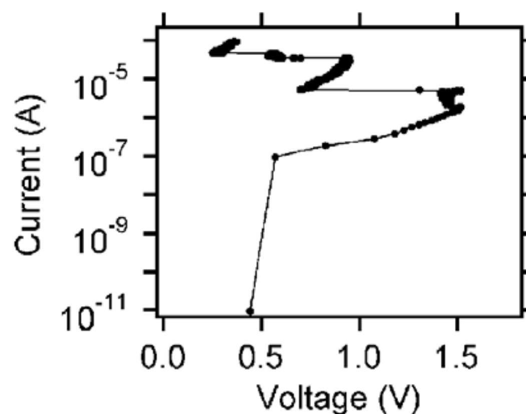


Figure 2.3: Representative IV curve for the GeTe/SnTe layered device [7].

We observed phase-change memory switching in all of the devices tested even though Ge_2Se_3 does not normally exhibit a phase-change response [21]. We determined that the phase-change switching was due to the movement of either Sn ions or Te ions into the Ge-containing layer, dependent upon the polarity of the potential applied to the electrode adjacent to the SnTe or SnSe layer [7]. Further detail on the electrical characterization and switching mechanism will be discussed in Chapter 5.

2.4 Conclusion

In Chapter 2 we discussed the desirable properties of the Ternary and Layered devices. From the Ternary DSC data it was concluded that each of the materials were strong candidates for multi-state programming due to the number of crystallization peaks for each material. It was also determined that that the 3% Sn and Zn samples would have a better chance of stable multi-resistance states than the 3% In sample.

For the Layered samples, structures were created with the expectation to improve the device reliability while reducing the power consumption. Previous work was performed and found the GeTe/SnTe stack structure to have two observable snap-back regions; indicating multi-bit behavior for the device. Phase-change switching was observed on all of the Layered samples listed with the GeTe/SnTe structure showing the most promise for multi-state programming [7].

CHAPTER 3: DEVICE FABRICATION

3.1 Introduction

In Chapter 2 we covered the benefits of both the Ternary and Layered devices being tested. This chapter covers the device fabrication methodology. It should be noted that the fabrication of the Ternary and Layered devices were performed at separate times and places. The Ternary structures were fabricated at Boise State University by a graduate student, Morgan Davis and newly fabricated Ternary devices (discussed in Chapter 4) were created by postdoctoral researcher Pulok Pattanayak; both working under the supervision of Dr. Campbell. The Layered structures were designed at Boise State University but were fabricated at Micron Technology in Boise, Idaho in 2005. The process details for the device fabrication have been collected and complied in the sections below.

3.2 General Considerations

We begin this chapter discussing the considerations that went into developing a process for making the Ternary and Layered structured memory cells. Initial considerations were made on the availability of equipment in our research lab at Boise State University and at Micron Technology. Many process decisions were made based on the availability of tools and materials. This was taken into account to limit the amount of process variation that would be seen for better test results. Even with these measures, post device fabrication, there was found to be center middle and edge variation on the Boise State and Micron samples.

3.2.1 Electrodes

The Ternary and Layered devices tested, listed in Table I, consist of one or two chalcogenide layers between two metal electrodes. In review of the literature on phase change memory cells, there is very little mention of reasoning behind materials chosen for electrodes. By far the most common material chosen for the heater element is TiN because of its relatively low thermal conductivity and acceptable electrical conductivity [9].

Table 3.1: Ternary and Layered devices tested

Sample	Bottom Electrode	Layer 1	Layer 2	Top Electrode
1	W (via)	GeTe	SnTe	W
2	W (via)	Ge_2Se_3	SnTe	W
3	W (via)	Ge_2Se_3	SnSe	W
4	W (via)	$(Ge_2Se_3)_{97}Sn_3$	*None*	W
5	W (via)	$(Ge_2Se_3)_{97}Zn_3$	*None*	W
6	W (via)	$(Ge_2Se_3)_{97}Sb_3$	*None*	W
7	W (via)	$(Ge_2Se_3)_{97}In_3$	*None*	W

Research at Hitachi, however, has lead to the use of Tungsten (W) electrodes, arguing that the lattice match between the Tungsten (W) and phase-change material structures reduce the current needed for programming the phase change material [9, 22, 23]. Thus, for these materials, Tungsten (W) was used for the bottom and top electrodes. The bottom electrode, which is always adjacent to the Ge-chalcogenide layer (Layer 1), consists of a via configuration (*i.e.* a hole through nitride to the W electrode). For the top electrode Tungsten (W) was once again used. The via diameters for the Layered devices were 0.25 μm, whereas the Boise State samples had via diameters ranging between 1 to 2 μm, thus defining the device diameter.

3.3 Device Process Structure

TEM cross-sections of the fabricated structures were collected as a result of some of the process variations found from the electrical testes. Further details will be given on this in Chapters 4 and 5.

3.3.1 Ternary Process Structure

In Figure 3.1 we have a cross-sectional representation of the Ternary device. The device structure consists of a via through a 600 Å silicon nitride (Si_3N_4) layer to a 600 Å common Tungsten (W) bottom electrode, deposited on a 250 Å Chromium (Cr) layer with a 100 mm p-type Si wafer substrate [24]. The wafers were purchased with these specific layers due to the deposition of the silicon nitride (Si_3N_4) layer not being possible at Boise State University at this time. Prior to the deposition of the Ternary chalcogenide layer the wafers received an Ar^+ sputter etch to remove residual unwanted material and any oxide layer that may have formed on the Tungsten (W) electrode. The $(Ge_2Se_3)_{97}Sn_3$, $(Ge_2Se_3)_{97}Zn_3$, $(Ge_2Se_3)_{97}Sb_3$, $(Ge_2Se_3)_{97}In_3$ Ternary films were prepared by thermal evaporation of the alloys using a CHA Industries SE-600-RAP thermal evaporator equipped with three 100 mm wafer holders with planetary rotation [24]. The rate of deposition was monitored using an Inficon IC6000 with a single 6 MHz crystal sensor [24]. The base pressure prior to all evaporations was 2.0 x 10^{-6} Torr [24]. All samples were evaporated from ceramic crucibles [24].

Figure 3.1: Representation of the cross-section for the Ternary devices [24].

3.3.2 Layered Process Structure

Figure 1.5 shows a cross-sectional representation of the Layered device. The device structure consists of a via through a nitride layer to a Tungsten (W) bottom electrode deposited on 200 mm p-type Si wafers [7]. The chalcogenide material layers were deposited with the Ge-chalcogenide layer first, followed by the Sn-chalcogenide layer. Prior to the deposition of the first chalcogenide layer. The wafers received an Ar^+ sputter-etch to remove residual material and any oxide layer that may have formed on the W electrode [7]. The Ge_2Se_3 layer was deposited by sputtering Ge_2Se_3 powder pressed into a target [7]. The GeTe, SnTe, and SnSe layeres were prepared by thermal evaporation of GeTe, SnTe, and SnSe (all from Alfa Aesar, 99.999% purity) using a CHA Industries SE-600-RAP thermal evaporator equipped with three 200 mm wafer

holders with planetary rotation [7]. The rate of material deposition was monitored using an Inficon IC 6000 with a single crystal sensor head. The base system pressure was 1 x 10^{-7} Torr prior to evaporation [7].

Using the planetary rotator, evaporated films were deposited on two types of wafers simultaneously in each experiment: (1) A film characterization wafer consisting of a p-type Si wafer substrate with the layers 350Å W/800Å Si_3N_4 and (2) two wafers processed for device fabrication consisting of vias etched through a Si_3N_4 layer to a W electrode for bottom electrode contact [7].

The film characterization wafer present in each evaporation step was used to characterize the actual thin-film material stoichiometry post evaporation since thermally evaporated films can have a stoichiometry different than the starting material [7]. The evaporation chamber was opened to the ambient atmosphere following the GeTe film depositions in order to expose the GeTe films to similar ambient atmospheric conditions as the sputtered Ge_2Se_3 films which had to get exposed to the atmosphere during transfer from the sputtering tool to the evaporator for the Sn-chalcogenide film deposition [7]. After the evaporation step(s) were complete, the device fabrication processing continued through top electrode deposition (350Å sputtered W), photo steps, and dry etch to form fully functional devices consisting of a bottom electrode, chalcogenide material layers, and top electrode [7]. Dry etch was performed by ion-milling with a Veeco ion-mill containing a quadrupole mass spectrometer for end-point detection [7].

The GeTe and Ge_2Se_3 films were amorphous as deposited with no observable XRD peaks [7]. The SnTe and SnSe films were polycrystalline, as indicated by their XRD spectra seen in Figure 3.2.

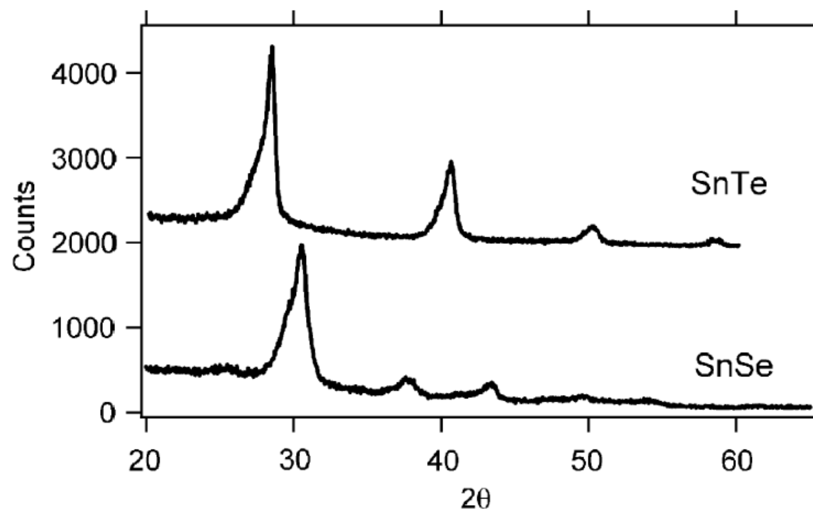


Figure 3.2: XRD spectra of SnTe and SnSe evaporated films [7].

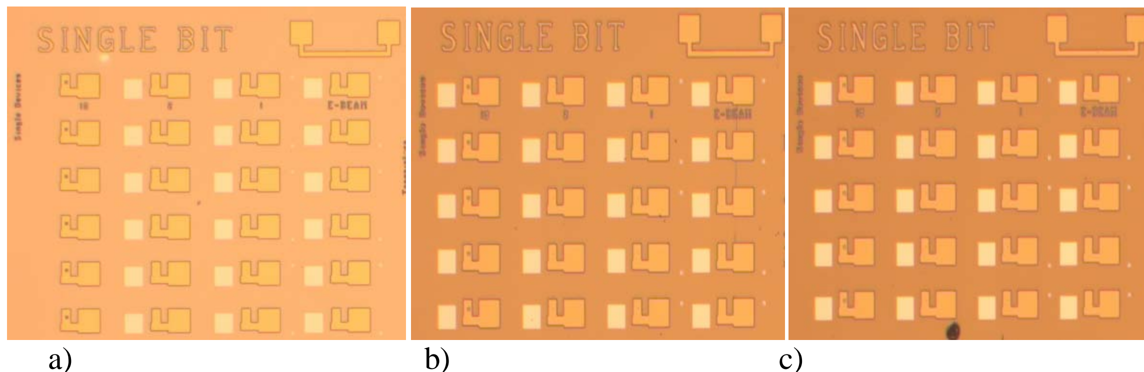
Due to the nature of the evaporation process, and pressure of the evaporation chamber prior to film deposition (1E-7 Torr), oxygen is most likely incorporated into the SnTe, SnSe, and GeTe films during deposition [7]. ICP data was collected on the samples, which provided film stoichiometry (excluding oxygen) with an accuracy of ± 0.8%. The actual thin film compositions measured with ICP are listed in Table 3.2.

Table 3.2: ICP Data

Device stack	Layer 1 composition	Layer 2 composition
GeTe/SnTe	$Ge_{47}Te_{53}$	$Sn_{49}Te_{51}$
Ge_2Se_3/SnTe	$Ge_{40}Se_{60}$	$Sn_{49}Te_{51}$
Ge_2Se_3/SnSe	$Ge_{40}Se_{60}$	$Sn_{49}Se_{51}$

3.4 Problems and Future Process Modifications

Post processing it was found that there was a large variation in color between the center, middle, and edge of the wafer on the Ternary samples as seen in Figure 3.3.



a) b) c)

Figure 3.3: Magnified Images of ternary device, showing color variation across wafer: edge (a); middle (b); center (c).

This variation is most likely due to the deposition process and/or the Dry Etch to create the via in the Si_3N_4 and Tungsten (W) film. Due to the color variation throughout each of the wafers, electrical measurements were taken at certain locations to ensure that the material being tested was of a similar state. From the electrical measurements center-middle-edge variation and bit-to-bit variation was found on both the Ternary and Layered devices. For the Layered structures the devices were setup as stand-alone memory cells; each one having an isolated bottom electrode.

3.5 Conclusions

This chapter described the process that could fabricate phase-change memory cells given the resources available at Boise State University and Micron Technology. A discussion was provided of the unforeseen problems with this initial process, such as the common bottom electrode used in the fabrication process for the Ternary devices and the

process variation between the center, middle, and edge of the wafer on both the Layered and Ternary devices. In the next two chapters, the performance of the Ternary memory cell (Chapter 4) and the Layered structures (Chapter 5) is described.

CHAPTER 4: TERNARY DEVICE CHARACTERIZATION

4.1 Introduction

The Ternary materials $Ge_xSe_ySn_z$, $Ge_xSe_yZn_z$, $Ge_xSe_yIn_z$, and $Ge_xSe_ySb_z$ are good candidates for making multi-state phase-change materials based on the multiple crystallization regions present in these samples as determined through the DSC measurements discussed in Chapter 2. Additionally, the presence of multiple snap-back regions in the IV traces for the Layered devices (Chapter 2) may be indicative of multiple crystalline phases. This chapter focuses on the electrical characterization of devices fabricated with these Ternary materials, beginning with a physical description of the devices as fabricated, followed by electrical characterization results.

4.1.1 Device Description

A TEM image of a cross-section of the $(Ge_2Se_3)_{97}Sn_3$ Ternary device, taken at the location of the device via, is shown in Figures 4.1 and 4.2. From the TEM image, the film thicknesses and width of the via were measured. The TEM image was taken halfway between the wafer center and the edge (referred to as the middle).

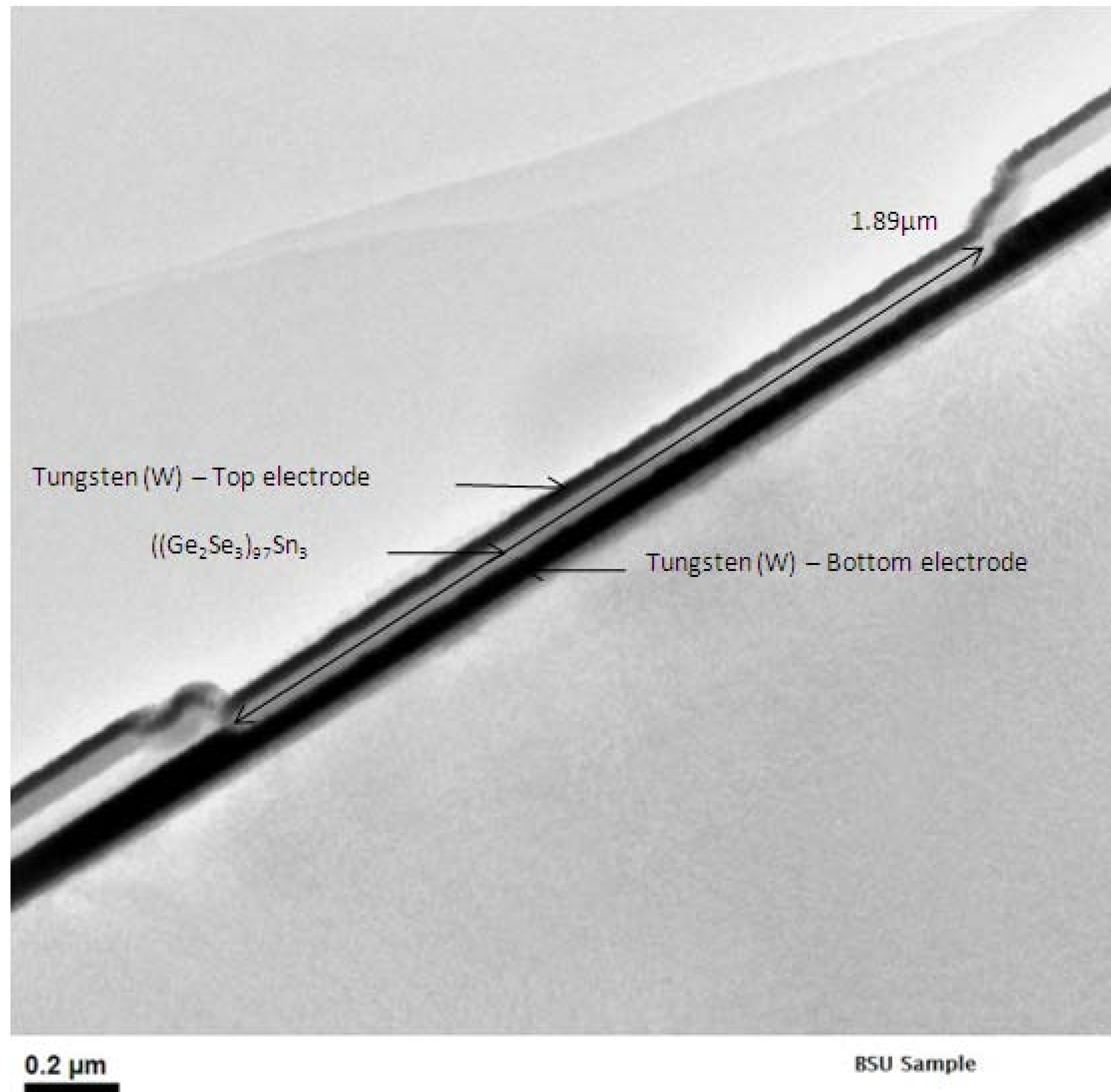


Figure 4.1: Ternary TEM image of $(Ge_2Se_3)_{97}Sn_3$ via; courtesy of Micron Technology.

In Figures 4.1 and 4.2, we can see the bottom and top W electrodes, the Si_3N_4, and amorphous $(Ge_2Se_3)_{97}Sn_3$ film; the $(Ge_2Se_3)_{97}Sn_3$ being sandwiched between the two metal films within the via. Below the bottom electrode there is an additional Chromium layer (Cr) being used to help reduce the film stress that would normally exist between the silicon substrate and the bottom W electrode. As seen in Figure 4.1, the bottom W

electrode is used as a common electrode, as was also shown in the representative cross-section in Figure 3.1.

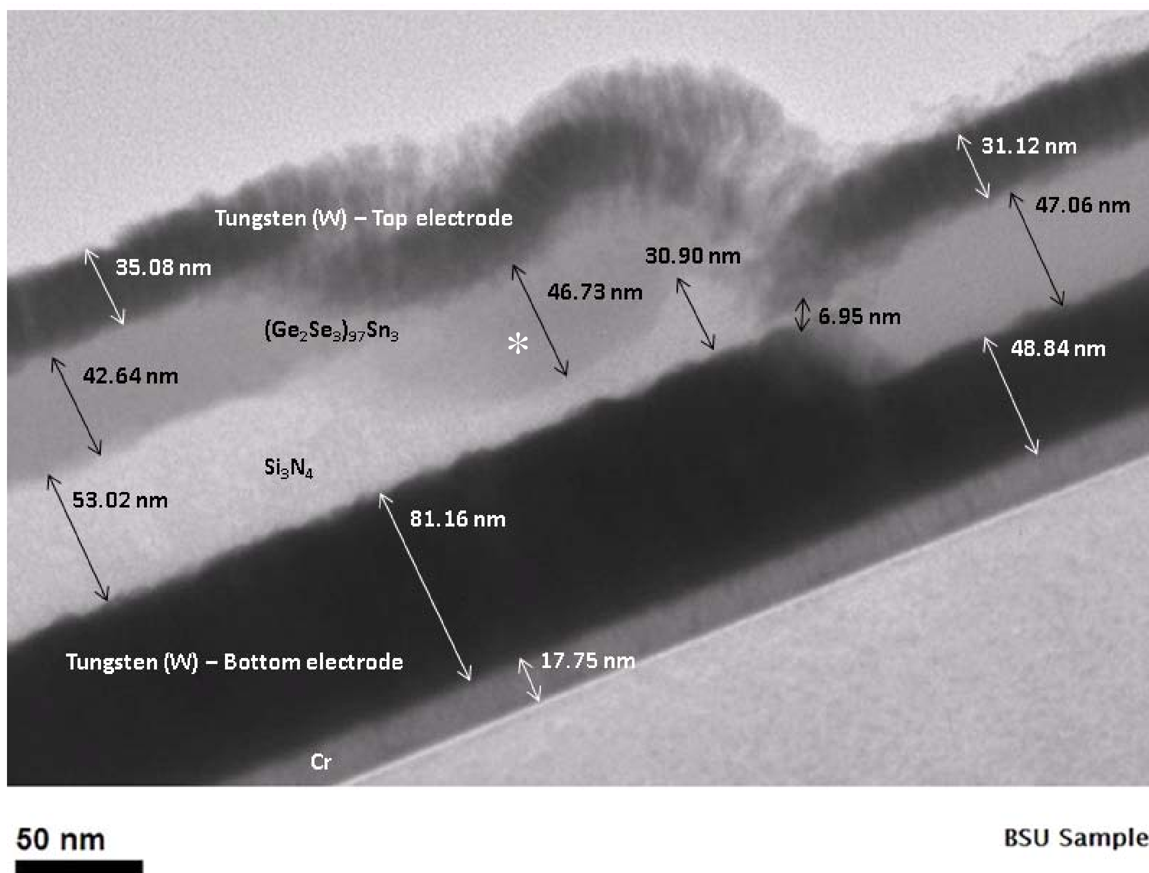


Figure 4.2: TEM image of Ternary $(Ge_2Se_3)_{97}Sn_3$ device at edge of via; courtesy of Micron Technology.

In Figure 4.2, it appears that a region in the nitride adjacent to the via was etched during the via etch process (see region to the left of the via marked by *). This could be due to sidelobing (i.e. beam pattern) due to the photo dose used during the via pattern-process, creating an unintentional region prone to etching. The Si_3N_4 layer above the bottom W electrode has been over-etched when forming the via of the Ternary device.

Due to the recess of the Si_3N_4 layer over the bottom W electrode, poor step coverage of the thermally evaporated Ternary layer was found. As seen in Figure 4.2, the W bottom and top electrode appears to be almost touching at the edge of the via. Furthermore, the thinner Ternary film present at the side wall of the via, when compared to the bottom of the via for the Ternary film, would likely cause this region of the via to melt more rapidly when current is forced through the device [15], thus preferentially switching a portion of the material near the sidewalls of the device.

4.2 Electrical Testing

This section will cover the electrical experimental setup that we used to program and characterize the phase-change memory devices, followed by the electrical characterization of the Ternary structures. The electrical characterization is performed through quasi-static (DC) IV traces and voltage pulse testing to identify possible multi-resistance states.

4.2.1 Electrical Test Setup

In general, the basic electrical testing for a phase-change memory cell can be performed using a pulse generator (for programming the device) and an oscilloscope to determine the voltage drop across the device (through the use of a series load resistor) [16]. There are, however, issues with using this simple setup for resistance variable devices, such as the phase-change device. The most important issue is that the series load resistor value needs to be closely matched to the phase-change material resistance values in the SET and RESET states, otherwise the results can become unreliable, due to

impedance mismatch between the device and the load resistor. This impedance mismatch may create a reflected voltage signal that can reprogram the device, or at the very least allow an unwanted signal with unknown amplitude and pulse width to be applied to the device via the reflected signal. This prevents an accurate measurement of the programming conditions of the device, and can in itself lead to misinformation concerning the device variation and programming conditions. Only if the device is 'over-programmed' to a very low resistance consistently will the electrical responses appear to be stable; however, this degrades the device lifetime and prevents an exploration of device electrical characteristics and cycling response [10, 25].

To avoid the use of a load resistor, room temperature electrical measurements were made using an Agilent B1500A parameter analyzer (Figure 4.3), equipped with a B1530A Waveform Generator/Fast Measurement Unit (WGFMU) module and, B1511A Source Monitor Units (SMU) module (for DC IV traces) connected to two external Remote Sense/Switch Units (RSU).

Figure 4.3: Agilent B1500A with RSU units displayed. The Source Monitor Units (1) and B1530A WGFMU (2) are accessed through a panel at the back of the B1500A.

The B1530A WGFMU is a self-contained module offering the combination of arbitrary linear waveform generation with synchronized fast current or voltage measurements. Each channel has built-in circuitry to impedance match during the measurement to prevent reflection-induced waveform measurement disturbances. When performing the pulse SET/RESET measurements described in Section 4.3.1, a single B1530A WGFMU (in connection with an RSU and the DC probe) is used to force the voltage pulse and measure the applied voltage at the top electrode, while the second WGFMU measures the current exiting from the bottom electrode. Due to the current flowing from the top electrode into the second WGFMU at the bottom electrode, the polarity of the measured current is opposite that of the applied voltage [26] as shown in all the pulse test figures in Section 4.3.2.

Micromanipulator probes with W coaxial probe tips (Micromanipulator size 1.5 μm) were used to connect to the top and bottom electrodes of the devices tested. The

shields of the Micromanipulator probes were shorted together to establish a current return path [26]. The probe station used was a Micromanipulator 6200 microprobe station (Figure 4.4).

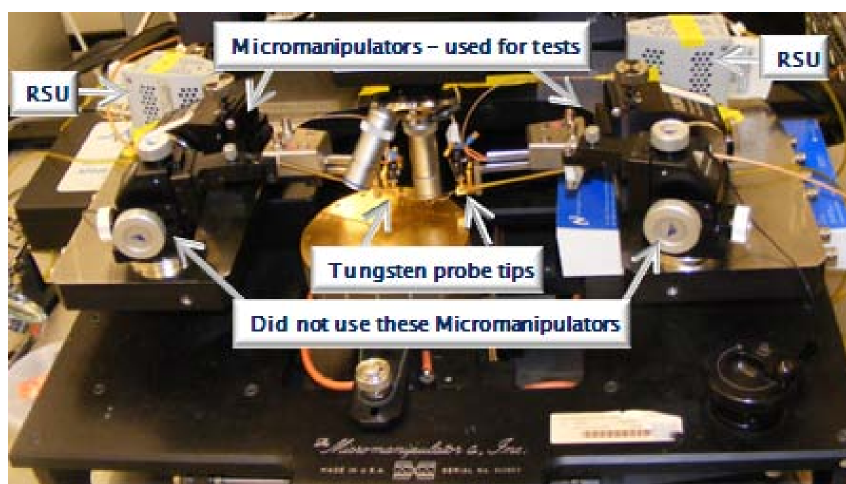


Figure 4.4: Micromanipulator 6200 microprobe station used for electrical characterization.

The RSUs were connected between the B1500A parameter analyzer's SMUs and the DC probes. The DC sweeps were carried out with the SMU in contact with the top electrode of the device, in current-force mode, thus forcing the current through the device while the voltage was monitored. The second SMU was used as a common ground.

4.2.2 DC Electrical Characterization

Standard DC current sweep tests were performed by sweeping the current to either 100 μA or 1 mA with step increments that varied depending upon the maximum current setting (due to limitations in the number of points allowed during a measurement). This was done to determine the resolution needed to capture the threshold

voltage of the device as well as the possible multiple snap-back regions of the Ternary structures.

4.2.3 Current – Voltage Characteristics

Using the electrical test setup defined in Section 4.2.1, we generated the DC IV measurements shown in Figure 4.5 on the Ternary samples. The IV traces shown in Figures 4.5 are representations of standard IV traces taken from each of the Ternary devices. Traces were collected by forcing current through a virgin bit in order to place the bit in a SET state. These traces show the case of a 1 mA maximum forced current (Figure 4.5, left) and 100 μA maximum current (Figure 4.5, right). Notice that the higher resolution seen in the 100 μA maximum current data (Figure 4.5, right) allows better observation of the snap-back region of each device type. The snap-back region observed in Figure 4.5 corresponds to the Negative Differential Conductance (NDC) switching phenomenon [16] introduced in Chapter 1.

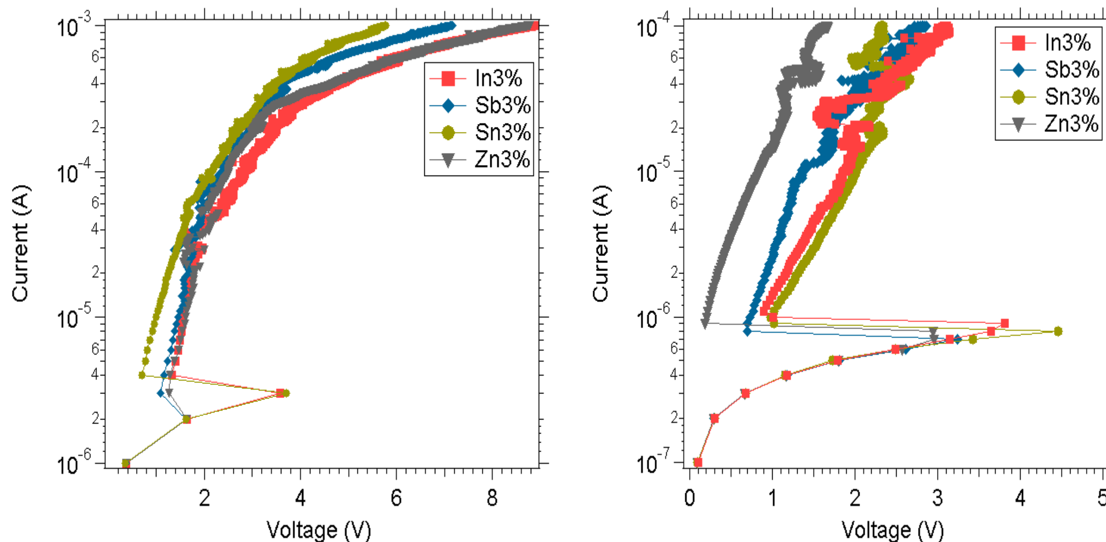


Figure 4.5: Representative IV traces for the Ternary devices with a positive potential applied to the top electrode, showing the threshold voltage variation with lower resolution: Left – 1 mA current sweep with 1 µA increments; Right – 100 µA current sweep with 100 nA increments.

As shown in Figures 4.5, only one snap-back region is apparent on each of the Ternary samples. As discussed in Chapter 2, multiple snap-back regions were expected in the IV traces of the Ternary materials due to the presence of more than one crystallization region in the DSC plots on each of the samples. One explanation for only one apparent snap-back region is due to the resolution of the current sweep applied; the current step size increments may be too large to accurately capture threshold shifts. As one can see in Figure 4.5, as the current sweep is reduced from 1 mA to 100 µA and the resolution is increased, a large change in the measured threshold voltage and current of the device is observed. This will be discussed in further detail in Section 4.2.4.

Another explanation for the lack of observable snap-back is that the change in resistance between crystalline regions may be minor. A minor change would not result in a drastic decrease in potential, which would correspond to an observable snap-back.

Table 4.1 shows the threshold voltage, threshold current, and SET resistances for the Ternary devices programmed with 1 mA and 100 µA of current.

Table 4.1: Typical programmed (SET) resistances and threshold voltages for the Ternary devices programmed with 1 mA and 100 µA of current. Of note, due to the lack of current resolution in the 1 mA sweeps, the threshold voltage and current are not listed.

Device:	SET Resistance (Ω)	Threshold voltage (V)	Threshold current (µA)
Ternary (BSU)	*(100 µA /1 mA)*	*(100 µA /1 mA)*	*(100 µA /1 mA)*
$(Ge_2Se_3)_{97}Sn_3$	$2 \times 10^4/6 \times 10^3$	~4.5/-	~0.9/-
$(Ge_2Se_3)_{97}Zn_3$	$2 \times 10^4/\sim 7 \times 10^3$	~3.0/-	~0.8/-
$(Ge_2Se_3)_{97}Sb_3$	$3 \times 10^4/9 \times 10^3$	~3.3/-	~0.7/-
$(Ge_2Se_3)_{97}In_3$	$3 \times 10^4/9 \times 10^3$	~3.8/-	~1.0/-

The 1 mA and 100 µA measurements have different current resolutions: 1 µA for the 1 mA case, and 100 nA for the 100 µA case. Given the difference in resolution, the threshold current and voltage values between the two current limit cases are not comparable due to the lack of resolution in the 1 mA case. Due to the low resolution, the threshold voltage/current are not considered valid for the 1 mA case and were not added to the tables below. Of importance in the data is the difference in resistance for the 1 mA versus 100 µA programming currents cases. There is almost an order of magnitude difference between the resistance states in each case. It is unknown whether this is due to partial crystallization at the 100 µA programming current, or if it is due to differing crystalline phases for each programming current. The different crystalline phases could

arise due to the differences in temperature of the device under 1 mA (hotter) versus 100 µA (cooler).

4.2.4 Measurement Current Resolution Effects

The effects of using higher resolution during current sweeping of the device was investigated by using various current limits and step increments. It was anticipated that the devices would potentially heat at lower voltages and current if the current was applied to the device longer, as is the case when the measurement resolution is high, due to the duration of the current increments being the same. Figures 4.6 and 4.7 show IV curves measured by forcing current through the devices from 100 nA to 100 µA and from 10 nA to 10 µA, with respective current step increments of 100 nA and10 nA, while measuring the voltage across the device.

Applying a positive potential to the top electrode the threshold switching or snap-back region of each material was found to deviate slightly from one bit to the next. Multiple bits were tested by applying a positive potential to the top electrode as seen in Figures 4.6 and 4.7.

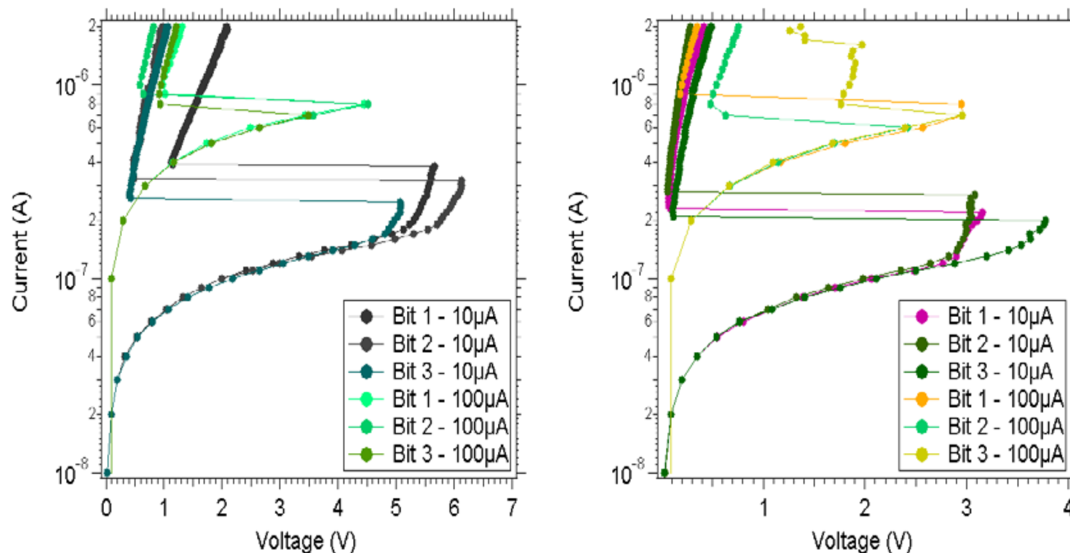


Figure 4.6: IV traces with a positive potential applied to the top electrode, showing bit-to-bit variation: Left - $(Ge_2Se_3)_{97}Sn_3$ device; Right - $(Ge_2Se_3)_{97}Zn_3$ device.

In the traces, a matching increase in current is seen in all of the bits up to the snap-back voltage. Moreover, one can see, by varying the step increments from 10 nA to 100 nA (for the respective 10 µA and 100 µA sweeps), a drastic change in the threshold voltage and location of the snap-back in reference to the current. This shift in the threshold voltage and threshold current was found on all the Ternary samples. One explanation for this shift is due to the rate at which the material is being heated (Joule heating) due to the dwell time at each current value. The higher resolution current increments cause the voltage to be applied for a longer period of time at potentials below the threshold voltage potential.

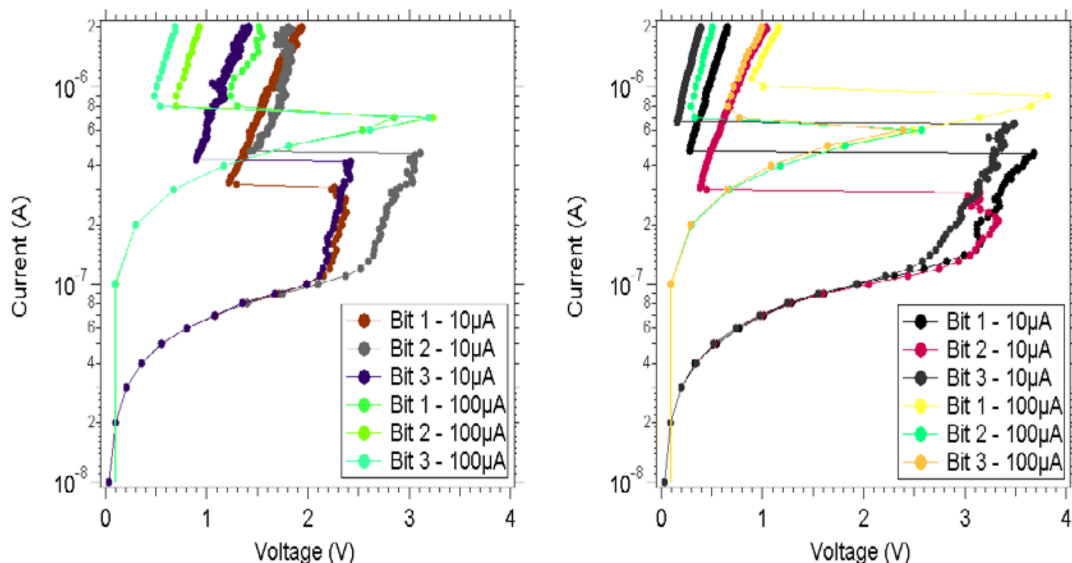


Figure 4.7: IV traces with a positive potential applied to the top electrode, showing bit-to-bit variation: Left - $(Ge_2Se_3)_{97}Sb_3$ device; Right - $(Ge_2Se_3)_{97}In_3$ device.

As seen in Figures 4.6 and 4.7, a slight variation in the threshold current and voltage were found when comparing the potential used on the top electrode of the Ternary devices. These variations are possibly due to the amorphous nature of the material (disorder giving each bit a slightly different material structure), or difference in film impurities during deposition. Table 4.2 is a numerical representation of the comparisons between the 10 µA, 100 µA, and 1 mA threshold voltage / current values, taken from Figures 4.5, 4.6, and 4.7.

Table 4.2: Typical threshold voltages/currents and SET resistances for devices programmed with 10 µA, 100 µA, and 1 mA of current.

Device:	SET Resistance (Ω)	Threshold voltage (V)	Threshold current (µA)
Ternary (BSU)	*(10 µA/ 100 µA/1 mA)*	*(10 µA /100 µA/1 mA)*	*(10 µA /100 µA/1 mA)*
$(Ge_2Se_3)_{97}Sn_3$	$2 \times 10^5/2 \times 10^4/6 \times 10^3$	~6.0 /~4.5 /-	~0.4/~0.9/-
$(Ge_2Se_3)_{97}Zn_3$	$1 \times 10^5/2 \times 10^4/{\sim}7 \times 10^3$	~3.8 /~3.0 /-	~0.2/~0.8/-
$(Ge_2Se_3)_{97}Sb_3$	$1 \times 10^5/3 \times 10^4/9 \times 10^3$	~3.2 /~3.3 /-	~0.4/~0.7/-
$(Ge_2Se_3)_{97}In_3$	$1 \times 10^5/3 \times 10^4/9 \times 10^3$	~3.7 /~3.8 /-	~0.5/~1.0/-

To observe variations in the Ternary film due to possible concentration differences of the 3% Zn, In, Sn, and Sb near the bottom electrode, when compared to the top, IV measurements were carried out with a negative potential applied to the top electrode. The current sweeps were performed by forcing current through the Ternary devices from 100 nA to 100 µA, while measuring the voltage across the devices, this time with a negative potential applied to the top electrode as seen in Figures 4.8 and 4.9. A numerical representation of the SET resistance, threshold voltage, and threshold current measured from the current sweeps, with the positive (V+) and negative (V-) potentials applied, are given in Table 4.3.

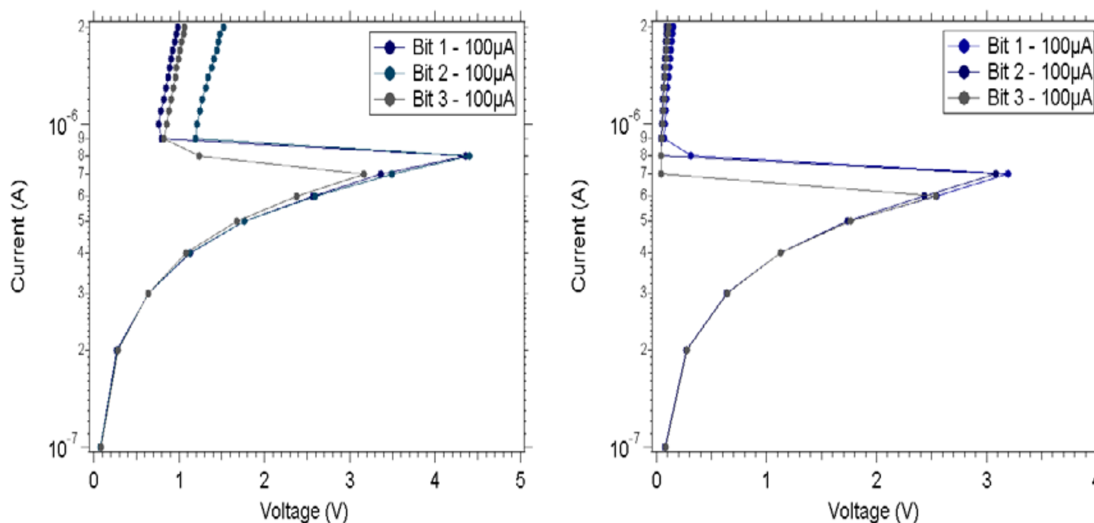


Figure 4.8: IV traces with a negative potential applied to the top electrode, showing bit-to-bit variation: Left - $(Ge_2Se_3)_{97}Sn_3$ device; Right - $(Ge_2Se_3)_{97}Zn_3$ device.

As seen in Figures 4.8 and 4.9, variations in threshold voltage of ~1 V can be seen when applying a negative potential across the device. This was also seen when applying a positive potential on all Ternary samples with the exception of $(Ge_2Se_3)_{97}Sb_3$, which was found to have a stable snap-back when a 100 μA current sweep was performed. However, when comparing the threshold voltage a difference of 0.9 V was found when the potential on the top electrode was changed for the $(Ge_2Se_3)_{97}Sb_3$ device. Of note, the stable snap-back of the $(Ge_2Se_3)_{97}Sb_3$ material was not found when performing the 10 μA current sweeps with a positive potential applied to the top electrode (Figure 4.9). One explanation for the observed difference is the possibility of heating the material at lower potentials during the higher resolution measurements.

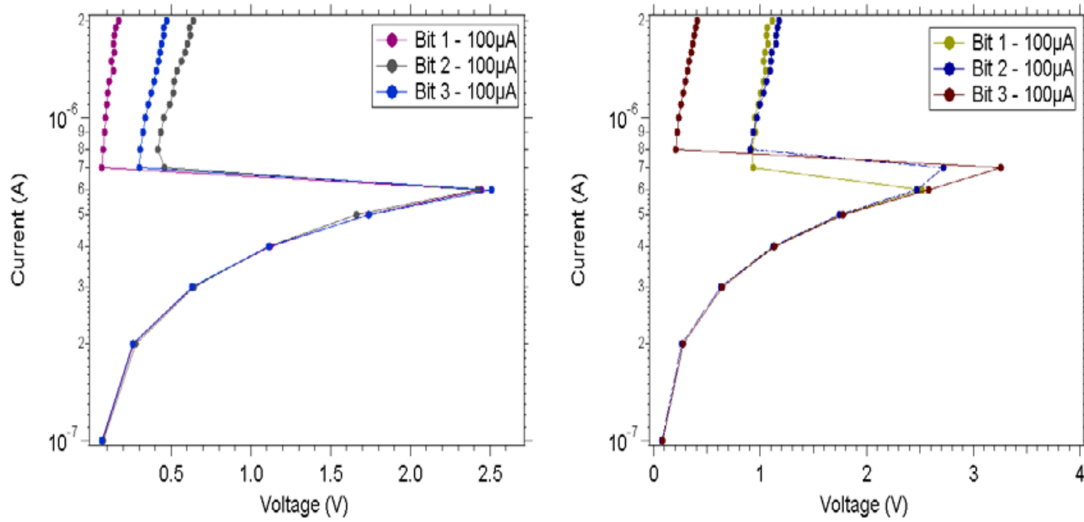


Figure 4.9: IV traces with a negative potential applied to the top electrode, showing bit-to-bit variation: Left - $(Ge_2Se_3)_{97}Sb_3$ device; Right - $(Ge_2Se_3)_{97}In_3$ device.

Table 4.3 provides the SET resistance, threshold voltage, and current at the threshold voltage snap-back taken from the measurement data shown in Figure 4.6 through 4.9.

Table 4.3: Typical threshold voltages/currents programmed with 100 µA of current, with opposite potentials applied to the top electrode positive (V^+) and negative (V^-).

Device:	SET Resistance (Ω)	Threshold voltage (V)	Threshold current (µA)
Ternary (BSU)	*(V^+ / V^-)*	*(V^+ / V^-)*	*(V^+ / V^-)*
$(Ge_2Se_3)_{97}Sn_3$	$2 \times 10^4/1 \times 10^4$	~4.5 /~3.7	~0.9 /~0.9
$(Ge_2Se_3)_{97}Zn_3$	$2 \times 10^4/3 \times 10^3$	~3.0 /~3.2	~0.8 /~0.8
$(Ge_2Se_3)_{97}Sb_3$	$3 \times 10^4/5 \times 10^3$	~3.3 /~2.5	~0.7 /~0.7
$(Ge_2Se_3)_{97}In_3$	$3 \times 10^4/1 \times 10^4$	~3.8 /~2.9	~1.0 /~0.8

From Table 4.3 one can see that with a negative potential applied to the top W electrode, the SET resistance deceases on all Ternary samples, indicating a possible

difference in the Ternary film composition between the bottom and top W electrodes. This decrease was also seen in the threshold voltage for all samples excluding $(Ge_2Se_3)_{97}Zn_3$ which was found to have a threshold voltage that increased slightly with the negative potential. However, the variation is so slight, that it could possibly be accounted for by normal device-to-device variation.

4.2.5 Ternary Performance

After collecting the DC IV traces for the Ternary structures, additional IV measurements were performed on: (1) Isolated Bottom Electrode (IBE) 3% Sn and Zn Ternary devices with film thickness of ~830 Å instead of 450 Å, which will be discussed in further detail in Section 4.3.2.2; and (2) 800 Å GST wafer fabricated at Micron Technology, with a via diameter of 0.25 µm and Titanium-Nitride (TiN) bottom and top electrodes, to compare the electrical performance of the Ternary devices to that of a GST device as shown in Figure 4.10.

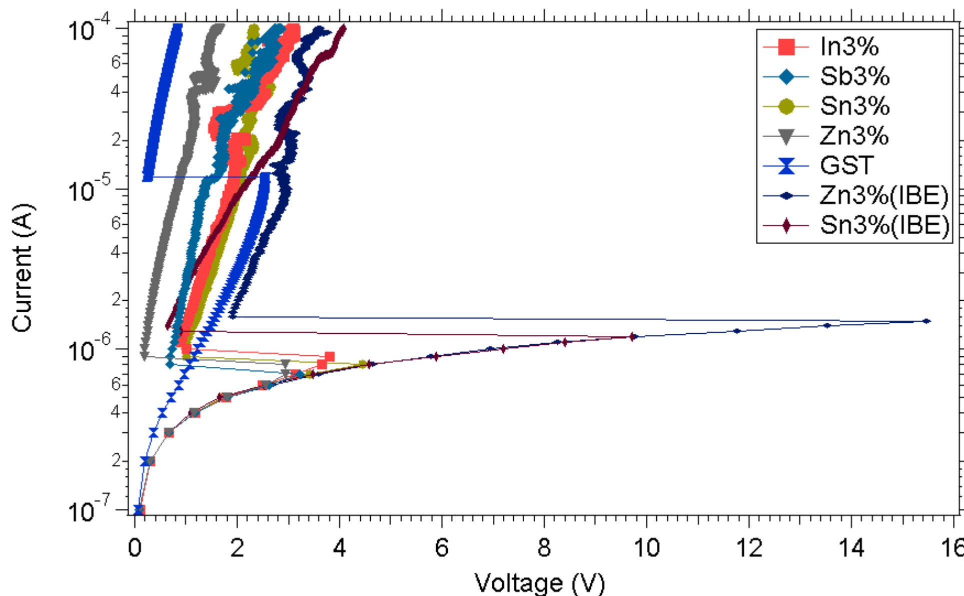


Figure 4.10: Representative IV traces of the GST, Ternary devices, and Isolated Bottom Electrode (IBE) Ternary devices. The GST devices were fabricated at Micron Technology in a process similar to the Layered devices and the IBE Ternary devices were fabricated in a process similar to the Ternary devices at Boise State University, as described in Chapter 3.

In Figure 4.10, IV traces of the GST and Ternary devices are shown. The current sweeps were performed by forcing current through the GST and Ternary devices from 100 nA to 100 µA, while measuring the voltage across the devices. As one can see, the snap-back current for the common bottom electrode Ternary devices was an order of magnitude less than that of the GST device. Similar, snap-back currents were also seen for the IBE Ternary devices even with the increase in film thickness (~830 Å instead of 450 Å), being the reason for the large increase in the threshold voltage for the IBE Ternary devices. However, the threshold voltage and SET resistance for the GST device was found to be lower than that of the Ternary devices as shown in Table 4.4.

Table 4.4: Typical threshold voltages/currents and SET resistances for Ternary and GST devices programmed with 100 µA of current.

Device:	SET Resistance (Ω)	Threshold voltage (V)	Threshold current (µA)
$(Ge_2Se_3)_{97}Sn_3$	2×10^4	~4.5	~0.9
$(Ge_2Se_3)_{97}Zn_3$	2×10^4	~3.0	~0.8
$(Ge_2Se_3)_{97}Sb_3$	3×10^4	~3.3	~0.7
$(Ge_2Se_3)_{97}In_3$	3×10^4	~3.8	~1.0
GST	1×10^4	2.5	10.0
IBE devices:			
$(Ge_2Se_3)_{97}Zn_3$	4×10^4	~15.0	~1.8
$(Ge_2Se_3)_{97}Sn_3$	4×10^4	~9.0	~1.3

4.3 Resistance Distribution

The Ternary wafer center, middle, and edge devices were measured, sweeping the current to 10 µA, 100 µA, and 1 mA with varying current resolution (due to limitations in the number of points allowed during a measurement on the B1500A). Resistance values extracted from IV traces at the center, middle, and edge of the wafer are compared in Figures 4.11 and 4.12.

4.3.1 Center, Middle and Edge Variation

The box plots contained in Figures 4.11 and 4.12, illustrate the sample mean with the line in the center of the diamond representing the group mean; the vertical span of the diamond representing the 95% confidence interval, with dash marks at the top and bottom most regions (of each box plot) representing one standard deviation. As shown in Figure 4.11, the bits located between the center and middle of the wafer show very similar

resistive values when compared to the edge; when programmed with 10 µA, 100 µA and 1mA of current. The 10 µA, 100 µA and 1mA SET resistances, show three distinct distributions regions on all Ternary samples excluding the 3% Sn sample due to variations in the SET resistance found during the measurements taken at the wafer edge. As discussed earlier, it is unknown whether these resistance distributions are due to partial crystallization at the 10 µA and 100 µA programming current, or due to the different crystalline phases that might be obtainable for each programming current. The different crystalline phases could arise due to the differences in temperature of the device under 1 mA (hottest), 100 µA (cooler), and 10 µA (even cooler) programming currents.

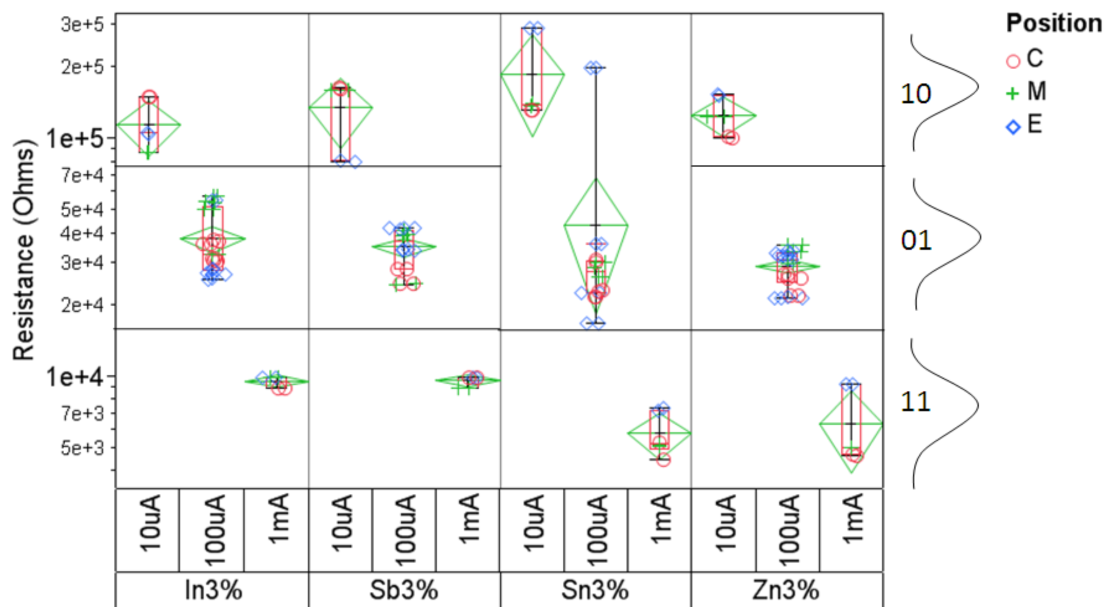


Figure 4.11: Representative resistance distributions seen for center (C), middle (M), and edge (E) position on the wafer for the Ternary devices programmed with 10 µA, 100 µA and 1 mA of current.

Figure 4.12, shows in greater detail the SET resistances for the Ternary devices, when comparing the mean resistance of a Virgin bit to one programmed with 10 µA and

100 µA, across the wafer (center, middle, and edge). From this data one can see three distinct, non-overlapping, resistance distributions. Indicating the possibility of multi-state behavior for the Ternary devices as explained in Chapter 2. However, the stability of the resistance distributions still need to be confirmed with cycling tests which were not performed due to the common bottom electrode. This will be discussed in further detail in Section 4.3.2.

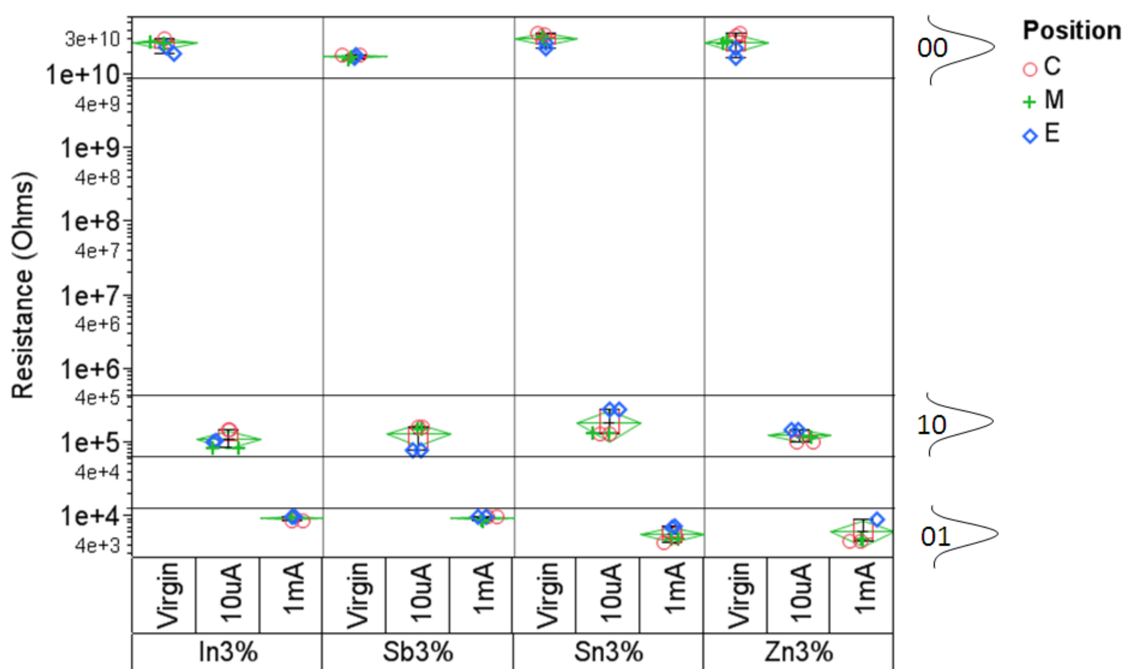


Figure 4.12: Representative resistance distribution seen when comparing sample material for center (C), middle (M), and edge (E) position on the wafer for the Ternary devices in a Virgin state and after programming multiple bits with 10 µA and 1 mA of current.

Table 4.5 summarizes the data shown in Figures 4.11 and 4.12, complete with values comparing the resistances mean and standard deviations for the Ternary devices in a virgin state and after being programmed with 10 µA, 100 µA (not shown in Figure 4.12), and 1 mA of current.

Table 4.5: Typical resistance distributions for the Ternary devices in a virgin state and programmed with 10 µA, 100 µA, and 1 mA of current.

Device:	Resistance (Ω)	Standard Deviation (Ω)
Ternary (BSU)	*(Virgin/10 µA/100 µA /1 mA)*	*(Virgin/10 µA/100 µA /1 mA)*
$(Ge_2Se_3)_{97}Sn_3$	3×10^{10} /1×10^5/2×10^4/5×10^3	5×10^9 /8×10^4/7×10^3/1×10^3
$(Ge_2Se_3)_{97}Zn_3$	2×10^{10} / 1×10^5/ 3×10^4/ 6×10^3	7×10^9 / 2×10^4/ 3×10^3/ 2×10^3
$(Ge_2Se_3)_{97}Sb_3$	1×10^{10} /1×10^5/3×10^4/9×10^3	1×10^9 /4×10^4/8×10^3/4×10^2
$(Ge_2Se_3)_{97}In_3$	2×10^{10} /1×10^5/ 3×10^4/9×10^3	4×10^9 / 2×10^4/ 1×10^4/ 5×10^2

4.3.2 Pulse Characteristics

Pulse measurements were performed on the Ternary samples to gain additional understanding of: (1) the possibility of multiple resistance states; and (2) to determine if the threshold voltage and programmed resistance of the device becomes stable as the material is cycled.

4.3.2.1 Pulse Testing

In determining the correct pulse widths and voltage amplitudes for the RESET/SET pulses, devices were initially programmed into a low resistance (SET) state by forcing 100 µA of current through the device with a DC sweep, as it is less stressful on a new device to program it when it is starting in a low resistance state. From the SET state, the devices were subjected to a series of pulses generated by the B1530A pulse module in order to: (1) RESET the device to a high resistance state; (2) read the device resistance; (3) SET the device to a low resistance state; and (4) read the device resistance. A representative pulse sequence is shown in Figure 4.13.

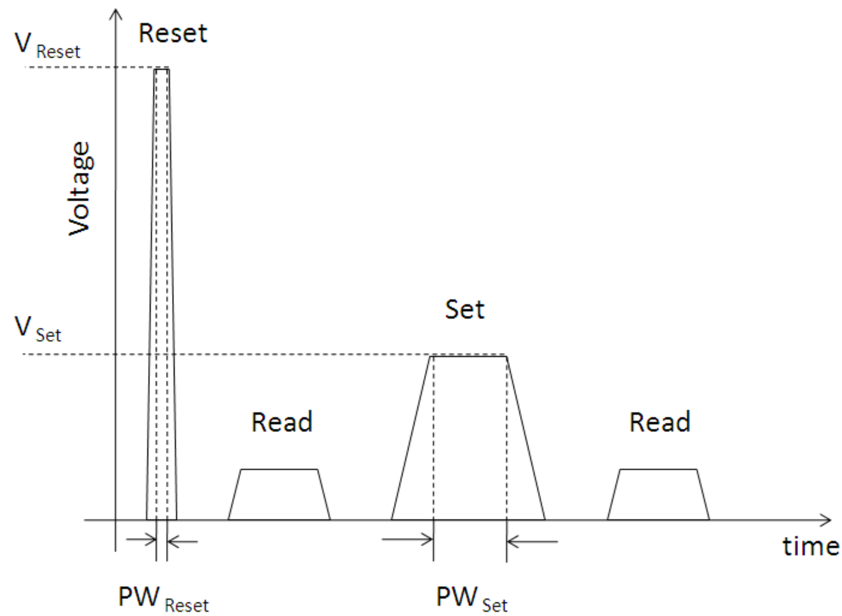


Figure 4.13: Representative trace of pulse tests performed, where V_{Set} is the amplitude of the SET pulse; V_{Reset} is the amplitude of the RESET pulse; PW_{Set} is the pulse width of the SET pulse; and PW_{Reset} is the pulse width of the RESET pulse. Between the SET and RESET are the READ pulses as shown above.

During the pulse tests with the Ternary devices, it was found that having a common bottom electrode across the wafer was too capacitive to allow for measurements of the device pulse response at the pulse widths necessary for programming. Figure 4.14 shows an example of one of the current traces measured during the pulse tests performed on the Ternary samples. In Figure 4.14 one can see current at the transitional edges of the voltage pulses (as the voltage potential switches), indicative of a large capacitance.

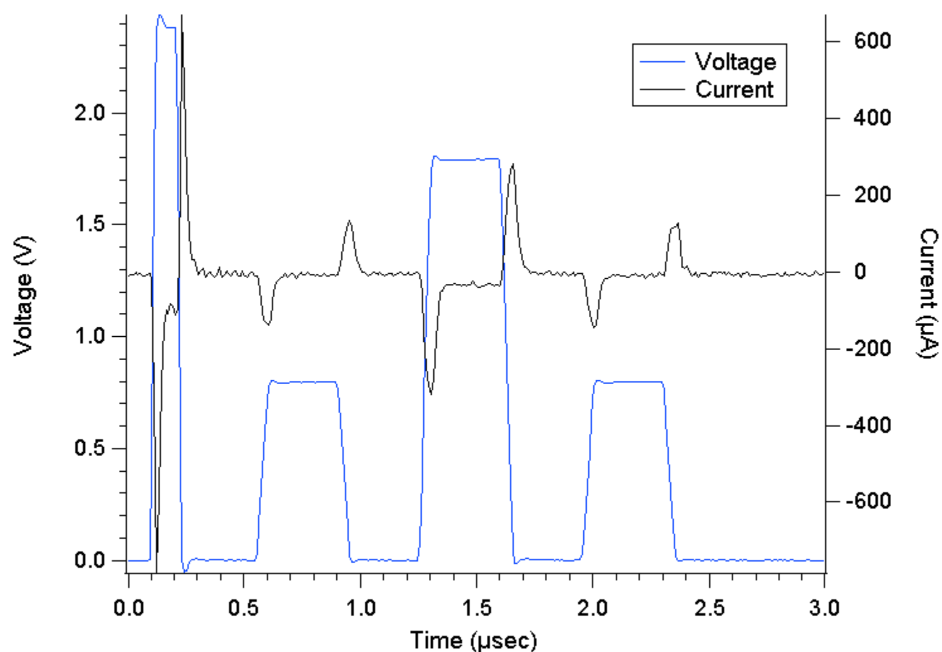


Figure 4.14: Current measured through a Ternary $(Ge_2Se_3)_{97}Sb_3$ device (black trace) in response to the applied voltage pulse train (blue trace). The large capacitance of the common bottom electrode, as observed in the current trace, prevents pulse testing on these samples.

Due to the common bottom electrode capacitance, samples consisting of layered chalcogenide materials, fabricated at Micron technology, were characterized while a new set of Ternary wafers with isolated bottom electrodes were processed at Boise State University. The data for the Layered samples is discussed in Chapter 5.

4.3.2.2 Isolated Bottom Electrode Ternary Devices

Ternary devices with 3% Sn and Zn with isolated bottom electrodes were fabricated at Boise State University to eliminate the issue of the capacitance due to a common bottom electrode. The newly fabricated Ternary samples were designed with isolated bottom electrodes, similar via dimensions, but thicker Ternary films (~830 Å

instead of 450 Å). Figure 4.15 provides a representative trace of the pulse tests for the $(Ge_2Se_3)_{97}Sn_3$, isolated bottom electrode device.

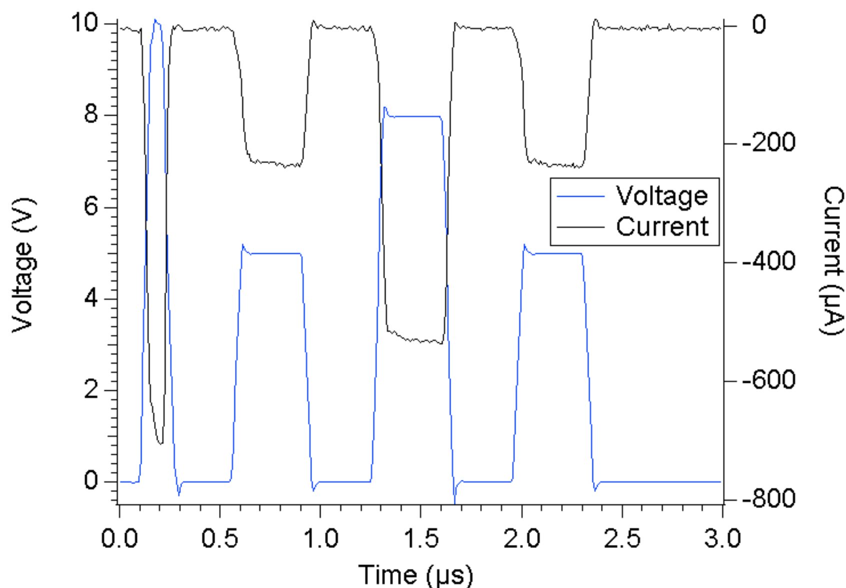


Figure 4.15: Representative trace of the pulse response for the $(Ge_2Se_3)_{97}Sn_3$ isolated bottom electrode devices.

As one can see from Figure 4.15, the large capacitance observed in all of the common bottom electrode samples is no longer present. Further pulse testing was not performed on the isolated bottom electrode Ternary samples due to the thickness of the Ternary film being much different than the devices tested in this thesis (830 Å vs 450 Å), causing the need for a very large RESET pulse amplitude and thus conditions too extreme for the B1530 measurement unit. However, these isolated bottom electrode Ternary structures did provide data supporting the theory that it was the common bottom electrode producing the large capacitance in the original Ternary devices, and they will be used for future studies on the electrical properties of the Ternary devices. Moreover,

TEM images will be collected on these isolated bottom electrode devices at Micron Technology, to see if the isolated bottom electrode Ternary samples have the same processing issues as seen on the Ternary samples, discussed in Section 4.1.1.

4.4 Conclusions

The electrical performance of the Ternary structures fabricated at Boise State University using the process that was described in Chapter 3 has been presented. From the IV traces only one visible snap-back region was found on each of the Ternary samples. Center, middle, and edge measurements were conducted, finding bits located between the center and middle of the wafer to have very similar resistive values when compared to the edge; when programmed with 10 µA, 100 µA and 1mA of current. Moreover, separable resistance distributions were measured for each of the current programming values of 10 µA, 100 µA and 1mA. The SET resistances show three distinct distributions on all Ternary samples excluding the 3% Sn sample due to variations in the SET resistance found during the measurements taken at the wafer edge. When reviewing the performance of the Ternary devices compared to the GST device fabricated at Micron Technology, a large improvement in the current requirements for the Ternary devices was found; all Ternary devices showed threshold currents that were of an order of magnitude less than that of the GST device. However, the threshold voltage and SET resistance for the GST device was lower than that of the Ternary devices.

A TEM cross-section image was collected at the location between the wafer center and middle of the wafer (middle: being the location between the wafer center and wafer edge) to characterize the fabricated device structure. Based on the TEM images it

was found that the Ternary devices have an unwanted etch region in the nitride adjacent to the via, which contributes to a thinner chalcogenide material at the via edges. TEM images will be collected for further investigation into Ternary wafers with isolated electrodes to see if the unwanted etch region has been eliminated.

When performing pulse tests, it was found that devices fabricated with a common bottom electrode exhibited too much capacitance to perform the pulse test measurements. Devices with isolated bottom electrodes were subsequently fabricated at BSU and did not exhibit the capacitance. However, the active Ternary layer in the isolated bottom electrode samples was too thick (nearly twice as thick as required), thus precluding the devices from being RESET through application of a pulse due to the higher potential requirements. In order to collect pulse data and cycling measurements, Layered structures with isolated bottom electrodes fabricated at Micron technology were tested. These results are described in further detail in Chapter 5.

CHAPTER 5: LAYERED DEVICE PERFORMAMCE

5.1 Introduction

Devices fabricated with the three different layer compositions, GeTe/SnTe, Ge_2Se_3/SnTe, and Ge_2Se_3/SnSe and isolated bottom electrodes were electrically characterized. These devices will be referred to throughout this chapter as the Layered structures, or the GeTe/SnTe, Ge_2Se_3/SnTe, and Ge_2Se_3/SnSe structures.

In this chapter, a physical description of the device as-fabricated is provided, along with a TEM image of one of the fabricated devices. This is followed by the electrical characterization results for DC and pulse response measurements.

5.1.1 Device Description

The Layered devices were fabricated at Micron Technology using a process described in Chapter 3. TEM cross-section images from the GeTe/SnTe device were taken from the wafer center region in 2005, one of which can be seen in Figure 5.1 [7], and again in September 2009 (Figure 5.2). As seen in Figure 5.1 the GeTe/SnTe evaporated material has reduced step coverage over the sidewalls of the via similar to the BSU Ternary samples. It should be noted that the same film deposition tool was used for the Micron Layered samples and the BSU Ternary samples; this tool was donated to BSU in 2006.

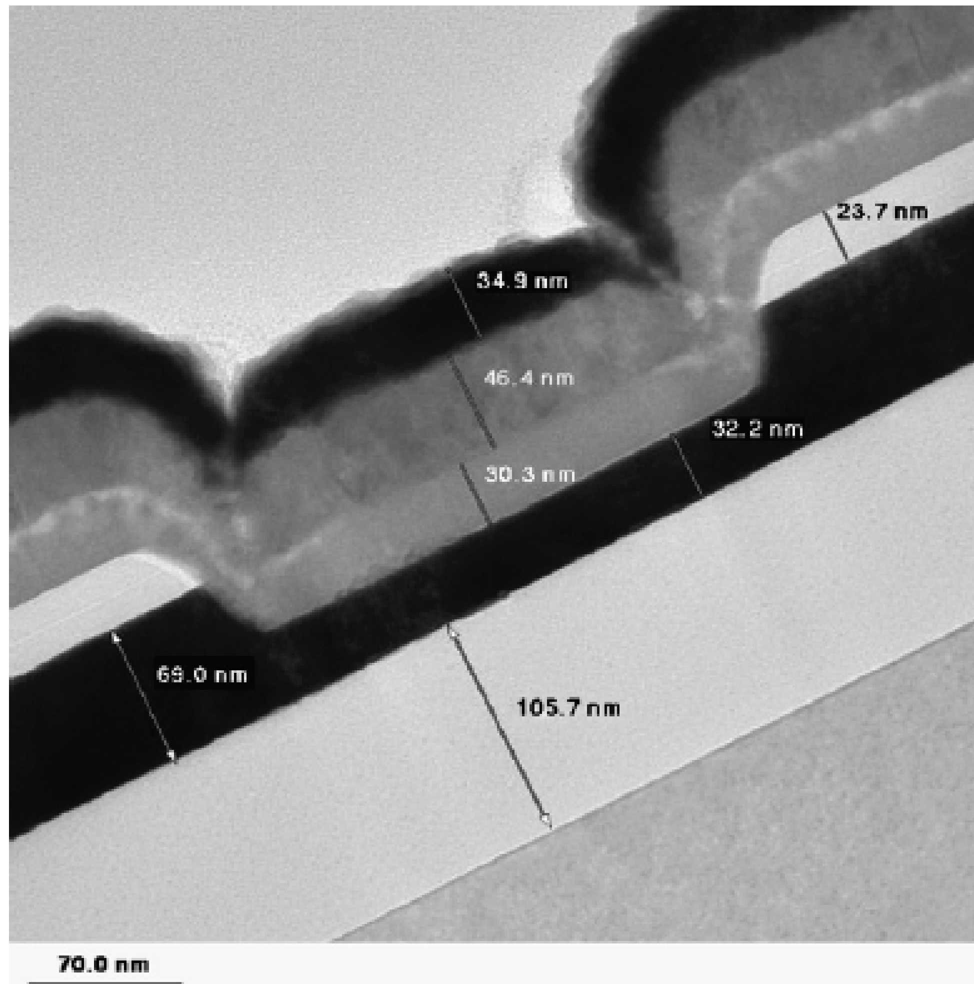


Figure 5.1: TEM cross-section taken in 2005 GeTe/SnTe device [7], created at Micron in 2005.

A TEM image was taken from a device at the wafer edge in September 2009, is shown in Figure 5.2. In this figure, side wall thinning, near the bottom W electrode and the Si_3N_4 interface, was found to be more apparent than shown in Figure 5.1. From the measurements taken, one can see that the nitride thickness of the edge sample is almost double the thickness of the center sample (Figure 5.1). As a result, the GeTe/SnTe film thickness between the bottom and top W electrodes at the side wall is much thinner than

the GeTe/SnTe layer near the center of the via (75.4 nm at the center). As shown in Figure 5.2, the Si_3N_4 layer at the wafer edge is almost double the thickness of the sample collected at the wafer center in 2005. Interestingly, the evaporated layers have better thickness uniformity across the wafer than the nitride film. It should also be noted that the contour of the Si_3N_4 layer at the step (on the right hand side of the via) is slightly different, increasing the slope of the step when compared to the opposite side of the via.

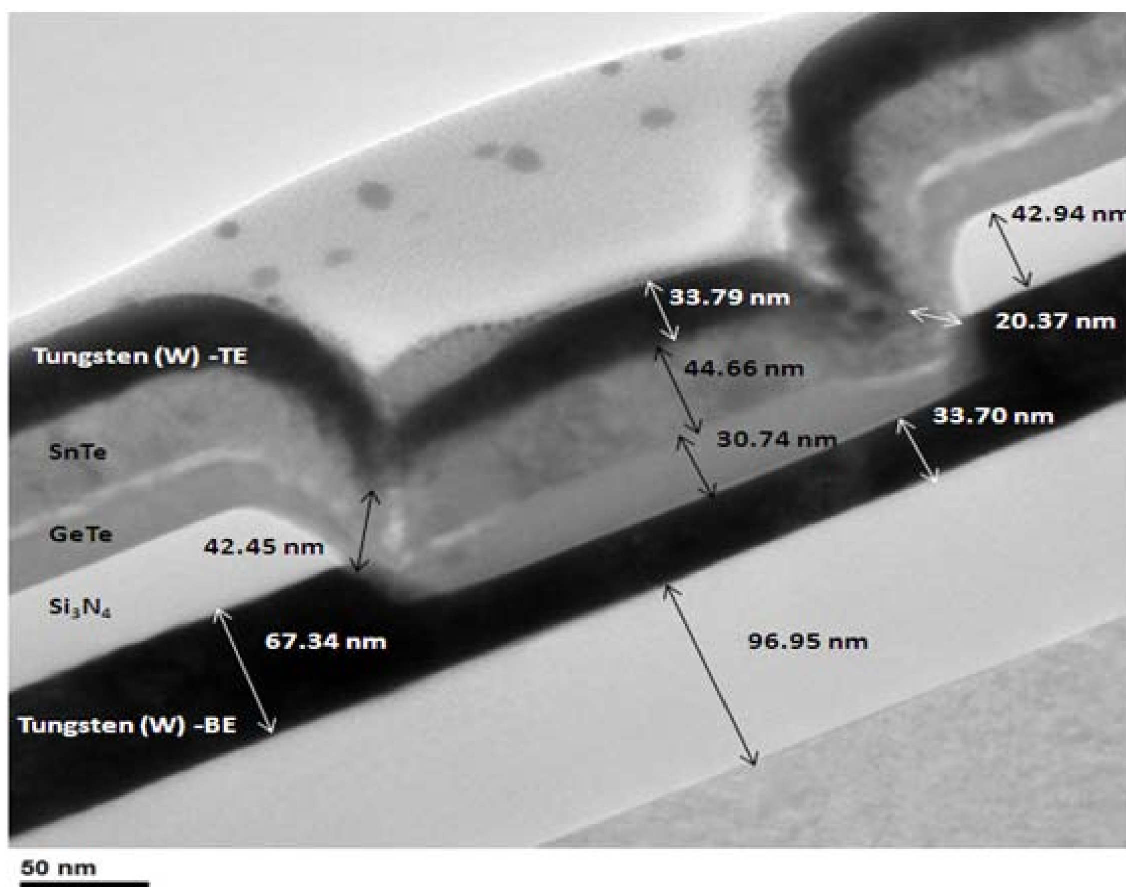


Figure 5.2: TEM cross-section taken in 2009 of GeTe/SnTe device. TEM image courtesy of Micron in 2009.

This reduction in the sidewall thickness was also seen in the Ternary samples, resulting in a possible non-standard active region, potentially effecting the electrical properties of the device. It should be noted that the electrical measurements provided in this thesis were performed on the edge sample from which this TEM cross-section in Figure 5.2 originated.

5.2 Electrical Testing and Measurements

Electrical testing on the Layered structures was performed using the same experimental setup used to test the Ternary devices (Section 4.2.1). In order to allow a direct comparison of the two devices, all electrical testing variables were kept the same.

5.2.1 Electrical Characteristics

Typical quasi-static IV traces from the GeTe/SnTe, Ge_2Se_3/SnTe and Ge_2Se_3/SnSe Layered samples are shown in Figure 5.3. The IV data was measured by forcing current through a virgin bit with current sweeps of 1 mA and 100 µA (for better resolution, as described in Chapter 4). Traces from the Ge_2Se_3/SnTe and Ge_2Se_3/SnSe Layered structures show a very sharp (low threshold current) snap-back when compared to the GeTe/SnTe structure for the 100 µA trace. Similar snap-back voltages were also found between the 1 mA and 100 µA current sweeps for the Ge_2Se_3/SnSe and GeTe/SnTe samples. Moreover, all Layered samples were found to have lower SET resistance values when compared to the Ternary devices as summarized in Table 5.1. The presence of multiple snap-back regions on all samples was not apparent for the 1 mA and 100 µA

current sweeps. However, there were some dissimilarities in the IV characteristics at higher current values.

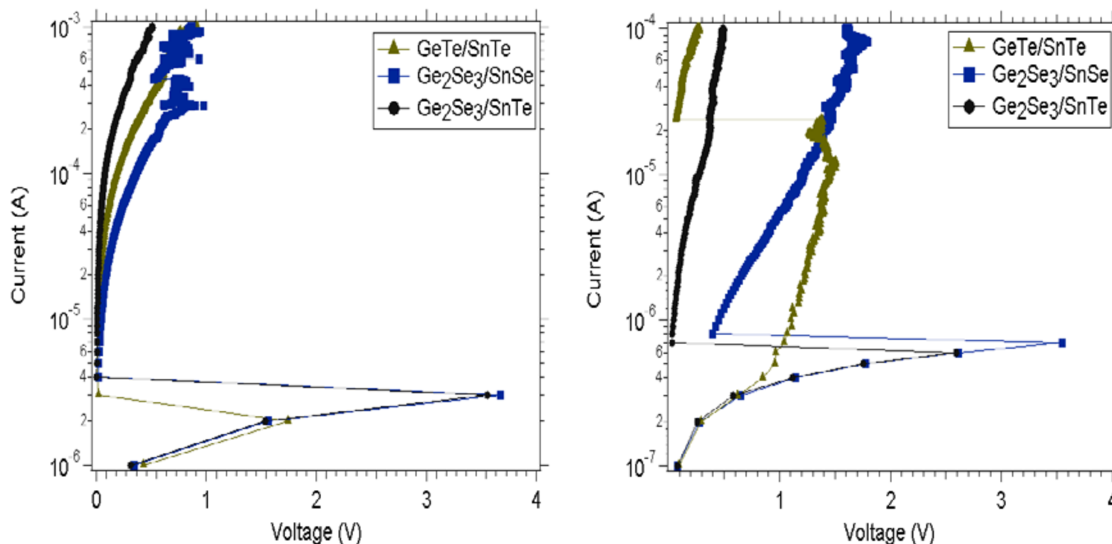


Figure 5.3: Representative IV traces for the Ternary devices with a positive potential applied to the top electrode, showing the threshold voltage variation with lower resolution: Left – 1 mA current sweep with 1 µA increments; Right – 100 µA current sweep with 100 nA increments.

Table 5.1 provides a comparison of the Ternary devices and the 2005/2009 Layered device measurements showing the threshold voltages/currents and typical initial resistance values of a device prior to switching and after the devices are programmed or SET with 1 mA of current. For all samples, the initial and programmed resistances were measured at 20 mV, for a direct comparison to the measurements taken on the Layered devices in 2005. Differences in the threshold voltage and resistance values were compared by applying a positive potential to the top W electrode, sweeping the current to 1 mA with increments of 1 µA. As one can see, only slight variations in the SET resistance and threshold voltages were found for Layered structures (Layered (2009)).

Table 5.1: Typical initial and programmed (SET) resistances and threshold voltage/currents for the devices programmed with 100 µA and 1 mA of current, using a positive potential on the top W electrode.

Device:	Initial Resistance (Ω)	SET Resistance (Ω)	Threshold Voltage (V)	Threshold Current (µA)
Ternary (BSU)	*Virgin Bit*	*(100 µA /1 mA)*	*(100 µA /1 mA)*	*(100 µA /1 mA)*
$(Ge_2Se_3)_{97}Sn_3$	>4 x 10^{10}	2 x 10^4/6 x 10^3	~4.5 /-	~0.9 /-
$(Ge_2Se_3)_{97}Zn_3$	>3 x 10^{10}	2 x 10^4/~7 x 10^3	~3.0 /-	~0.8 /-
$(Ge_2Se_3)_{97}Sb_3$	>2 x 10^{10}	3 x 10^4/9 x 10^3	~3.3 /-	~0.7 /-
$(Ge_2Se_3)_{97}In_3$	>3 x 10^{10}	3 x 10^4/9 x 10^3	~3.8 /-	~1.0 /-
Layered (2005)				
Ge_2Se_3/SnTe	>6 x 10^6	2 x 10^3/7 x 10^2	3.7 /3.7	-
Ge_2Se_3/SnSe	>6 x 10^6	1 x 10^3/5 x 10^2	3.7 V /3.7 V	-
GeTe/SnTe	>5 x 10^6	1 x 10^4/5 x 10^2	1.6 V /1.6 V	-
Layered (2009)				
Ge_2Se_3/SnTe	>6 x 10^6	6 x 10^3/1 x 10^3	~2.6 /-	~0.7 /-
Ge_2Se_3/SnSe	>5 x 10^6	7 x 10^3/1 x 10^3	~3.7 /-	~0.8 /-
GeTe/SnTe	>5 x 10^6	2 x 10^3/7 x 10^2	~1.6 /-	~20.0 /-

As one can see from Table 5.1, the $(Ge_2Se_3)_{97}Zn_3$ and $(Ge_2Se_3)_{97}Sb_3$Ternary devices show a significant performance improvement over the Ge_2Se_3/SnTe and Ge_2Se_3/SnSe Layered devices for the 1 mA current sweeps. As shown/discussed in Chapter 4, it was found that when using a 1 mA current sweep an inaccurate threshold voltage for the device is displayed due the resolution being too low to determine the true location of the snap-back for the devices. Using lower current sweeps and increased

sampling, it was found that the threshold voltage for all Ternary devices increased. However, this was not as apparent for the Layered structures.

One can also see that the SET resistances for the Ternary devices are on average an order of magnitude higher than that of the Layered devices for all samples tested. Moreover, the threshold currents and voltages are found to be very similar when comparing the 100 µA measurements; excluding the GeTe/SnTe and $(Ge_2Se_3)_{97}Sn_3$ devices which were found to have the lowest and the highest threshold voltages, respectively.

5.2.2 Bit-to-Bit Variation

All IV traces shown in Figures 5.4 and 5.5 were collected by forcing current through virgin Layered devices from 100 nA to 100 µA and 10 nA to 10 µA while measuring the voltage across the device.

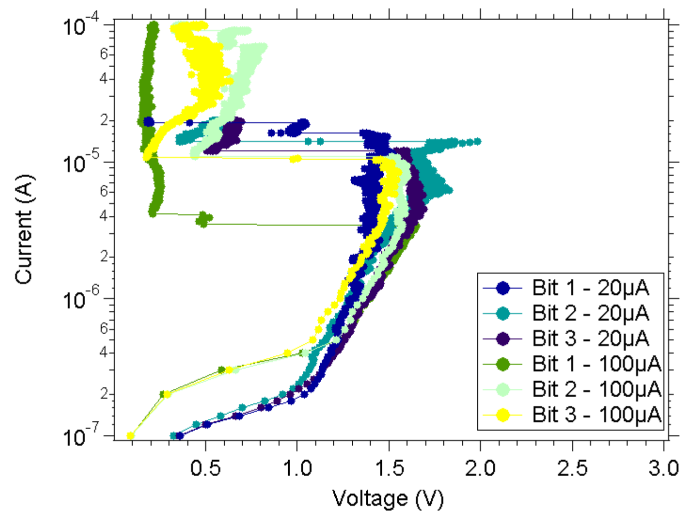


Figure 5.4: Representative IV curve for a GeTe/SnTe Layered device with a positive potential applied to the top electrode, showing bit-to-bit variation.

When measuring the IV characteristics of the GeTe/SnTe Layered structure, a current sweep of 10 µA was found to be too low to cause the bit to reach a threshold voltage of 1.6 V. To capture the snap-back voltage for the GeTe/SnTe device a 20 µA current sweep was performed showing comparatively stable snap-back voltage at 1.6 V, with only slight variations in the threshold current for the majority of the bits when comparing the 20 µA current sweep to the 100 µA current sweep. Of note, as seen on the Bit1-20 µA and Bit1-100 µA trace, multiple snap-backs are present. However, a single snap-back for the GeTe/SnTe Layered device was found to be more common than the dual snap-back shown in the Bit1-20 µA and Bit1-100 µA traces.

When comparing the bit-to-bit variation seen on the Ge_2Se_3/SnTe and Ge_2Se_3/SnSe Layered devices, a similar pattern as the Ternary devices was found in that an increase in sampling at lower current values corresponds to a decrease in the threshold current. This is shown in Figure 5.5. As explained in Chapter 4, one possibility for this pattern is due to the rate at which the material is being heated (Joule heating) due to the increment at which the current is being applied.

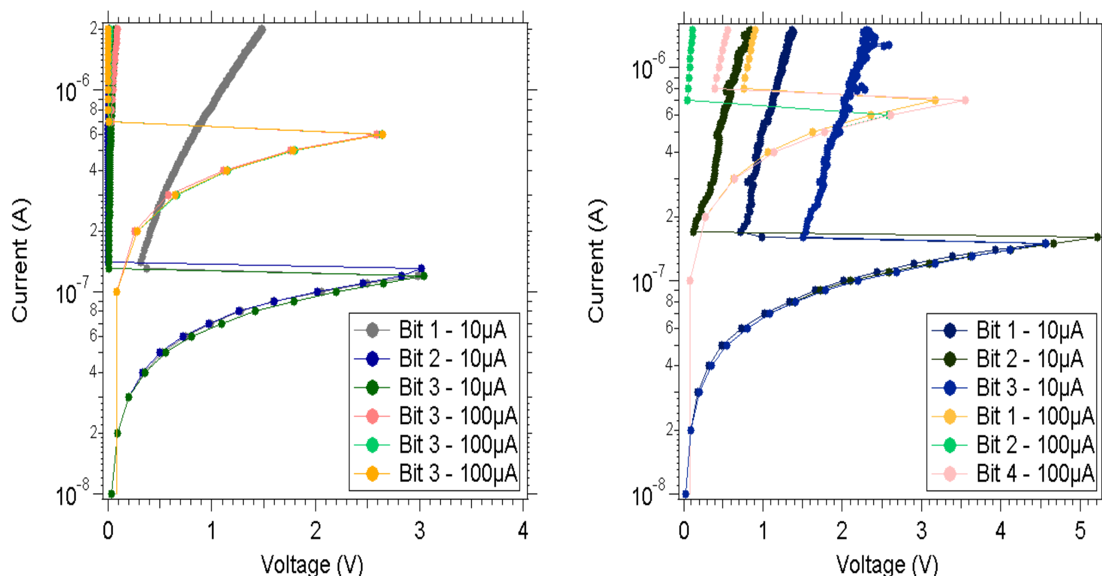


Figure 5.5: Representative IV-Curve with a positive potential applied to the top electrode, showing bit-to-bit variation: Left - Ge_2Se_3/SnTe device; Right - Ge_2Se_3/SnSe device.

A summary of the SET resistances and threshold current/voltages from the device with measured-IV curves shown in Figures 5.3 through 5.5 is provided in Table 5.3. In each case, a positive potential is applied to the top electrode.

Table 5.2: Typical threshold voltage/current values for devices programmed with 10 µA, 100 µA, and 1 mA of current with a positive potential applied to the top electrode.

Device:	SET Resistance (Ω)	Threshold voltage (V)	Threshold current (µA)
Layered (Micron)	*(10 µA/100 µA/1 mA)*	*(10 µA /100 µA/1 mA)*	*(10 µA /100 µA/1 mA)*
Ge_2Se_3/SnTe	$4x10^4/6x10^3/1x10^3$	~3.2 /~2.6 /-	~0.1 /~0.7 /-
Ge_2Se_3/SnSe	$1x10^5/7x10^3/1x10^3$	~4.6 /~3.7 /-	~0.2 /~0.8 /-
GeTe/SnTe	- / $2x10^3/7x10^2$	- /~1.6 /-	- /~20.0 /-

Note: - indicates that measureable response is not valid due to the current resolution.

As was shown in Chapter 4 for the Ternary materials, slight variations in the threshold voltage/current were found after applying the 10 µA and 100 µA programming current sweeps. When compared to the variations seen for the Ternary samples the Layered structures were found to be more consistent for the threshold voltage and less consistent for the threshold currents with increased resolution (i.e. or lower programming currents). It should also be noted that the SET resistances after applying the 10 µA, 100 µA, and 1 mA are an order of magnitude different. This resistance distribution for the Layered devices is very important and is sought after for multi-bit storage devices. These resistance distributions can better be seen in the box plots shown in Figures 5.6 and 5.7.

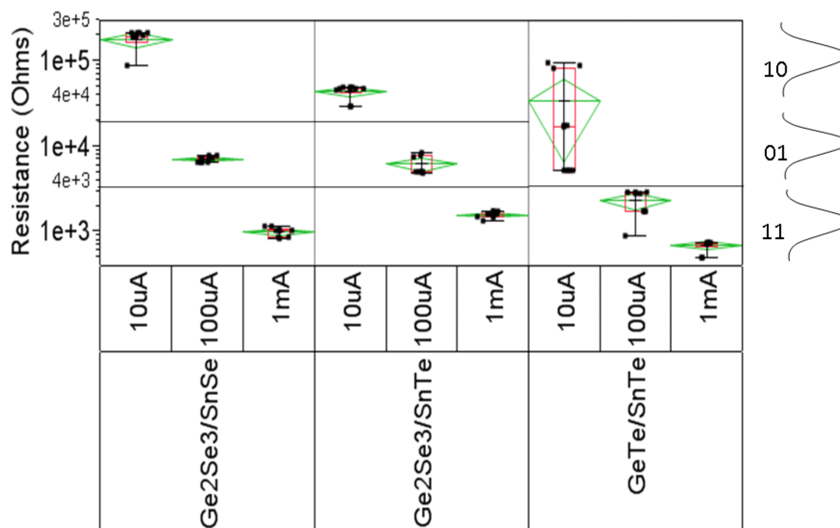


Figure 5.6: Representative resistance distributions seen for the Layered devices programmed with 10 µA, 100 µA and 1 mA of current.

Figure 5.6 provides the representative resistance distribution of the Layered devices after being programmed with 10 µA, 100 µA, and 1 mA of current showing three distinct SET resistance values for the Ge_2Se_3/SnSe and Ge_2Se_3/SnTe devices and only two for the GeTe/SnTe device. Similar resistance distributions were also seen for the

Ternary samples indicating the possibility of multi-state programming. However, the stability of the resistance distributions are still unknown. Moreover, it is possible that the bits are in a partially crystalline state at these resistance values. Figure 5.7 is an additional representative resistance distribution showing the Layered devices resistance for a virgin bit and one programmed with 10 µA and 1 mA, further showing the possibility of distinct, non-overlapping resistance distributions for possible multi-state programming.

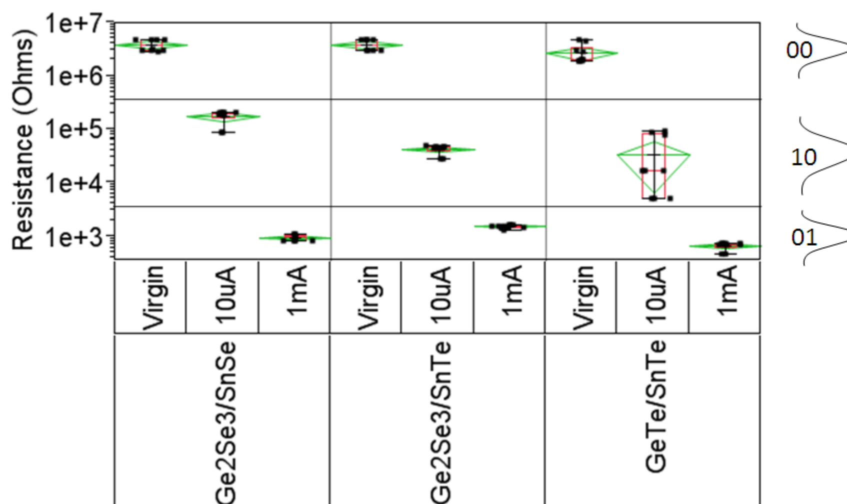


Figure 5.7: Representative resistance distributions seen for the Layered devices in a Virgin state and after being programmed with 10 µA and 1 mA of current.

With a positive potential applied to the top W electrode there is likely Sn-ion migration from the SnSe or SnTe layer into the Ge_2Se_3 or GeTe as the material is programmed; chemically altering the Ge_2Se_3 and GeTe layers to an $(Ge_2Se_3)_xSn_y$ or $(GeTe)_xSn_y$ alloy. To observe possible changes in the snap-back voltage without the possible Sn-ion migration, the polarity of the top and bottom electrodes were switched.

Figure 5.8 shows a representative IV trace for the GeTe/SnTe Layered device with a negative potential applied to the top W electrode. As one can see from Figure 5.8, a significant change in the threshold voltage and current were found when compared to the electrical measurements with a positive potential applied to the top electrode of the GeTe/SnTe device (Figure 5.4), as was also seen in the 2005 measurements. A large amount of variation was seen in the threshold current when a negative potential was applied, compared to the current traces with a positive potential applied to the top electrode of the device.

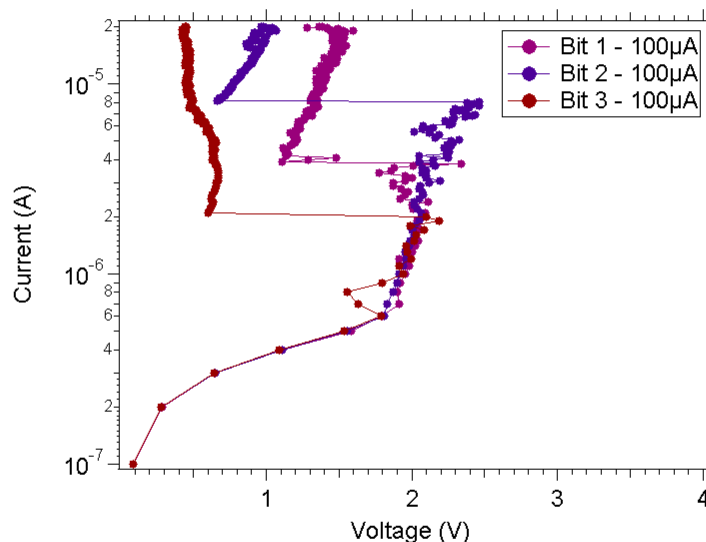


Figure 5.8: Representative IV curve for a GeTe/SnTe Layered device with a negative potential applied to the top electrode, showing bit-to-bit variation.

As seen in Figure 5.9, a slight increase in the threshold voltage was found for the Ge_2Se_3/SnTe device, with a threshold voltage increasing from ~2.6 V to ~3.7 V. The Ge_2Se_3/SnSe Layered devices with a negative potential is applied to the top electrode showed no switching response, which was as expected since there was neither Sn ions

nor Te ions available for migration into the Ge_2Se_3 glass layer [7]. If it were possible for Se ions to be forced into the Ge_2Se_3 glass from the SnSe layer, they would likely only succeed in making a Ge_2Se_3 glass more Se-rich and thus still incapable of phase-change switching under the operating conditions used in this thesis [7].

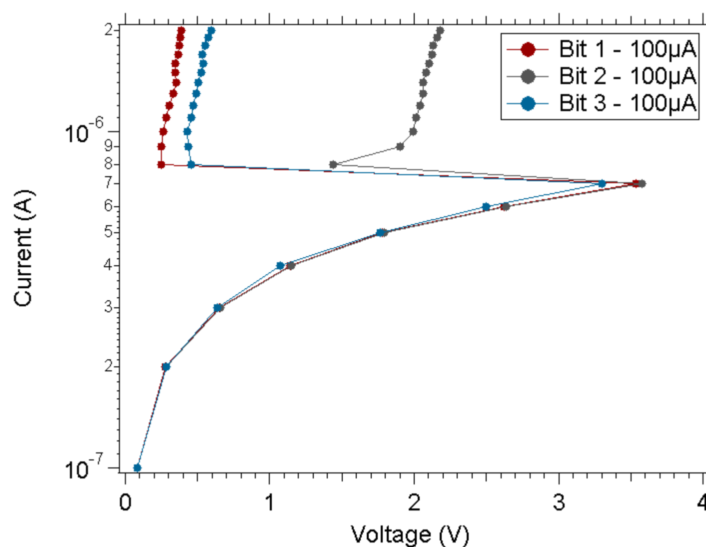


Figure 5.9: Representative IV-Curve with a negative potential applied to the top electrode, showing bit-to-bit variation: Left - Ge_2Se_3/SnTe device.

Table 5.3 as summary of the SET resistance and threshold voltages and currents for the data given in Figures 5.8 and 5.9, including data with positive (V^+) and negative (V^-) polarities applied to the top W electrode.

Table 5.3: Typical threshold voltage/current values for devices programmed with 100 μA of current with a positive and negative potential applied to the top electrode.

Device:	SET Resistance (Ω)	Threshold voltage (V)	Threshold current (μA)
<u>*Layered (2009)*</u>	*(V^+ / V^-)*	*(V^+ / V^-)*	*(V^+ / V^-)*
Ge_2Se_3/SnTe	6 x 10^3/7 x 10^3	~2.6 /~ 3.7	~0.7 / ~0.8
Ge_2Se_3/SnSe	7 x 10^3/ -	~3.7 / -	~0.8 / -
GeTe/SnTe	2 x 10^3/2 x 10^4	~1.6/ ~2.4	~20.0 / ~7.0

Note: - indicates no measureable response.

5.2.3 <u>Layered Structure Performance</u>

In comparing the Layered device performance to the GST device performance (which was discussed in Section 4.2.4), the Ge_2Se_3/SnTe and Ge_2Se_3/SnTe Layered structures were found to have a large improvement in the current requirements as was seen with the Ternary samples. In both cases, the threshold current was an order of magnitude less than that of the GST device. However, for the GeTe/SnTe device the threshold current was found to be very similar to that of the GST device, showing instead an improvement in the voltage requirements; the threshold being ~1V less than that of the GST device as seen in Figure 5.10.

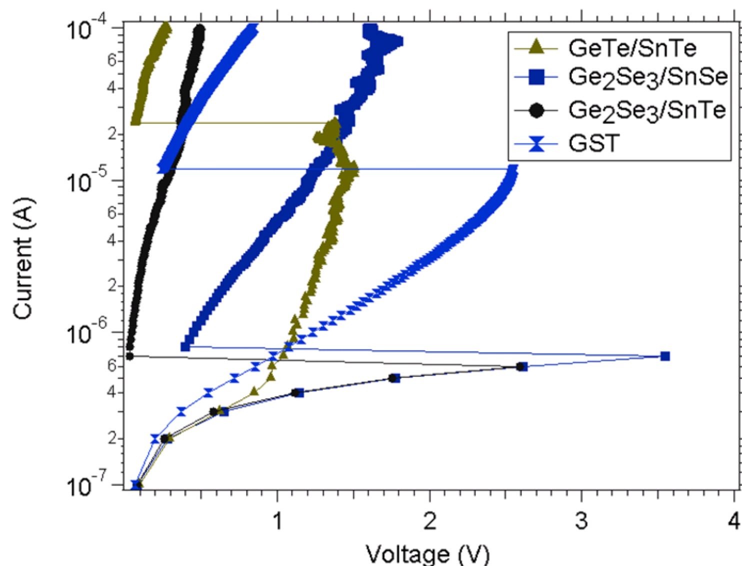


Figure 5.10: Representative IV traces of the GST vs Layered structures fabricated at Micron Technology.

5.2.4 Pulse Characteristics

Pulse measurements were performed on the Layered samples to elucidate the possibility of multiple resistance states and the effects of possible Sn-ion and Te-ion migration into the Ge-chalcogenide layer as the material is cycled. The majority of the test results in this section are collected with the GeTe/SnTe Layered devices as a result of a suitable RESET pulse value not being found for the Ge_2Se_3/SnTe and Ge_2Se_3/SnSe devices.

5.2.4.1 Pulse Testing

Due to the unknown pulse response of the Layered devices, rise/fall times and pulse amplitudes were determined by exploring various pulse conditions while the device response was measured. Once the device response was better understood, a pulse sequence (specific programming amplitudes and pulse widths) was selected and used for

characterization. The selected pulse conditions were not necessarily the best conditions for device longevity or cycling; a selection of those conditions would require a completely different testing emphasis. However, the selected conditions were adequate for the testing mechanisms proposed in this work.

As seen in Figure 5.11, minor alterations in the voltage amplitude can cause significant changes in the device response, as observed through the measured current traces. From the changes seen in the current traces in Figure 5.11, one can predict that: (1) a RESET voltage pulse amplitude of 2 V, will place the GeTe/SnTe device in a RESET state; this is apparent in the T1_Current trace, which shows no current during the “READ” pulse; (2) a RESET voltage amplitude pulse lower than 1.8 V will not RESET the GeTe/SnTe devices, as indicated by the READ pulse measured seen in the T2_Current trace after the RESET pulse; and (3) a SET voltage amplitude pulse of greater than 0.6 V is needed to SET the device (based on the amplitude of the READ pulse) with 1.5 V being sufficient as seen in the T1_ and T2_Current trace. Using this data, voltage pulse amplitude values can be determined for the RESET/SET pulses. In addition, the resistance of the material can be determined from the READ pulse, providing the needed data to reveal the possibility of multiple resistance states.

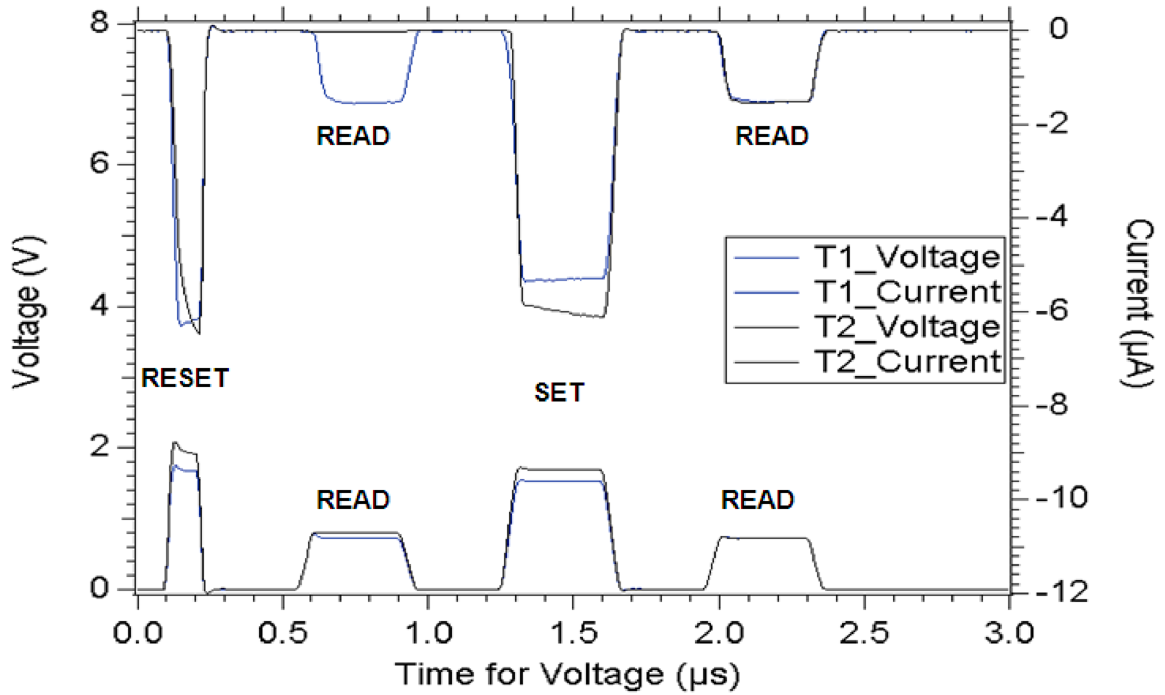


Figure 5.11: Representative pulse traces for the initial tests ran on the GeTe/SnTe device with pulse amplitude adjustments being made to the RESET and SET pulse.

5.2.4.2 RESET Pulse: GeTe/SnTe

Multiple pulse tests were performed, using the method explained in the previous section. Figure 5.12, shows a representation of various RESET pulse amplitude tests, with the rise and fall times fixed at 10 ns (the shortest fall time specified for the B1530A).

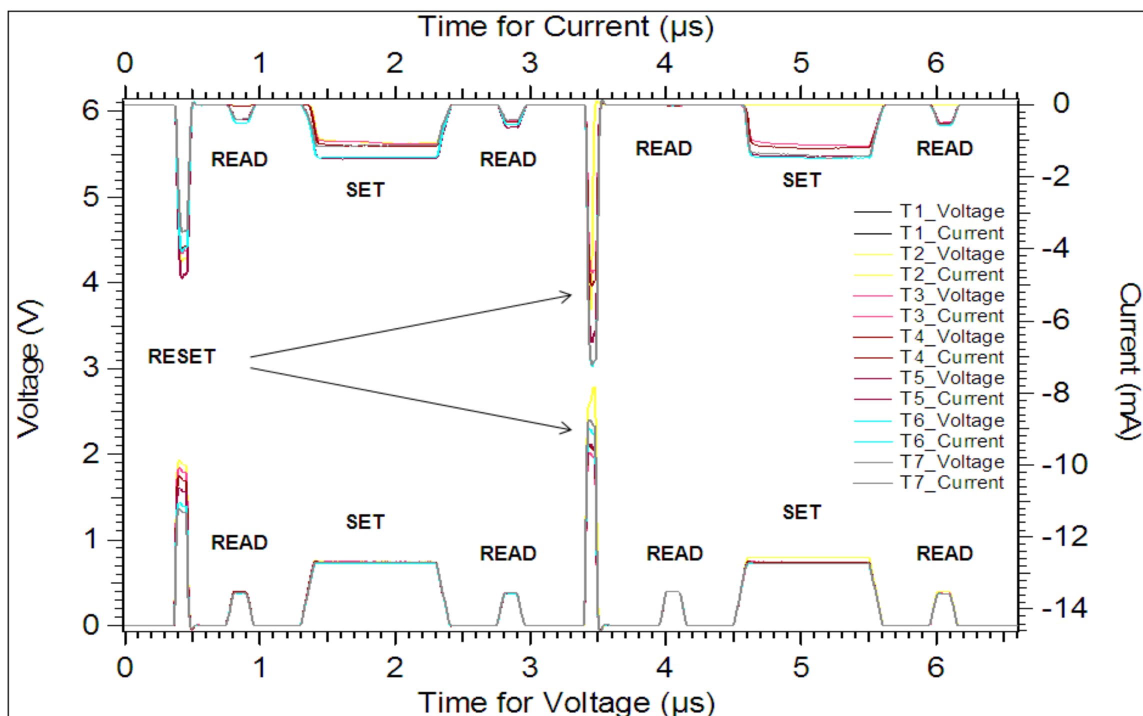


Figure 5.12: Representative pulse traces for the GeTe/SnTe device with amplitude adjustments being made to the RESET pulse.

As seen in Figure 5.12, with a reduced voltage pulse (below 2 V), not enough current is provided across the device to generate the Joule heating necessary to melt the material. Voltage amplitudes ranging from 2 V to 2.25 V were found to be sufficient to place the GeTe/SnTe in a stable RESET. Values above 2.8 V were found to cause the resistance to decrease and eventually break the device (see the 3 V case shown in the T2_Current trace in Figure 5.12 and 5.13).

Figure 5.13 is an expanded view of the voltage amplitude RESET pulse test shown in Figure 5.12. In Figure 5.13 one can clearly see that the current during the duration of the READ after the RESET pulse is not present, indicating that the bit is

RESET. However, after the (0.85 V) SET pulse is applied, the current during the READ pulse is once again present indicating that the bit has been placed in a SET state.

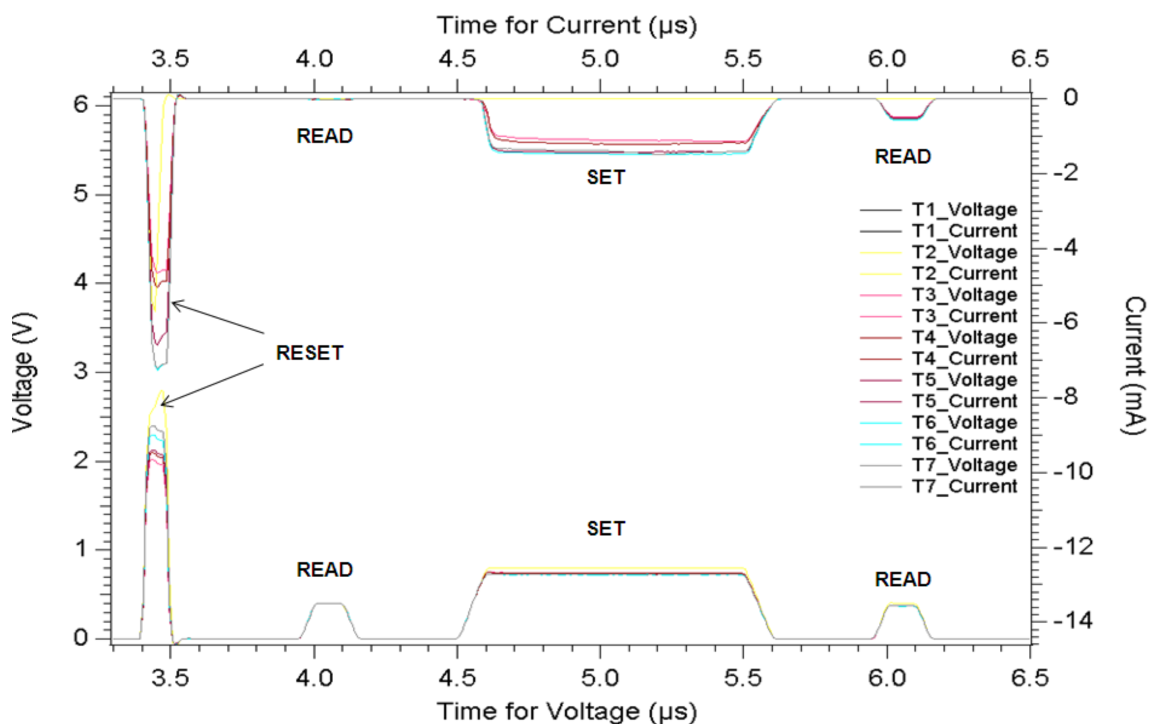


Figure 5.13: Representative pulse traces for the GeTe/SnTe device with amplitude adjustments being made to the RESET pulse taken from Figure 5.12 to emphasize the trace pattern.

Table 5.4 summarizes the data provided from the RESET amplitude tests shown in Figures 5.12 and 5.13, and a RESET pulse width test (which was not shown). From the RESET voltage amplitude tests, it was determined that RESET voltage amplitude of 2.25 V was sufficient to generate a stable RESET pulse when performed with the 100 ns pulse width and 10 ns rise/fall times.

Table 5.4: GeTe/SnTe device with pulse width adjustments made to the RESET pulse. Pulse width test had pulse amplitudes of 2.8 V; Pulse amplitude test had pulse widths of 100 ns; all RESET pulses had rise/fall times of 10 ns.

Device:	Pulse Width (ns)	Resistance (Ω)	Pulse Amplitude (V)	Resistance (Ω)
GeTe/SnTe	40	~2 x 10^4	1.6	7 x 10^3
	50	~2 x 10^4	2.0	2 x 10^4
	60	~2 x 10^4	2.1	2 x 10^4
	70	3 x 10^4	2.15	3 x 10^4
	80	3 x 10^4	2.2	4 x 10^4
	90	2 x 10^4	2.25	4 x 10^4
	100	2 x 10^4	2.8	2 x 10^4

For the pulse width tests, one can see significant resistance variations between 40 ns and 60 ns for the GeTe/SnTe devices. These fluctuations in resistance are most likely related to the limitations found when using the B1530A. Of note, when pulsing the Layered devices at these lower pulse widths, the voltage amplitude requested would often not be reached during the duration of the pulse. As a result, a voltage amplitude of 2.8 V was used on all pulse width tests to supply a voltage high enough to place the GeTe/SnTe device in a RESET state.

As the pulse width is increased above 70 ns, the voltage amplitude requested was found to be more uniform. As a result, pulse measurements below 70 ns were not found to be reliable when using the B1500A. From the test results shown in Table 5.4, rise/fall times of 10 ns were determined to be sufficient, to place the GeTe/SnTe Layered device

in a RESET state. It was also determined that a pulse width of 100 ns generated a stable RESET pulse for the GeTe/SnTe device.

For the Ge_2Se_3/SnTe and Ge_2Se_3/SnSe Layered devices multiple attempts at finding the RESET pulse were performed. However, no RESET pulse was found. One explanation for the RESET pulse issues seen with the Ge_2Se_3/SnTe and Ge_2Se_3/SnSe layered films is related to the low current, rapid snap-back, seen in the IV traces, suggesting a very fast transition when programming the devices. It is possible that in order to RESET these devices a pulse width of less than 30 ns with rise and fall times less than 10 ns would be needed to fully RESET these devices. Due to the lower pulse width limit on the Agilent B1530A being set at 30 ns, RESET tests were not found for the devices, an additional limitation found when using the B1530A for these tests.

5.2.4.3 SET Pulse: GeTe/SnTe

To SET the device or return it to a SET state when using a voltage pulse, the following sequence was performed: (1) A 100 nA to 100 μA current sweep was performed, prior to the RESET pulse to ensure that the bit was in a similar state at the beginning of each test; (2) The 100 ns RESET pulse with a voltage amplitude of 2.25 V was applied; (3) A READ pulse was then applied to ensure that the bit was RESET as seen in Figure 5.14; (4) Voltage amplitude adjustments were then made to the SET pulse; and (5) A READ pulse was used to determine the resistance of the bit after the SET pulse.

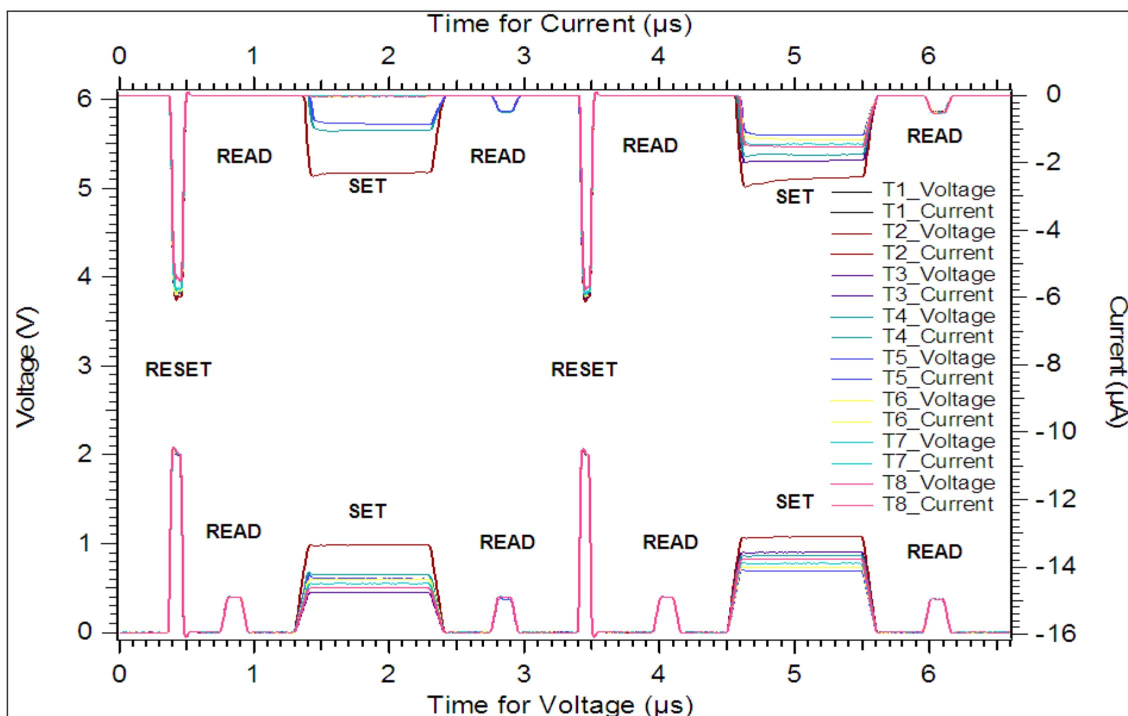


Figure 5.14: Representative pulse trace for the GeTe/SnTe device with amplitude adjustments being made to the SET pulse.

Figure 5.14 shows an overlay of various SET pulse voltage amplitude measurement results for a GeTe/SnTe Layered device. During the duration of the SET pulse a typical pattern is observed when programming the device into a SET state. This pattern (shown in Figure 5.14 and 5.15) consists of, a slight drop in current during the duration of the applied voltage pulse (as indicated by the * in Figure 5.15 on the T2_Current trace), followed by an extended fall time in the current trace. This pattern is an indication that the bit being tested is entering a SET state.

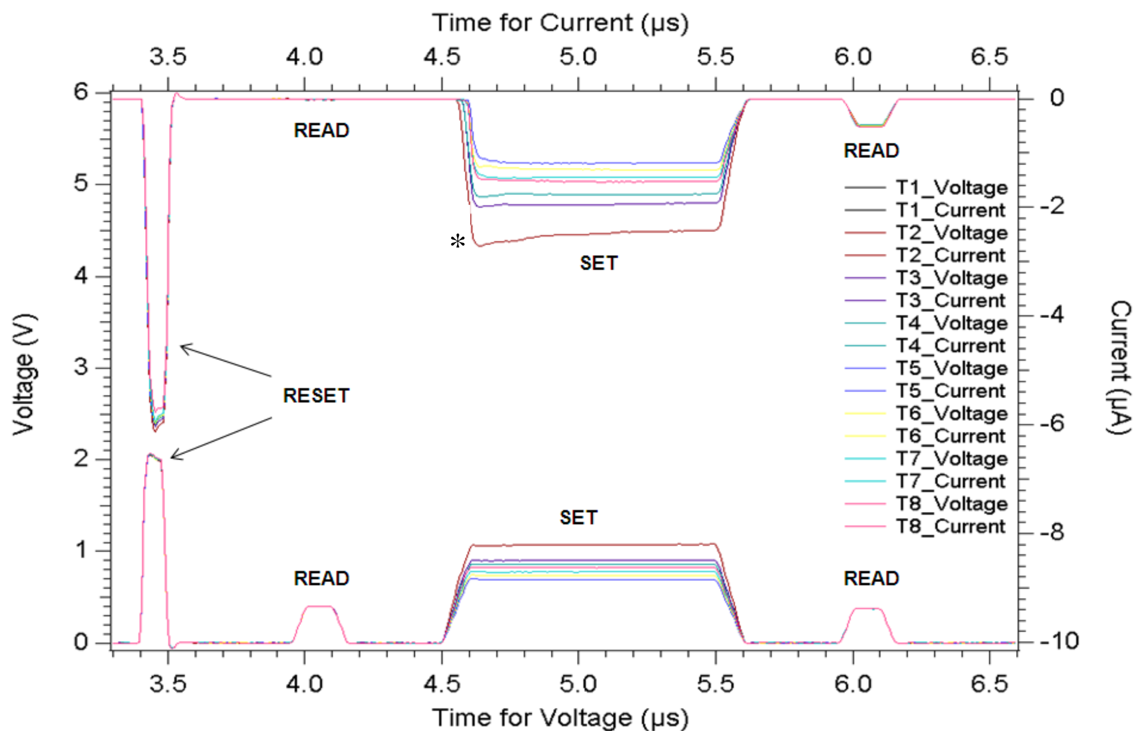


Figure 5.15: Representative pulse trace for the GeTe/SnTe device with amplitude adjustments being made to the SET pulse.

Table 5.5 summarizes the resistance changes seen in the SET pulse traces. From this data it was found that voltage amplitudes greater than 0.6 V are needed in order to change the phase of the device (*i.e.* in this case, to raise the temperature of the bit above the glass transition temperature as discussed in Chapter 1). For values between 0.75 V and 0.95 V stable SET pulse amplitudes were found, showing stable resistance values of 7 x 10^2 when applying a pulse width of 800 ns with 100 ns rise/fall times. This SET resistance value was found to be slightly higher when performing the SET pulse widths below 500 ns, as shown in Table 5.5.

Table 5.5: GeTe/SnTe device with pulse width adjustments made to the SET pulse. Pulse width test had pulse amplitudes of 0.85 V; Pulse amplitude test had pulse widths of 800 ns; all SET traces had rise/fall times of 100 ns.

Device:	Pulse Width (ns)	Resistance (Ω)	Pulse Amplitude (V)	Resistance (Ω)
GeTe/SnTe	150	1×10^4	0.45	3×10^4
	200	2×10^3	0.5	2×10^4
	250	1×10^3	0.55	3×10^4
	300	2×10^3	0.6	3×10^4
	350	2×10^3	0.65	8×10^2
	400	1×10^3	0.7	8×10^2
	450	1×10^3	0.75	7×10^2
	800	7×10^2	0.85	7×10^2

From Tables 5.4 and 5.5, the distribution in resistance values found after performing the SET and RESET pulse tests is not very broad when compared to the literature on materials tested for multi-bit storage [11, 15, 16] suggesting that the GeTe/SnSe sample tested in 2009 would most likely not be a very good candidate for multi-bit storage unless other pulse conditions could be found that would increase the resistance distribution separation. This was also evident in the majority of the IV traces for the GeTe/SnTe Layered devices, commonly having only one snap-back (Figure 5.4). It is possible that this is a result of the wafer edge location and thinner material sidewall at which the GeTe/SnTe devices were tested, as discussed in Section 5.1.

5.2.4.4 Cycling: GeTe/SnTe

Once the RESET / SET pulses were selected, cycling tests were performed on multiple bits to gain additional understanding of the effects of possible Sn-ion and Te-ion migration into the Ge-chalcogenide layer. Each bit was cycled up to 300 times with the optimized RESET/SET pulses, using the pattern represented in Figure 4.13.

In Figure 5.16 a representation of the GeTe/SnTe layered structure after 100 cycles is shown in order to demonstrate the ability of the B1500A to capture the device response to each cycle.

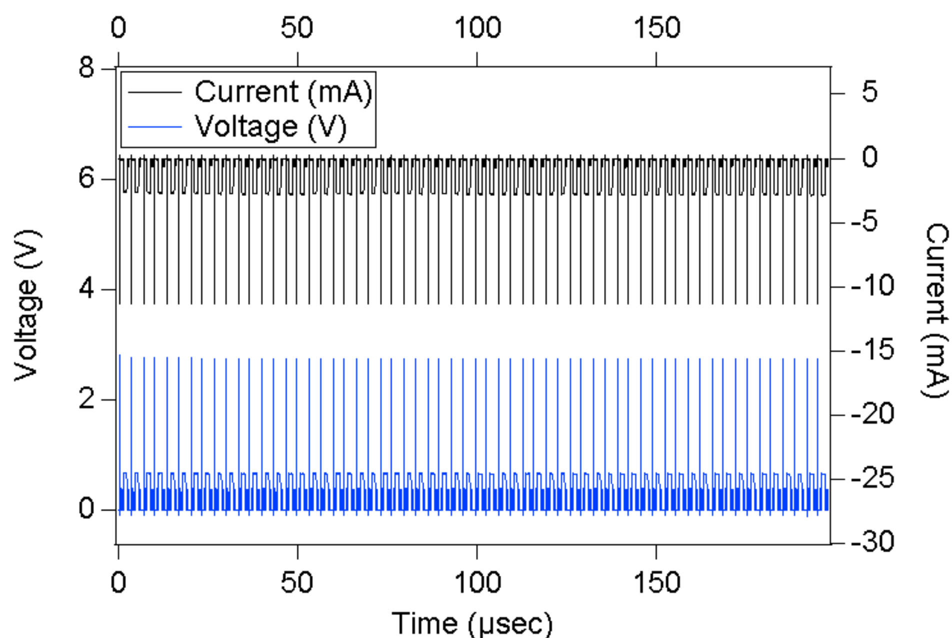


Figure 5.16: Representative pulse trace for the GeTe/SnTe device being cycled 100 times. The input pulse is shown in blue (bottom trace) and the device response is shown in black (top trace).

One can see based on the current trace that the amplitude of the current is somewhat similar. This was not found on all GeTe/SnTe bits but was seen on the majority of the bits tested. However, when comparing the RESET and SET resistance values from the cycling tests as shown in Table 5.6, it was found that a significant change occurs between 20 cycles and 100 cycles for the RESET and SET resistances. It should also be noted that a significant drop in the RESET resistances was also seen after 300 cycles. This is an indication that the cycling conditions selected for the RESET are not optimized.

Table 5.6: Numerical data form cycling tests performed on the GeTe/SnTe device.

Device:	Cycles	Resistance (Ω) - RESET	Resistance (Ω) -SET
GeTe/SnTe	20	2×10^4	1×10^3
	100	1×10^4	7×10^2
	300	6×10^3	7×10^2

5.3 Conclusion

In summary, the electrical characterization of Layered structures fabricated at Micron Technology have been successfully cycled using a system capable of measuring the device response during pulse testing. These measurements do not have an impedance mismatch issue due to the use of the B1500A and the built in circuitry in the B1530A and RSUs which account for the dynamic resistance changes. Current-voltage traces were collected and pulse testing was performed to determine the multi-state properties of the Layered structures. From the IV traces for the Layered devices, lower resistances were found after the initial snap-back when compared to the Ternary samples. Moreover, the

presence of multiple snap-back regions on all samples was not as apparent as was seen for the Ternary samples. However, multiple non-overlapping resistance distributions were found for all Layered devices, indicating the possibility of multi-state storage similar to the Ternary devices. Moreover, bit-to-bit variation similar to the Ternary samples was seen on all Layered devices for the threshold voltage. For the performance of the Layered structures when compared to the GST device, it was found that the Ge_2Se_3/SnTe and Ge_2Se_3/SnSe Layered structures had a large improvement in the current requirements when compared to the GST device, the GeTe/SnTe showing a large improvement in the voltage requirements when compared to the GST device.

Pulse tests were performed on the Layered samples to gain additional insight into the possibility of multiple resistance states and the effects of possible Sn-ion and Te-ion migration into the Ge-chalcogenide layer (as the material is cycled). With the pulse programming conditions used, multi-level resistance values were not found for the GeTe/SnTe Layered device. This is not unexpected since to achieve multiple resistance states, the right programming conditions for each state need to be determined. A comparison of the RESET and SET resistance values from the cycling tests showed that a significant change in resistance occurs between 20 cycles and 100 cycles for the RESET and SET resistance.

CHAPTER 6: CONCLUSION

6.1 Introduction

The electrical characterization results of the Ternary and Layered devices is summarized in this chapter. In conclusion, the benefits of the Ternary versus Layered structures is presented, followed by a discussion of the remaining issues that limit their performance.

6.2 Summary of Work

6.2.1 Ternary Materials

In review, there were several reasons found for investigating the 3% Ternary devices: (1) To investigate the electrical performance differences resulting from the expected difference in chemical incorporation into the Ge-chalcogenide glass layer [7]; (2) To electrically explore the crystallization regions seen in the DSC traces, and (3) To find new forms of possible multi-state memory devices and gain understanding of the chemical incorporation into the Ge_2Se_3 chalcogenide material.

6.2.2 Layered Structures

In review of the Layered structures, the objective was (1) To improve adhesion to the electrode and reduce the voltages, currents, and switching speeds needed for phase-change memory operation without the need for a complicated physical device structure [7]; (2) To explore the possibility of multi-state behavior as was previously published for the device [7] and (3) To perform cycling tests to explore the effects of possible Sn-ion and Te-ion migration into the Ge-chalcogenide layer.

6.3 Ternary Device Performance

In summary, from the IV traces only one apparent snap-back region was found on each of the Ternary samples. Center, middle, and edge wafer measurements were conducted, finding resistance distribution patterns when comparing the 10 µA, 100 µA and 1mA SET resistances, showing three distinct resistance distributions on all Ternary samples excluding the 3%Sn sample due to variations in the SET resistance at the wafer edge, indicating possible multi-state storage. TEM cross-section images were collected at the location between the wafer center and middle of the wafer. From the TEM images it was found that the Ternary devices have an unwanted etch region in the nitride adjacent to the via, which contributes to a thinner chalcogenide material at the via edges. TEM images will be collected for further investigation into Ternary wafers with isolated bottom electrodes to see if the unwanted etch region has been fixed with the most recent isolated bottom electrode process.

Standard DC current sweep tests were performed by sweeping the current to either 100 µA or 1 mA with step increments that varied depending upon the maximum current setting. With increased resolution a more defined threshold voltage for the Ternary devices were found. Additional current sweeps with the potential reversed on the top electrode were performed with programming currents of 100 µA. Similar variations were again found when comparing the threshold voltage/current with opposite potentials applied to the top W electrode.

When reviewing the performance of the Ternary devices to the GST device fabricated at Micron Technology, a large improvement in the current requirements for the

Ternary devices was found; all Ternary devices showed threshold currents of an order of magnitude less than that of the GST device. However, the threshold voltage and SET resistance for the GST device was found to be lower than that of the Ternary devices

When performing the pulse tests, it was found that devices fabricated with a common bottom electrode exhibited too much capacitance to perform the pulse test measurements. Devices with isolated bottom electrodes were subsequently fabricated at BSU which did not exhibit the capacitance preventing pulse testing.

6.4 Layered Device Performance

When comparing the IV traces for the Layered devices to those of the Ternary devices, lower resistances were found. However, bit-to-bit variation similar to the Ternary samples was measured on all Layered devices for the threshold voltage. Multiple resistance distributions were measured for all Layered devices indicating the possibility of multiple resistance states, however, the stability of the resistance states was not found during the cycling tests. TEM cross-section images were collected showing reduced step coverage over the sidewalls of the via (similar to the BSU samples), resulting in a possible thinner active region at the side wall of the via for the Ternary and Layered devices. Performance improvements were found when comparing the Layered structures to a GST device fabricated at Micron Technology, showing the Ge_2Se_3/SnTe and Ge_2Se_3/SnSe Layered structures to have a large improvement in the current requirements when compared to the GST device, the GeTe/SnTe showing a large improvement in the voltage requirements when compared to the GST device.

Pulse tests were performed on the Layered samples to gain additional insight into the possibility of multiple resistance states and the effects of possible Sn-ion and Te-ion migration into the Ge-chalcogenide layer (as the material is cycled). With the pulse programming conditions used, multi-level resistance values were not found for the GeTe/SnTe Layered device. This was not unexpected since to achieve multiple resistance states, the right programming conditions for each state need to be determined. A comparison of the RESET and SET resistance values from the cycling tests showed that a significant change in resistance occurs between 20 cycles and 100 cycles for the RESET and SET resistance (Table 5.6). With additional variation in the RESET pulse as the GeTe/SnTe device continues to be cycled, indicating that the RESET pulse is not optimized.

6.5 Outstanding Problems

Several outstanding problems were found when performing the electrical tests on the Ternary and Layered devices. For the Ternary devices, the common bottom electrode created capacitance issues precluding pulse measurements. This was just recently resolved after testing new Ternary structures with isolated bottom electrodes. However, due to the capacitance issues found, pulse tests and cycling testes were not completed, limiting the amount of information that could be gained on the stability of multiple resistance states. It would be beneficial to have additional Ternary devices made of the 3% Zn, Sn, Sb, and In compositions to further explore the possibility of stable multi-resistance states for the Ternary devices.

For both the Ternary and Layered devices, nitride variations were found near the via edge, showing reduced step coverage at the sidewall of the via; possibly changing the location of the active region of the devices. Furthermore, when performing the electrical IV and electrical pulse tests, variations in the threshold current/voltage and resistance values were found.

6.6 Future Work

Thus, in addressing the outstanding problems mentioned in the previous section, we have a clear path for our future work: (1) To create Ternary devices with isolated bottom electrodes, with thicknesses of 450 Å to match the samples tested in this thesis and to further test the possibility of stable multi-resistance states; (2) To perform structural changes in the shape of the via, improving the shape by implementing a smoother contour and smaller slope at the step; improving the step coverage; (3) To look into improved methods to reduce the nitride thickness variation seen between the center and edge of the wafer (see on the Layered device) and at the via edge (seen on the Ternary device); (4) To perform pulse tests on the Layered and Ternary devices using a pulse generator capable of generating pulse widths below 30ns, with rise/fall times below 10ns, to see if an optimal RESET pulse can be determined.

These modifications to the structures and electrical measurement methods should improve the stability and performance of the devices being tested. Further benefits could be seen in the possibility of stable multi-resistance states for the Ternary and Layered devices, addressing some of the uncertainty of the volume of the programmed material and how the device will perform.

6.7 Summary

In conclusion, there are four points that we have developed in the course of this work:

1. We have identified that the 3% Ternary devices and Layered structures are viable candidates for multi-state PCRAM devices.
2. We have developed a working fabrication process, uncovering a number of processing issues. These process issues being discovered as a result of the electrical tests which were performed on the devices. We discovered: (1) Capacitance issues due to the use of a common bottom electrode on the original Ternary fabrication process, which was confirmed after testing the Ternary devices with the patterned bottom electrode; (2) Step coverage issues, due to the shape and the slope of the via step and nitride thickness variations at the via edge; and (3) Limitations were found with the B1500A and B1530, when performing electrical pulse measurements for the Layered devices, indicating that an optimal RESET pulse would require a pulse width of less than 30 ns; which the B1530A is incapable of reaching.
3. In operation, the Ternary structures were found to have similar threshold switching voltages when compared to the Layered structures (excluding GeTe/SnTe). Additionally, both the Ternary and Layered devices were found to have a large improvement in the current requirements when compared to the GST device tested (excluding the GeTe/SnTe device). However the GeTe/SnTe device

was found to show a large improvement in the voltage requirements when compared to the GST device.

4. Cycling of the GeTe/SnTe was performed up to 300 cycles, showing the largest cycling effect after 20 cycles. RESET values were found to continue to drop up to 300 cycles indicating the RESET pulse created is not optimized.

With this knowledge, we can continue to develop and explore the Ternary and Layered phase change devices, to further explore the possibility of new multi-resistance state materials for PCRAM.

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