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Gain Error Correction for CMOS Image Sensor using Delta-Sigma Modulation

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Abstract – A delta-sigma modulation analog-to-digital converter (ADC) has many benefits over the use of a pipeline ADC in a CMOS image sensor. This includes lower power, noise reduction, ease of maximizing the input range, and simpler signal routing for large arrays. Multiple delta-sigma modulation ADC is required in a CMOS image sensor, one for each pixel column. Any voltage threshold mismatch between ADCs will introduce gain and offset error in its transfer function, which will lead to fix pattern noise. Correcting these gain and offset error for every ADCs in the image sensor will require a complex digital signal processor. Therefore, a technique to minimize the effects of gain error in a delta-sigma modulation ADC for CMOS image sensor is discussed.

***Keywords – Delta-Sigma Modulator, DSM, clocked comparator, 4 phase non-overlapping clock, CMOS Image Sensor ADC*.**

I. INTRODUCTION

The pipeline analog-to-digital converter (ADC) is usually used in today's CMOS image sensors to convert the analog pixel integration voltage to a digital code [1]. There may be one pipeline ADC in a CMOS image sensor that converts the color of each color pixel in the array: green, blue and red. As the pixel density in the CMOS image sensor increases, or the level of color quality increases, the pipeline ADC will require a larger layout area and consume more power. Furthermore, as the size and density of the CMOS image sensor increases, coupled noise and voltage variation from the long distance required to route the signal between pixel and the pipeline ADC becomes an issue.

A per column delta-sigma modulation (DSM) ADC sensing circuit was introduced as a potential solution to the problem [1]. A per column DSM ADC is susceptible to fixed pattern noise due to voltage threshold mismatch between adjacent DSM ADCs in the array. Voltage threshold mismatch causes offset and gain error in its transfer function.

Path switching was introduced as a method to reduce the effects of offset error in a per column DSM ADC [1], [2]. This paper will introduce a technique to help reduce the effects of gain error in a per column DSM ADC.

II. DELTA-SIGMA MODULATION ADC SENSING OPERATION IN A CMOS IMAGE SENSOR

Fig. 1 illustrates the sensing scheme used by a DSM in a CMOS image sensor. There is one DSM for each column of pixels and the sensing occurs in parallel for each column.

The sensing scheme begins with sampling the pixel's reset signal onto the reset sample and hold capacitor, C_{HR}. This is accomplished by turning on the rowline and ResetN signals on one of the multiple rows of pixels in the array. Each pixel on the activated row will output its reset signal onto its respective column line. This reset signal is then sampled onto the C_{HR} capacitor through the activated SHR switch. Once the reset signal is sampled, the rowline, ResetN, and SHR switch is turned off.

After the reset signal is sampled, the pixel is then exposed to light for a length of time. Once the exposure time has expired, the same rowline and SHI switch is turned on. This samples the image signal onto the image sample and hold capacitor, C_{HI}. The rowline and SHI switch is turned off once the image signal is sampled onto C_{HI}.

Next, the DSM will take the reset and image input signals that were sampled on the two capacitors and convert them to a digital code equivalent. The n-bit wide counter that is connected at the end of the DSM converts the digital output of the DSM into an n-bit wide digital code.

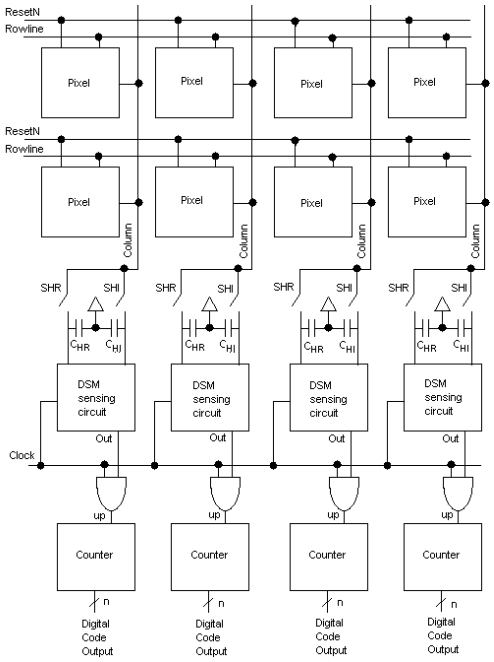

Figure 1. A typical 2x4 pixel diagram of a CMOS image sensor using DSM ADC [3].

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III. A Delta-Sigma Modulation ADC without offset and gain error correction

The basic DSM sensing circuit without any offset and gain error correction is seen in Fig. 2. It measures the difference between the two analog input signals, V_{RESET} and V_{IMAGE} with respect to a single reference input signal, V_{REF}. The DSM is clocked for N times over the entire sensing period. A simple two phase non-overlapping clock is required, where PHI1B is the inverse of the first phase and PHI2B is the inverse of the second phase. Its frequency is equal to the rate of the master clock denoted as f_{PHI}.

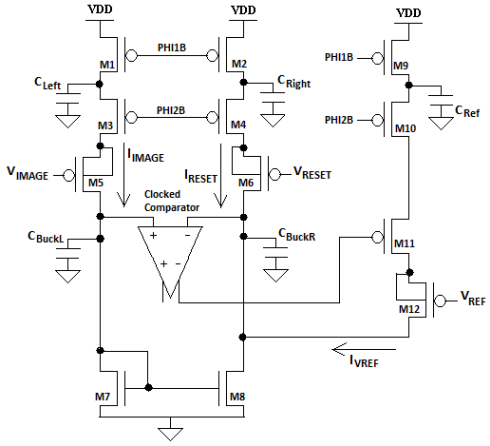

Figure 2. DSM ADC without gain and offset error correction circuitry.

At the end of the first phase of the clock, the clock comparator in the DSM measures the voltages on capacitor C_{BUCKL} and C_{BUCKR} and turns on M11 for the subsequent phase if the voltage on C_{BUCKR} is lower than the voltage on C_{BUCKL}. This occurs for M times over the entire sensing period.

During the first phase of the clock, C_{LEFT}, C_{RIGHT}, and C_{REFf} are set to VDD. On the next phase of the clock, the image current, I_{IMAGE} and reset current, I_{RESET} flows into C_{BUCKL} and C_{BUCKR} respectively.

$$I_{IMAGE} = C_{LEFT} f_{PHI}\left(VDD - V_{IMAGE} - V_{th,M5}\right) \quad (1)$$

$$I_{RESET} = C_{RIGHT} f_{PHI}\left(VDD - V_{RESET} - V_{th,M6}\right) \quad (2)$$

$V_{th,M5}$ and $V_{th,M6}$ is the threshold voltage of M5 and M6. If M11 is turned on, a reference current, I_{VREF} will flow into C_{BUCKR} and its magnitude average over the whole sensing period is

$$I_{VREF1} = \frac{M}{N} C_{REF} f_{PHI}\left(VDD - V_{REF} - V_{th,M12}\right) \quad (3)$$

$V_{th,M12}$ is the threshold voltage of M12.

The digital code representation of the analog input signals with respect to the reference signal can be found by summing the current into the C_{BUCKR} capacitor.

$$M = N\left(\frac{C_{LEFT}(VDD - V_{IMAGE} - V_{th,M5}) - C_{RIGHT}(VDD - V_{RESET} - V_{th,M6})}{C_{REF}(VDD - V_{REF} - V_{th,M12})}\right) \quad (4)$$

The input-output transfer function of this DSM is prone offset and gain error if voltage threshold mismatches exist between the many DSM ADCs in the array. If a voltage threshold mismatch on M5 and M6 exist, an offset error will occur. On the other hand if a voltage threshold mismatch on M12 exist, a gain error will occur. Therefore, CMOS image sensor that uses this DSM will be susceptible to fixed pattern noise because the transfer functions between the many DSM ADCs in the array will be different.

IV. Delta-Sigma Modulation ADC with gain error correction

As mentioned earlier, a per column DSM ADC with path switching was introduced to reduce the effects of offset error [1]. A DSM sensing circuit with gain error correction is shown in Fig. 3. This DSM measures the difference between the two analog input signals, V_{RESET} and V_{SIGNAL} with respect to two reference input signals, V_{REF1} and V_{REF2} instead. The DSM is also clocked for N times over the entire sensing period.

A 4-phase non-overlapping clock signal is required for this design, Fig. 4. The PHI1, PHI2, PHI3, and PHI4 signals are the four non-overlapping clock phases and its complement signals are PHI1B, PHI2B, PHI3B, and PHI4B. Its frequency is 1/4th the rate of the master clock denoted as f_{PHI}.

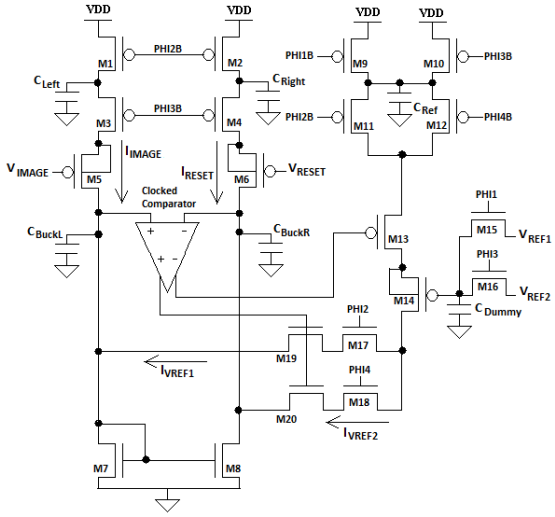

Figure 3. DSM ADC with gain error correction circuitry.

The clock comparator in this DSM also measures the voltages on capacitor C_{BUCKL} and C_{BUCKR} at the end of the first phase of the clock but it turns on M13, M19 and M20 for the remaining three clock phases instead if the voltage on C_{BUCKR} is lower than the voltage on C_{BUCKL}. The clock comparator turns on M13, M19 and M20 for M times over the entire sensing period.

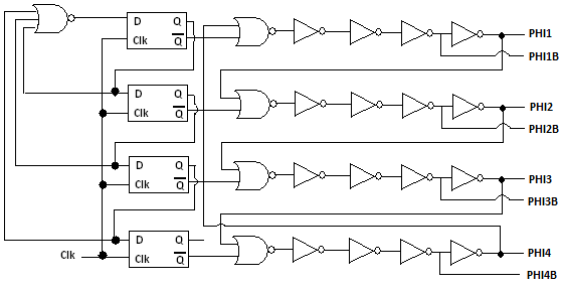

Figure 4. A schematic diagram that shows the 4 non-overlapping clock phases.

A dummy capacitor C_{DUMMY} is added to the gate of M14 as a mean to reduce the effects of charge injection and clock feed-through when PHI1 and PHI3 signals transitions from high to low. The reference signal voltages needs to be on the gate of M14 a phase earlier and stays unchanged for the whole duration of the subsequent phase. This is to prevent any error in the magnitude of the two reference current, I_{VREF1} and I_{VREF2}.

During the first phase of the clock signal, M9 turns on and sets the voltage on C_{REF} to VDD. At the same time, M15 turns on and allows the reference signal V_{REF1} to propagate to the gate of M14.

On the next phase of the clock, M11 turns on and the first reference current, I_{VREF1} will flow from C_{REF} to C_{BUCKL} if M13, M17 and M18 is turned on by the comparator. The average reference current that flows into C_{BUCKL} is

$$I_{VREF1} = \frac{M}{N} C_{REF} \frac{f_{PHI}}{4} \left(VDD - V_{REF1} - V_{th,M14}\right) \quad (5)$$

$V_{th,M14}$ is the threshold voltage of M14. On the same clock phase, the voltage on C_{LEFT} and C_{RIGHT} are set to VDD.

On the third phase of the clock, C_{REF} is force to VDD and the second reference voltage signal, V_{REF2} is propagated to the gate M14. During this phase, the image current, I_{IMAGE} and reset current, I_{RESET} will flow to C_{BUCKL} and C_{BUCKR} respectively.

$$I_{IMAGE} = C_{LEFT} \frac{f_{PHI}}{4} \left(VDD - V_{IMAGE} - V_{th,M5}\right) \quad (6)$$

$$I_{RESET} = C_{RIGHT} \frac{f_{PHI}}{4} \left(VDD - V_{RESET} - V_{th,M6}\right) \quad (7)$$

On the last phase of the clock, the second reference current, I_{VREF2} will flow from C_{REF} to C_{BUCKR} if M13, M17 and M18 remains on. The average reference current that flows into C_{BUCKR} is

$$I_{VREF2} = \frac{M}{N} C_{REF} \frac{f_{PHI}}{4} \left(VDD - V_{REF2} - V_{th,M14}\right) \quad (8)$$

Over N clocked cycles, the sum of current into C_{BUCKR} is ideally zero and the digital relationship between the analog input signals with respect to the reference signals is

$$M = N \left(\frac{C_{LEFT}(VDD - V_{IMAGE} - V_{th,M5}) - C_{RIGHT}(VDD - V_{RESET} - V_{th,M6})}{C_{REF}(V_{REF1} - V_{REF2})}\right) \quad (9)$$

The transfer function for this DSM shows that it is robust to any gain error cause by voltage threshold mismatch. This is because the denominator of the transfer function does not contain the voltage threshold of any transistor in the DSM. The gain of the DSM is controlled by the two reference voltage signals, V_{REF1} and V_{REF2}. The difference between V_{REF1} and V_{REF2} determines the gain of the DSM.

However, this DSM is prone to offset error as the nominator of the transfer function contains the voltage threshold of M5 and M6. Path switching methodology can be applied to this DSM to reduce the effects of offset error [1]. Fig. 5 illustrated the DSM with both offset and gain error correction.

The sensing period of the DSM is now divided into 2 equal halves. Each halves is N/2 clock cycles long. On the first half of the sensing period, control signals SLT and SLB is set to VDD and VSS respectively. During this sensing period, the digital code representation of the analog input signals with respect to the two reference input signals, $M_{t=1}$ is

$$M_{t=1} = \frac{N}{2} \left(\frac{C_{LEFT}(VDD - V_{IMAGE} - V_{th,M5}) - C_{RIGHT}(VDD - V_{RESET} - V_{th,M6})}{C_{REF}(V_{REF1} - V_{REF2})}\right) \quad (10)$$

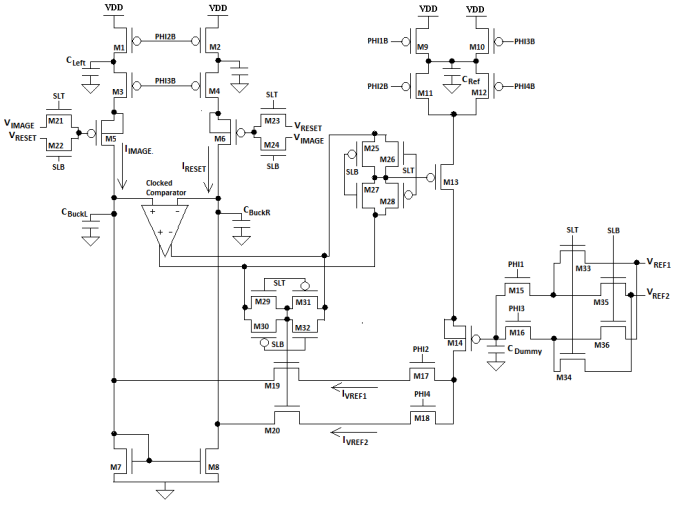

Figure 5. DSM ADC with gain and offset error correction.

On the next half of the sensing period, the controls signals SLT and SLB is set to VSS and VDD respectively. The digital code representation of the analog input signals with respect to the two reference input signals for the second half of the sensing period, $M_{t=2}$ is

$$M_{t=2} = \frac{N}{2} \left(\frac{C_{RIGHT}(VDD - V_{IMAGE} - V_{th,M6}) - C_{LEFT}(VDD - V_{RESET} - V_{th,M5})}{C_{REF}(V_{REF1} - V_{REF2})}\right) \quad (11)$$

At the end of the sensing period, the digital output code for the two halves of the sensing period is added together and the final digital output code for the DSM with both gain and offset correction is

$$M_{t=1} + M_{t=2} = \frac{N}{2} \left(\frac{(C_{LEFT} + C_{RIGHT})(V_{RESET} - V_{IMAGE})}{C_{REF}(V_{REF1} - V_{REF2})}\right) \quad (12)$$

The input-output transfer function of this DSM does not contain the voltage threshold of any transistor in the DSM. This means that the DSM is robust to any offset or gain error cause by voltage threshold mismatches. However, a gain error might still occur if the capacitor ratio between the sum of C_{LEFT} and C_{RIGHT} and C_{REF} is not identical between the many DSMs in the array.

The least significant bit voltage, V_{LSB} for the DSM with both offset and gain error correction can be approximated by

$$V_{LSB} = \frac{1}{N} \left(\frac{C_{REF}}{(C_{LEFT} + C_{RIGHT})}\right) \left(\frac{2}{(V_{REF1} - V_{REF2})}\right) \quad (13)$$

The bit accuracy increases linearly with the number of clock cycles, N during the sensing period.

V. SIMULATION

A voltage source was added in series with the gate of a transistor to simulate a variation in its threshold voltage. A simulation is ran on the DSM without offset and gain error correction like in Fig. 2. A voltage threshold offset on M5

causes the transfer to either shift upwards or downwards from ideal and it is known as offset error. A negative offset on M5 causes the curve to shift upwards and vice-versa. On the other hand, a voltage threshold offset on M12 causes the slope of the transfer function to either increase or decrease from ideal and this is gain error. A negative offset on M12 decreases the slope.

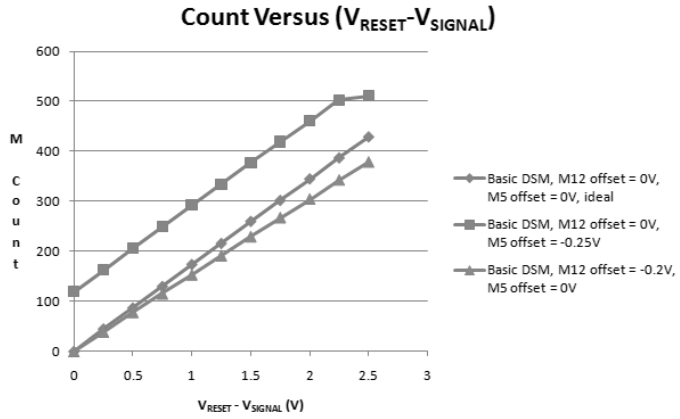

Figure 6. Simulation results for the DSM without offset and gain error correction. Different voltage offsets are applied to M5 and M12.

A simulation was run on the DSM with only gain error correction. Voltage offsets is placed in series with the gate of M14 to simulate voltage threshold variation that leads to gain error in its transfer function. Fig. 7 shows that the slope of the transfer function for this DSM does not change with different offsets on M13.

A 0.25V voltage offset was added in series with the gate of M5 and its transfer function is shifted downwards from ideal. As expected, the DSM with only gain error correction is susceptible to offset error.

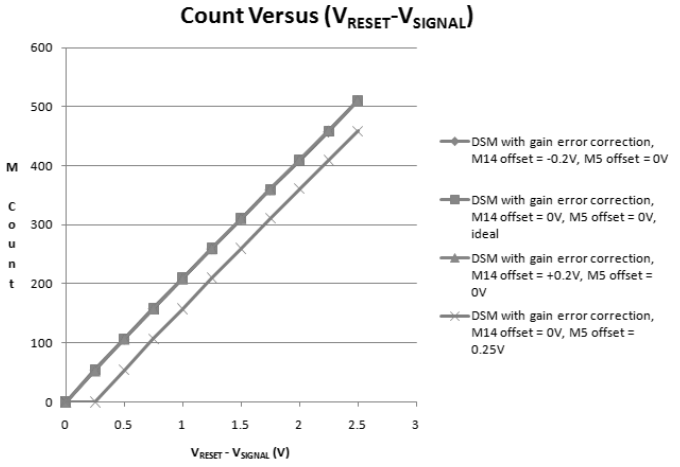

Figure 7. Simulation results for the DSM with only gain error correction. Different voltage offsets are applied to M5 and M14.

Fig. 8 shows that the DSM with both offset and gain error correction is robust to offset and gain error. Voltage offsets was added in series with the gate M14 and M5 to simulate gain and offset error. The transfer function with both voltage offsets looks identical to the transfer function of an ideal DSM except for the front and tail end. The magnitude of the deviation is equal to the amount of voltage offset applied to the gate of M5. This means the DSM input dynamic range is reduced by 0.5V or twice the amount of voltage threshold mismatch on M5.

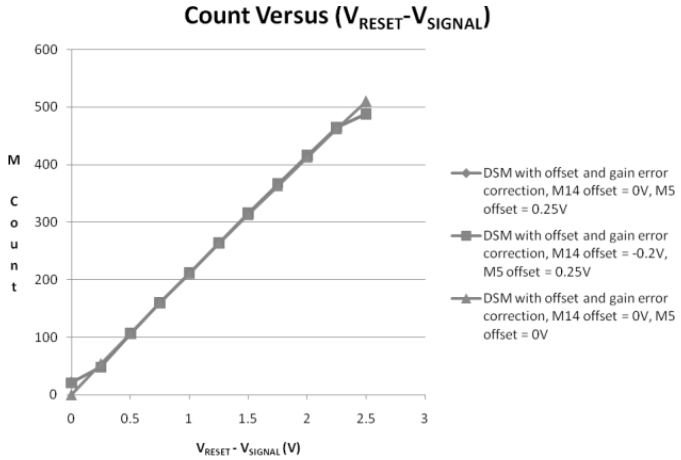

Figure 8. Simulation results for the DSM with both offset gain error correction. Different voltage offsets are applied to M5 and M14.

VI. Summary and Conclusions

The DSM proposed is robust to any voltage threshold mismatch that causes gain error. Path switching technique can be applied to this DSM which will cancel both offset and gain error. This will further reduce fixed pattern noise in a CMOS image sensor using per column DSM ADC because the transfer function of every DSM ADCs in the array will be closely match.

Acknowledgment

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