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Synthesis of Higher-Order K-Delta-1-Sigma Modulators for Wideband ADCs

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***Abstract*—As CMOS technology shrinks, the transistor speed increases enabling higher speed communications and more complex systems. These benefits come at the cost of decreasing inherent device gain, increased transistor leakage currents and device mismatches due to process variations. All of these drawbacks affect the design of high-resolution analog-to-digital converters (ADCs) in nano-CMOS processes. To move towards an ADC topology useful in nano-CMOS, the K-Delta-1-Sigma (KD1S) modulator-based ADC was proposed. This paper extends the KD1S to higher order topologies using a systematic synthesis procedure. Second and third order KD1S modulator are designed and simulated to demonstrate the synthesis method.**

***Index Terms*—Analog to digital converter, delta-sigma modulation, interleaved data converters, noise-shaping, parallel delta-sigma, wideband ADC.**

I. Introduction

CONTINUED CMOS scaling has enabled ever increasing device speeds leading to numerous standards in wireless and wireline segments. The integrated circuit technologies used to manufacture analog-to-digital converters (ADCs) are shrinking to include more system functionality in a smaller chip area. This reduction in size comes at the cost of pronounced manufacturing variances, including circuit (transistor) characteristics, which limit the availability of precise components often required in an ADC. In order to design high-resolution wideband ADCs in nano-CMOS with significant device variances, complex digital calibration algorithms are required at the cost of area and power consumption. Thus investigating novel ADC topologies which are inherently tolerant to device mismatches and nonlinearity is desirable [1].

It is known that the oversampling or delta-sigma ADCs trade sampling frequency with the signal bandwidth to achieve much higher signal-to-noise ratio (SNR). A delta-sigma ADC constitutes of a delta-sigma modulator (DSM) followed by digital filters and decimation stages [1]. The modulator employs oversampling, i.e. the sampling frequency is a multiple of the input signal bandwidth, defined as the oversampling ratio (OSR). The DSM loop shapes the quantization noise, Q_e, and moves it to higher frequency away from the baseband signal bandwidth. The noise-shaping results in lower quantization noise in the signal bandwidth and the modulated noise can be filtered out digitally leading to significantly higher SNR. Thus, much of the analog signal processing is transferred to the digital domain which is favorable for continued CMOS scaling. The delta-sigma feedback loop is insensitive to device mismatches and nonlinearity in the forward path due to the high loop gain at the lower frequencies. However, due to oversampling the delta-sigma ADCs are narrow-band and the signal bandwidth is limited to $BW \leq f_s/(2{\cdot}OSR)$. Therefore, the traditional delta-sigma ADCs can not achieve Nyquist-rate sampling as desired for wideband data conversion. Also time-interleaving of K delta-sigma modulators in parallel does not result in true wideband noise-shaping [2].

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II. The K-Delta-1-Sigma Modulator

A new topology called the K-Delta-1-Sigma (KD1S) was introduced in [1] to achieve wideband noise-shaping using a switched-capacitor implementation. The KD1S, shown in Fig. 1, employs K time-interleaved sampling paths with a shared integrator [2]. Here, the KD1S modulator is clocked by K-phases of a clock with a rate equal to f_s. The effective sampling rate of the modulator is set by the spacing between the edges of the clock phases and is given as

$$f_{s,new} = K_{path} \cdot f_s \tag{1}$$

The summing of the K-path outputs, $y_k[n]$, $k = 0, 1, .., (K–1)$, using a fast adder leads to a path filter response of $(1–z^{-K})/(1–z^{-1})$, which acts as a decimation filter. Here, the input sampling phase for a path lasts for T_s/K_{path} time while the integrating phase has duration equal to $T_s/2$. As we can observe the integrator is connected to $K_{path}/2$ distinct paths at any given time, and thus spreading the sampled input signal across $K_{path}/2$ paths.

Since a single op-amp is shared across all the K paths, the forward path mismatches are minimized. The offsets of each of the comparators are desensitized by the large loop gain. It is also expected that the spreading of signal across the K-paths will average out the mismatch effects in the feedback paths. In order to achieve true first-order noise-shaping, the comparator in each of the paths must fully respond to the partial settling of the integrator within $T_s/(2K_{path})$ time interval. In other words, the quantization noise in the modulator is differentiated in every T_s/K_{path} time-slice. The noise transfer spectrum for the KD1S modulator is shown in Fig. 2 and compared with the noise-shaping of a parallel DSM. Here, the quantization noise is pushed out to frequencies as high as $K_{path} \cdot fs/2$ and thus achieving noise-shaping similar to a first-order delta-sigma modulator operating with a $K_{path} \cdot fs$ clock rate. The the KD1S topology seen in Fig. 1 achieves a 1.5 bit gain in resolution per doubling in the number of paths. In other words, doubling of the number of paths has the same effect as doubling the OSR.

The K-path Switched-Capacitor Integrator (K-SCI)

In a discrete-time realization of delta-sigma modulator, using switched-capacitor circuits, the maximum attainable over-

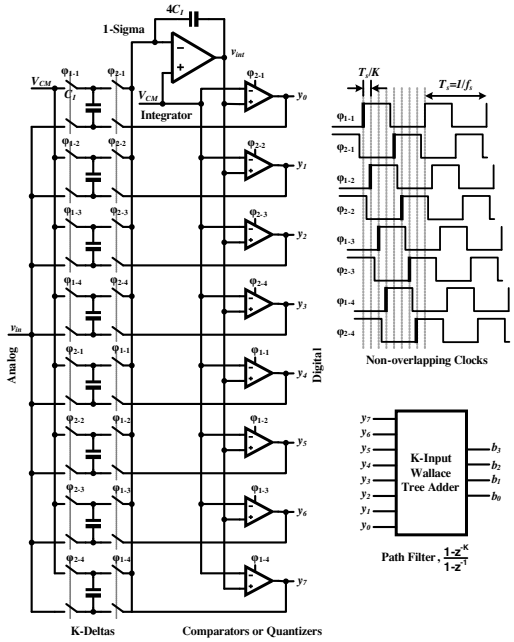

Figure 1. The K-Delta-1-Sigma modulator topology.

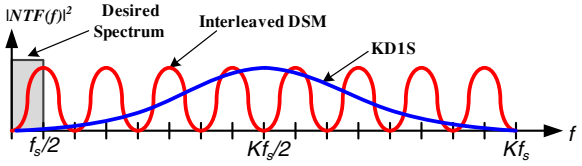

Figure 2. True wideband noise-shaping using a K-Delta-1-Sigma Modulator.

sampling clock rate is limited by the op-amp settling requirements. The op-amp settling error increases exponentially with a decrease in f_{un}/f_s ratio. The K-path switched-capacitor integrator increases the sampling rate of the conventional SC Integrator by K times, without any increase in op-amp settling requirements. In this integrator, for each of the switched-capacitor the sampling and the integrating phases last for a time interval equal to $T_s/2$, i.e. half the clock period. Here, the unity-gain frequency, f_{un}, of the op-amp can be as low as $3f_s$. The discrete-time dynamics of the SC K-path Integrator can be understood as follows. The input signal for a path is sampled on the falling edges of the 8-phase clock (say $\phi_{1-1}$for the first path). This is followed by the rising edge of the phase ϕ_{2-1}, when the capacitor (C_I) with the charge proportional to the sampled input is connected to the integrator. Note that, at a particular instance four (i.e. $K_{path}/2$) sampling capacitors are connected to the integrator through the switches. Now, if the time interval between the rising edges of the 8-phase clock is much larger than the switched-capacitor charging time, charge sharing will occur amongst the four capacitors connected to the integrator's input node (v_x). After charge sharing, the integrator's output will move corresponding to the initial-push delivered by the partial settling of the integrator. The charge spreading effects are illustrated in Fig. 3.

The equivalent transfer function for the K-path integrator

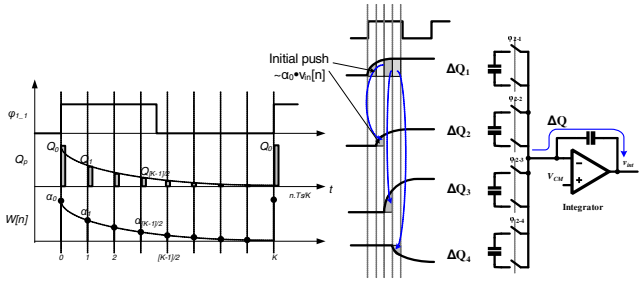

Figure 3. Illustration of charge-spreading and the equivalent filtering action in a K-path SCI.

has been derived to be equal to

$$H_1(z) = \frac{C_I}{C_F}\frac{z^{-1}}{1-z^{-1}}\frac{1-\alpha_0}{1-\gamma_0 z^{-1}} \tag{2}$$

where the op-amp settling factor $\alpha_0 = e^{-\pi\beta\frac{f_{un}}{K_{path}f_s}}$ and the additional pole location is given as $\gamma_0 = \left(\frac{\frac{K}{2}-1}{\frac{K}{2}}\right)\alpha_0$. This is equivalent to an ideal discrete-time integrator response being convolved with a filter given by the transfer function

$$W(z) = \frac{1-\alpha_0}{1-\gamma_0 z^{-1}} \tag{3}$$

III. Synthesis Procedure for KD1S Modulators

The KD1S concept can be extended to design higher order noise-shaping modulators. An efficient method to design higher-order traditional single-path DSMs is by utilizing the popular Delta-Sigma Toolbox in MATLAB [3]. This toolbox internally uses ABCD matrix to design the DSM loop filter and for dynamic range scaling and modulator simulation. The ABCD matrix is a combination of four matrices which describe the dynamics of any discrete-time linear system. The state-space equations for the DSM loop filter are described as

$$\begin{aligned} \mathbf{x}[n+1] &= A\mathbf{x}[n] + B\begin{bmatrix} u[n] \\ v[n] \end{bmatrix} \\ \mathbf{y}[n] &= C\mathbf{x}[n] + D\begin{bmatrix} u[n] \\ v[n] \end{bmatrix} \end{aligned} \tag{4}$$

where $\mathbf{x}(n) \in R^{M\times 1}$ is the state vector at time n for an M^{th}-order modulator. The matrix $A \in R^{M\times M}$ defines the interconnections withing the loop filter. The matrix $B \in R^{M\times 2}$ describes how the modulator input $u[n]$ and the feedback DAC output $v[n]$ are applied to the loop filter $H(z)$. The matrices $C \in R^{1\times M}$ and $D \in R^{1\times 2}$ describe the computation of the output $y[n]$ from the states $\mathbf{x}[n]$ and the loop filter inputs $(\ u[n] \quad v[n]\ )^T$ [4].

The KD1S modulator can be designed by appropriately modifying an equivalent single-path DSM and by incorporating the analytical results for the K-path switched-capacitor integrator (K-SCI). It can be observed that in a KD1S modulator, there is always a delay of T_s/K_{path} time-slice (or z^{-1} delay for $K_{path}f_s$ clock rate). Due to this, the KD1S modulator can only be realized by using the **CIFB** (Cascade of integrators, feedback form) and **CIFF** (Cascade of integrators, feedforward form) topologies [4]. Now, we need to account for

the charge-spreading filter in the K-SCIs used in the modulator . This problem is analogous to the simulation of continuous-time (CT) DSMs where op-amp non-idealities are an important concern. A 'lifting' method has been devised for continuous-time state-space of the CT-DSMs in [5]. This method has been customized to the discrete-time case of KD1S to incorporate the non-idealities (i.e. the additional pole at $z = \gamma_0$ and gain scaling by $(1 - \alpha_0)$) of the K-SCI.

Let's say that the input to all the integrators in the DSM loop-filter is $\mathbf{P}[n]$ and the output of all the integrators is $\mathbf{O}[n]$. This changes the state-space representation of the loop-filter to

$$\begin{aligned} \mathbf{P}[n] &= \mathbf{x}[n+1] - \mathbf{x}[n] = (A - I)\mathbf{O}[n] + B\mathbf{U}[n] \\ y[n] &= C\mathbf{O}(n) + D\mathbf{U}(n) \end{aligned} \quad (5)$$

where $\mathbf{U}[n] = \begin{bmatrix} u[n] & v[n] \end{bmatrix}^T$. The behavior of all the K-SCIs in the loop-filter can be described by the discrete-time state-space model

$$\begin{aligned} \mathbf{x}[n+1] &= A_{int}\mathbf{x}[n] + B_{int}\mathbf{P}[n] \\ \mathbf{O}[n] &= C_{int}\mathbf{x}[n] \end{aligned} \quad (6)$$

where $\mathbf{x}[n]$ is now the new state vector of the KD1S loop-filter with the K-SCI non-idealities.

Combining Eqs. 5 and 6, we get the state-space model for the overall KD1S modulator as

$$\begin{aligned} \mathbf{x}[n+1] &= [A_{int} + B_{int}(A - I)C_{int}]\mathbf{x}(n) + B_{int}B\mathbf{U}[n] \\ \mathbf{y}(n) &= CC_{int}\mathbf{x}(n) + D\mathbf{U}[n] \end{aligned} \quad (7)$$

From Eq. 2, for the first-order KD1S modulator, we have the ABCD matrix for the integrators given by

$$\left[\begin{array}{c|c} A & B \\ \hline C & D \end{array}\right]_{int} = \left[\begin{array}{cc|c} 1 & 0 & 1 \\ 1-\alpha_0 & \gamma_0 & 0 \\ \hline 1-\alpha_0 & \gamma_0 & 0 \end{array}\right] \quad (8)$$

For a second-order KD1S modulator, the integrator ABCD matrix is

$$\left[\begin{array}{c|c} A & B \\ \hline C & D \end{array}\right]_{int} = \left[\begin{array}{cccc|cc} 1 & 0 & 0 & 0 & 1 & 0 \\ 1-\alpha_{0_1} & \gamma_{0_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 \\ 0 & 0 & 1-\alpha_{0_2} & \gamma_{0_2} & 0 & 0 \\ \hline 1-\alpha_{0_1} & \gamma_{0_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 1-\alpha_{0_2} & \gamma_{0_2} & 0 & 0 \end{array}\right] \quad (9)$$

Similarly the combined integrator ABCD matrix for any order of modular can be easily obtained. The modified state-space model for KD1S, as in Eq. 7, has been implemented in Matlab by extending the delta-sigma toolbox functionality.

Finally, the procedure for designing a generalized KD1S modulator can be summarized in Algorithm 1.

Algorithm 1 Using the modified delta-sigma toolbox,
1. Synthesize a NTF zero optimized, single-path modulator for a given order with an effective oversampling ratio equal to $K \cdot OSR$.
2. Apply dynamic range scaling on the $ABCD$ matrix of the synthesized loop-filter.
3. Map the scaled $ABCD$ matrix to either CIFB or CIFF modulator topology.
4. Find the $ABCD_{int}$ matrix to represent all the K-path SCIs in the loop-filer.
5. Use the $ABCD_{int}$ matrix to find the overall $ABCD$ matrix for the KD1S modulator using Eq. 7.
6. Using simulations, estimate the effective gain of the quantizer ($\hat{k_q}$) employed in the modulator as $\hat{k_q} = \frac{E[|y|]}{E[y^2]}$.
7. Evaluate the NTF and STF for the synthesized KD1S modulator using the estimated $\hat{k_q}$ value.
8. Plot their pole-zero plot (root locus) and simulate the modulator to test for its stability.
9. Iteratively adjust the f_{un} of the op-amps to optimize the power consumption and stability of the designed KD1S modulator.

IV. Results

In order to demonstrate the efficacy of the higher-order KD1S modulator synthesis procedure, outlined in the last section, a second-order CIFB and a third-order CIFF KD1S modulators have been synthesized. For these modulators $K_{path} = 8$ so that the effective oversampling ratio is $K_{path} \cdot OSR = 64$. An 8-phase clock operating at a frequency of $f_s = 100\,MHz$ is used which results in an effective sampling frequency $f_{s,new} = 800\,MHz$. Here, the signal bandwidth in equal to $6.25\,MHz$. The comparators in the quantizer are assumed to be able to settle completely in $T_s/K_{path} = 1.25\,ns$ with negligible small-input metastability. However, the unity gain frequency of each of the op-amps is constrained to a small multiple of the clock frequency f_s.

Second-order CIFB KD1S Modulator: A second-order feedback-type KD1S modulator block diagram is shown in Fig. 4. The synthesis procedure described in the last section is applied to obtain the loop-filter parameter vectors $\mathbf{a}$, $\mathbf{b}$, $\mathbf{c}$ and $\mathbf{g}$. For this design, the op-amp gain-bandwidths are chosen to be equal to $3f_s$ (=$3/8 f_{s,new} = 300\,MHz$). The design is dynamic range scaled (DRS) to bound the integrator state within 0.6 times the supply voltage. The simulation results for the designed modulator are illustrated in Fig. 5. The simulation shows an SNR equal to 73.7 dB or a resolution of 11.94 bits. The maximum stable amplitude was found to be equal to $u_{max} = 0.9$.

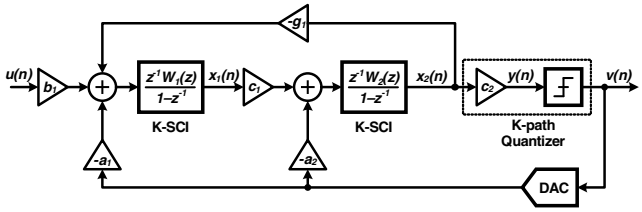

Figure 4. The synthesized second-order, single-bit CIFB KD1S modulator. Here $a_1 = 0.125$, $a_2 = 0.1$, $b_1 = 0.125$, $c_1 = 0.223$, $c_2 = 7.66$ and $g_1 = 0.04$.

In order to verify the conformance of the state-space model with the actual circuit implementation, the second-order KD1S modulator was implemented at circuit level in Cadence (see

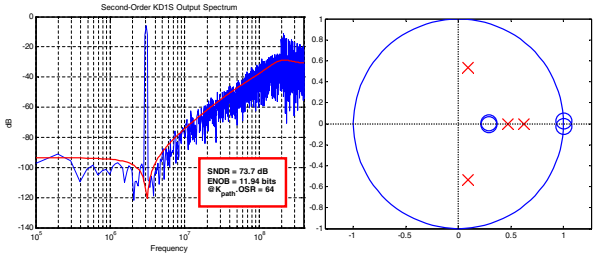

Figure 5. Simulated PSD of the output and the NTF pole-zero plot for the second-order CIFB-type KD1S modulator.

Fig. 6). The resulting Spectre simulation results are illustrated in Fig. 7. The resulting noise transfer function, with finite op-amp gain-bandwidth, is very close to the analytical modeling.

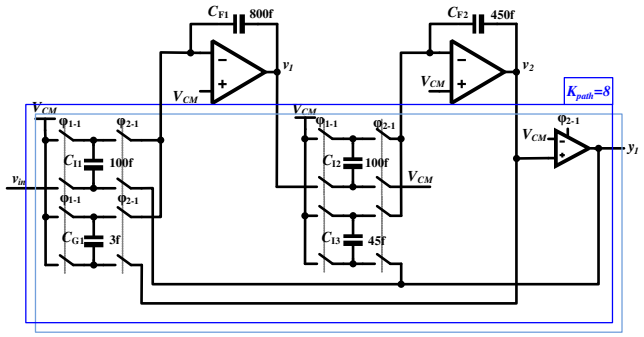

Figure 6. A concise representation of the singly-ended, switched-capacitor implementation of the second-order KD1S modulator seen in Fig. 5.

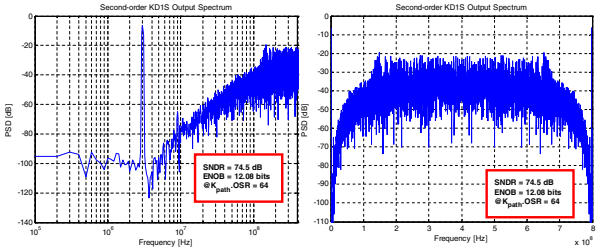

Figure 7. Spectre simulated spectrum for the second-order KD1S modulator (log and linear frequency axes).

Third-order CIFF KD1S Modulator: Feedforward type (CIFF) modulators are have been widely employed to realize wideband (low-OSR) data-conversion with lower signal distortion. This results from the fact that the input to the modulator's loop-filter only consists of the quantization noise. However the CIFF topologies require a fast, low-distortion adder at the input of the quantizer [4]. A third-order KD1S modulator has been synthesized and illustrated in Fig. 8 to further demonstrate the efficacy of the synthesis algorithm. Here, in order to stabilize the modulator the op-amps are designed with a gain-bandwidth equal to $5f_s = 500\,MHz$ to keep the poles well within the unit circle.

The simulation for the third-order modulator shows an SNR equal to 77.3 dB or a resolution of 12.55 bits. The maximum

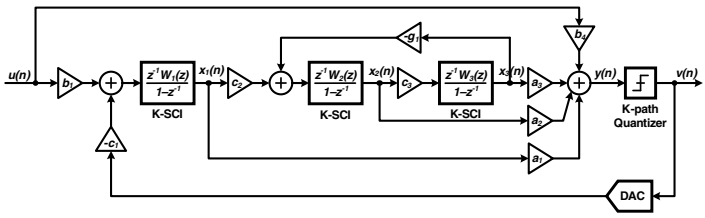

Figure 8. The synthesized third-order, single-bit CIFF KD1S modulator. Here $a_1 = 2.85$, $a_2 = 2.85$, $a_3 = 2.35$, $b_1 = 2.8$, $b_4 = 1$, $c_1 = 0.28$, $c_2 = 0.36$, $c_3 = 0.18$ and $g_1 = 0.08$.

stable amplitude was estimated to be equal to $u_{max} = 0.4$.

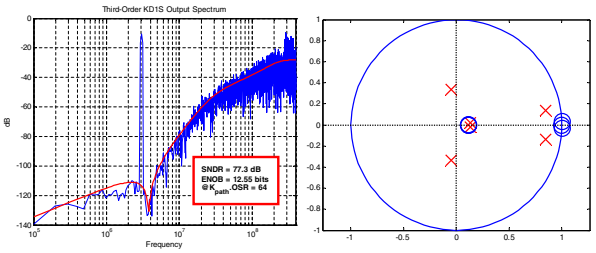

Figure 9. Simulated PSD of the output and the NTF pole-zero plot for the third-order CIFF-type KD1S modulator.

The higher-order KD1S modulators achieve lower performance when compared to single-path delta-sigma modulators with an effective oversampling rate of $K_{path} \cdot OSR$, but they still offer a reasonable trade-off with relaxed performance requirements on the op-amps and the clock generation circuits. Also, here only linear setting of the integrators has been considered for rapid synthesis of KD1S modulators. The nonlinear effects of the synthesized loop-filter must be simulated with behavioral circuit modeling of op-amp slewing.

V. Conclusion

A novel state-space based synthesis method has been proposed to realize higher-order KD1S modulators with any generalized topology. This method enables rapidly synthesis wideband KD1S modulators without designing their circuit level implementation and then simulating them to determine their stability. Second and third order feedback and feedforward type KD1S modulators are designed demonstrate the efficacy of the proposed synthesis method.

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