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Compact Method for Modeling and Simulation of Memristor Devices

Ion conductor chalcogenide-based memristor devices

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***Abstract*—A compact model and simulation methodology for chalcogenide based memristor devices is proposed. From a microprocessor design view point, it is important to be able to simulate large numbers of devices within the integrated circuit architecture in order to speed up reliably the development process. Ideally, device models would accurately describe the characteristic device behavior and would be represented by single-valued equations without requiring the need for recursive or numerically intensive solutions. With this in mind, we have developed an empirical chalcogenide compact memristor model that accurately describes all regions of operations of memristor devices employing single-valued equations.**

Keywords- Memristor; Memory Device; Thin Film Device

I. INTRODUCTION

The memristor device postulated in 1971 by Leon Chua [1] as the fourth basic circuit element has received much attention in the research community since the publication of Strukov's 2008 paper titled "The missing memristor found" [2] The memristor name is a contraction for memory resistor [1] because that is exactly its function: to remember its history [3]. The memristor is a two terminal passive device whose resistance state depends on its previous state and present electrical biasing conditions, and when combined with transistors in a hybrid chip, memristors could radically improve the performance of digital circuits without the need for further reduction of transistor dimensions [3]. Given their two terminal structural simplicity and electronic passivity, the applications for memristor technology range from non-volatile memory, instant on computers, reconfigurable electronics and neuromorphic computing [3,4]. According to Chua [4], the memristor behaves like a linear resistor with memory but also exhibits many interesting nonlinear characteristics, and several electronic models have been presented to describe the electrical behavior of memristor devices [1,2,4-6]. However, given that memristor devices are not commercially available, good physical model-to-hardware correlations have not been yet been reported in the published literature. Therefore, in this work, we present what we believe to be the first model-to-hardware correlation of memristor electrical characteristics. In our studies, we have employed both linear and nonlinear models from the published literature to fit our memristor hardware. However, we have observed that these published models do not represent accurately the electrical characteristic behavior or our memristor device hardware. Therefore, we have developed a simple compact model that accurately represents the electrical behavior of chalcogenide based memristors..

II. EXPERIMENTAL DETAILS

Memristor devices were fabricated on 200 mm p-type Si wafers. Isolated tungsten bottom electrodes were patterned on the wafers and a planarized nitride layer was used for device isolation. Vias were etched through the nitride layer to provide contact to the bottom electrode and to define the device active region. Prior to deposition of the memristor materials, the wafers received an Ar+ sputter clean to remove residual material and potentially remove any oxides that might have formed over the tungsten electrode. The memristor device structure consists of the layers (from bottom electrode contact side to top electrode contact): 300 Å Ge2Se3/500 Å Ag2Se/100 Å Ge2Se3/500 Å Ag/100 Å Ge2Se3. The 100 Å Ge2Se3 layers are needed for device processing only since Ag cannot be deposited directly on Ag2Se and since tungsten (for the top electrode) does not adhere well to Ag in this material stack. The layers were deposited by thermal evaporation using a *CHA Industries SE-600-RAP* thermal evaporator equipped with three 200 mm wafer planetary rotation. The rate of material deposition was monitored using an *Infincon IC 6000* with a single crystal sensor head. The base system pressure was 1x10-7 Torr prior to evaporation. A tungsten top electrode was deposited by sputtering tungsten (350 Å) and etching to define the device top contact and bond pad. Etching was performed with a *Veeco* ion-mill by etching through the tungsten and the memristor device materials and stopping on nitride. The top and bottom electrode bond pad contacts were 80 um x 80 um.

Electrical measurements were performed with either an *HP4145B* or an *Agilent B1500A* semiconductor parameter analyzer. A *Micromanipulator 6200* microprobe station equipped with a temperature controllable wafer chuck was used

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for the wafer-level device measurements. Probe tips were either *Micromanipulator W size 7B* or *American Probe and Technologies 73CT-APTA* probe tips. The tested devices were 180 nm in diameter as defined by the via etched through the nitride layer to the bottom electrode. As fabricated, the devices do not display negative differential resistance (NDR). NDR is induced in the devices by application of short (ns) negative potential pulses (negative with respect to the top electrode). Application of several of these pulses irreversibly induces NDR in the devices allowing them to permanently function as memristor devices.

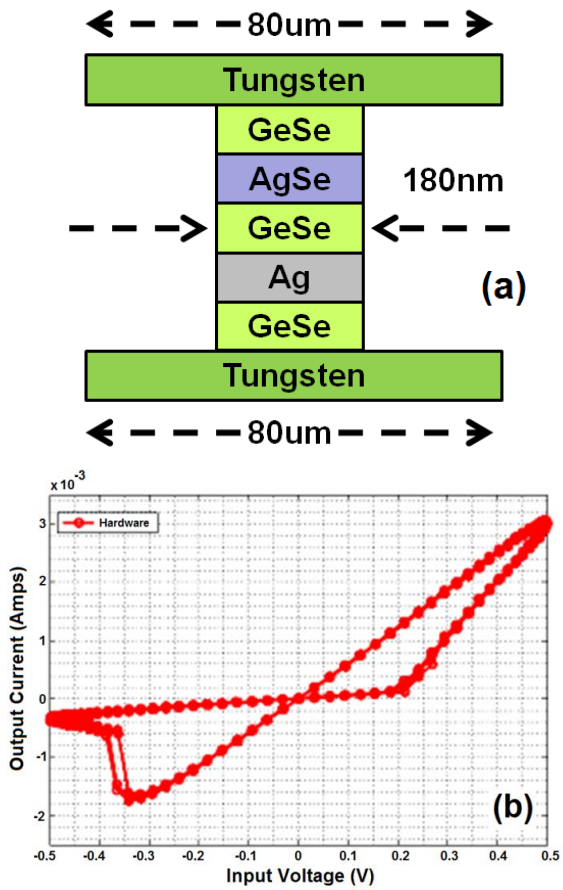

Fig. 1. (a) Memristor fabrication design and (b) typical memristor device Lissajous I-V curve characteristic behavior at100Hz frequency.

Figure 1(a) displays the memristor typical device structure, and figure 1(b) shows the electrical Lissajous I-V curve characteristic response behavior of a memristor device under a sinusoidal input of 0.5 V volts amplitude and 100 Hz frequency. From the figure we can clearly observe that the memristor device toggles between two states of high and low conductivity. As the device transitions between low to high conductivity states it goes through high nonlinear diode-like processes at approximately -0.35 and 0.2 V threshold voltages respectively. The threshold voltage analogy is used here to describe the biasing regions where nonlinear behavior occurs.

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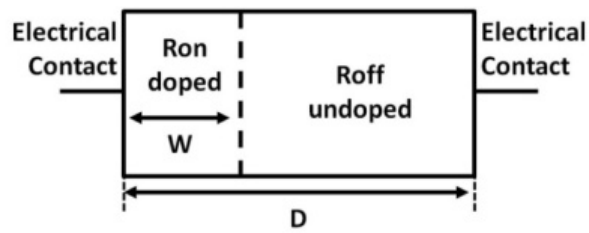

Fig. 2. Memristor device modeling structural diagram.

III. Memristor Models

The most basic mathematical definition of a memristor is that of a current-controlled device for circuit analysis in the generalized class of nonlinear dynamical systems called memristive systems described by the equations [2,4]

$$v = R(w, i)i \tag{1}$$

$$\frac{dw}{dt} = f(w, i) \tag{2}$$

where w can be a set of state variables and R and f can in general be explicit functions of time [2], [4]. For simplicity and ease of simulation, the memristor's resistance or memristance definition has been reduced to that of a current-controlled, time-invariant, one-port device given by [2]

$$M(w) = \frac{w}{D} R_{on} + \left(1 - \frac{w}{D}\right) R_{off} \tag{3}$$

where w represents the doped region of the memristor, D the total device length, and Ron/Roff the lowest and highest resistance states graphically described in Figure 2.

Equation (2) has been defined to describe the velocity at which w increases, meaning the device is becoming less resistive, we use as follows [2]

$$\frac{dw(t)}{dt} = u_v \frac{R_{on}}{D} i(t) \tag{4}$$

where uv is the average ion mobility for the simplest case of ohmic electronic conduction and linear ionic drift in a uniform field [2].

Utilizing Ohm's law that states that the voltage across a resistor is directly proportional to the resistance times the current through the conductor; we can obtain from equations (3) and (4) the following relationship [2]

$$w(t) = u_v \frac{R_{on}}{D} q(t) \tag{5}$$

and by inserting Equation (5) into Equation (3), we can obtain the memristance of the system, which for an Ron much less than Roff can be simplified to [2]

$$M(q) = R_{off}\left(1 - u_v \frac{R_{on}}{D^2} q(t)\right) \tag{6}$$

Equation (6) describes the memristance of the memristor system as a function of the charge q(t).

Additional improvements have been proposed to the aforementioned memristor model to include non-linear boundary conditions [5,6]. The non-linear boundary conditions proposed are of the form

$$f_p(w) = 1 - \left(\frac{w}{D} - \mathrm{stp}(-i)\right)^{2p} \tag{7a}$$

$$f_p(w) = 1 - \left(2\frac{w}{D} - 1\right)^{2p} \tag{7b}$$

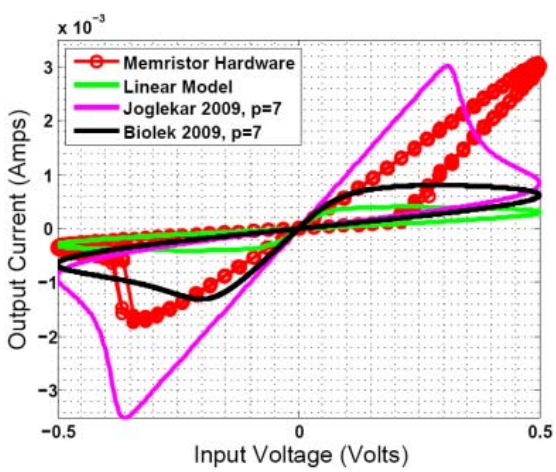

Fig. 3. Memristor hardware and model fit correlation between experiment and linear [2], green line, and nonlinear memristor models, magenta [5] line and black [6].

The nonlinear window functions in Equation (7a and b) guarantees zero velocity of the doped/undoped barrier interface described in Figure 1 as w approaches either boundary, w=0 or w=D. Moreover, the differences between the models with linear and nonlinear drift disappear when p increases [5]. The incorporation of the window function described by Equation (7) requires the redefining of Equation (4) as follows [6]

$$\frac{dw(t)}{dt} = u_v \frac{R_{on}}{D} i(t) f_p(w) \tag{8}$$

IV. Results and Discussion

Attempts have been made to perform a model fit utilizing both the linear [2] and nonlinear [5,6] memristor models. Figure 3 shows the memristor model-to-hardware correlation fit utilizing the linear [2], green line, and the nonlinear models proposed by Joglekar and Biolek [5,6], magenta and black lines. From the figure, it is clear that the linear and nonlinear model results do not accurately describe the Lissajous I-V characteristic behavior of our physical memristor. Given the lack of experiment and model correlation for both linear and nonlinear models, we have developed a simple empirical memristor compact model to model and simulate the Lissajous I-V characteristic behavior.

One important characteristic of memristor devices is the fact that their present behavior is dependent on their past state. Therefore, our simple compact model characteristic behavior is dependent on the previous memristor state requiring initial conditions. For example, $R_{mem}(t=T)$ represents the initial state of the device at time T, and R_{on} and R_{off} represent minimum and maximum states. Assuming the device's initial state is $R_{mem}(t=0)=R_{on}$ and that in time an input potential voltage greater than V_{th} is present across the device, we can describe the memristance behavior follows:

$$R_{mem}(t) = R_{mem}(t-\Delta t) - \Delta t K_{h1} e^{K_{h2}(V_{in}(t) - T_h)} \begin{cases} if\ R_{mem}(t) < R_{on} \\ else\ R_{mem}(t) = R_{on} \end{cases} \tag{9}$$

where Δt=1e-3/f corresponds to the minimum integral time step between memresistance observations, f is the frequency of the sinusoidal input voltage, T_h corresponds to the threshold voltage required to enter the nonlinear region from the off region, K_{h1} and K_{h2} correspond to fitting parameters used to capture the nonlinear effects.

On the other hand, if an input potential voltage lower than V_{tl} is present across the device, we can describe the behavior of the memristor device a follows:

$$R_{mem}(t) = R_{mem}(t-\Delta t) - \Delta t K_{l1} e^{K_{l2}(V_{in}(t) - T_l)} \begin{cases} if\ R_{mem}(t) > R_{off} \\ else\ R_{mem}(t) = R_{off} \end{cases} \tag{10}$$

where T_l corresponds to the threshold voltage required to enter the nonlinear region from the on region, and K_{l1} and K_{l2} are the fitting parameters to capture the nonlinear effects.

Otherwise, the state of the memristor device remains unchanged, and the present state of the memristor equals that of its previous resistance state, $R_{mem}(t) = R_{mem}(t\text{-}\Delta t)$.

Figure 4(a) shows the correlation between the device electrical characterization data and our proposed memristor model. From the Figure 4(a), we can observe that the compact model is able to describe all regions of electrical operation of the memristor device including the high and low conductivity regions and the nonlinear regions. The figure also includes the linear model fit for reference The compact model fitting parameters used to achieve the compact model fit displayed in Figure 5 are: R_{on}=160, R_{off}=1200, T_h=0.2, T_l=-0.35, K_{h1}=5e6, K_{h2}=-20, K_{l1}=4e6, K_{l2}=20, an input sinusoidal voltage of 0.5 V amplitude and 100 Hz frequency and the initial condition that $R_{mem}(t) = R_{off}$. In addition, Figure 4(b) displays the time dependent compact model results versus the experimental results for the memristor device hardware showing a good model-to-hardware correlation in the time domain.

V. Conclusion

We have proposed a simple compact model that describes the behavior of chalcogenide based memristor devices. Several models have been proposed in the literature on the linear and nonlinear electronic characteristic behavior of memristor devices; however, these reported models do not accurately describe the behavior of our chalcogenide memristors. Thus, we have developed an empirical simple compact model that describes the electrical behavior of memristor devices under sinusoidal input

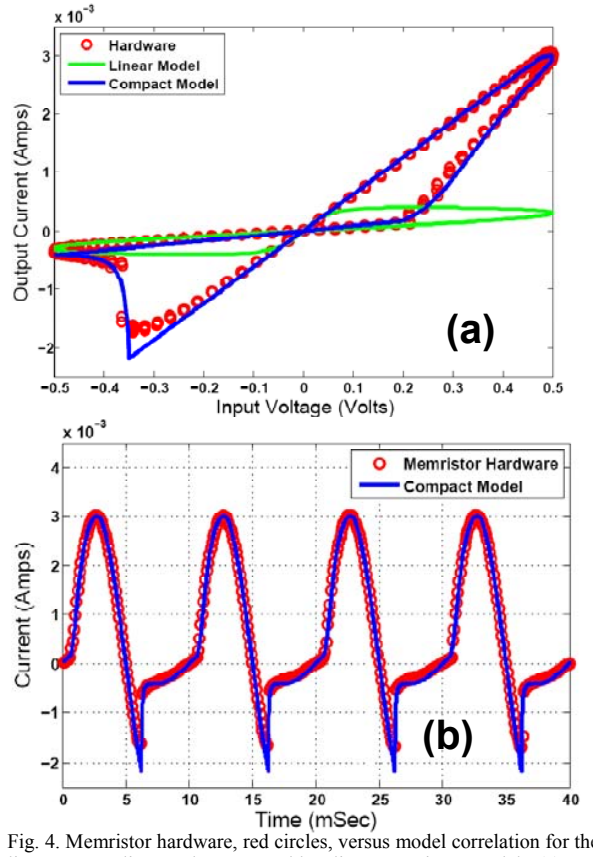

Fig. 4. Memristor hardware, red circles, versus model correlation for the linear, green line, and compact, blue line, memristor models (a) and memristor hardware, red circles, fit as function of time versus and compact model, blue line, (b).

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