8-1-2008

# A New Approach to the Design, Fabrication, and Testing of Chalcogenide-Based Multi-State Phase-Change Nonvolatile Memory

H. K. Ande

P. Busa

M. Balasubramanian

Kristy A. Campbell
*Boise State University*

R. Jacob Baker
*Boise State University*

# A New Approach to the Design, Fabrication, and Testing of Chalcogenide-Based Multi-state Phase-Change Nonvolatile Memory

H. K. Ande, P. Busa, M. Balasubramanian, K. A. Campbell, and R. J. Baker
Department of Electrical and Computer Engineering
Boise State University, Boise, Idaho, USA, jbaker@ieee.org

***Abstract* - A new approach to developing, fabricating, and testing chalcogenide-based multi-state phase-change nonvolatile memory (NVM) is presented. A test chip is fabricated through the MOSIS service. Then post processing, in the Boise State University lab, is performed on the chip to add the chalcogenide material that forms the NVM. Each memory bit consists of an NMOS access transistor and the chalcogenide material placed between the metal3 of the test chip, connected to the access device, and a common, to all memory bits, electrode. This paper describes the design of the memory bit and of the test structures used for reliability and radiation testing. Fabrication and post-processing of the memory are also discussed.**

*Keywords*- ***Phase change memory (PCM), nonvolatile memory, PCM test chip, memory reliability, fabrication, post-processing.***

## I. INTRODUCTION

Phase Change memory is considered to be one of the most promising candidates for the next generation of nonvolatile memory (NVM) [1]. The aerospace community considers chalcogenide-based phase-change memory (PCM) as a likely candidate technology in future of NVM for space applications [2]. Existing memory technologies like Dynamic Random Access memory (DRAM) and Flash memory work on the concept of charge storage [3]. DRAM suffers from scaling limitations, loss of data when power is removed (volatility) and data corruption due to radiation effects. Flash memory, though nonvolatile, is prone to radiation damage and has reliability issues due to its limited number of program/erase cycles. These limitations have led to efforts to develop chalcogenide-based NVM. The phase change memory (PCM) is a resistance based technology which operates on the principle of changing the resistance on the device to define the memory state as either '0' or '1'. The change in resistance occurs due to the change in phase of the chalcogenide material between a high resistance amorphous phase and a low resistance crystalline phase or vice-versa. Moreover, the characteristics of a chalcogenide based PCM lend themselves to store multiple bits (multiple states) in a single cell which results in much denser memories. Further PCM NVM can be scaled into high density arrays, has a large number of program/erase cycles, and has the potential to be more reliable than Flash memory due it its resistance to radiation effects, thus making it ideal for space applications.

This paper describes our current efforts to develop PCM using the MOSIS service [4] for fabrication of test chips. Through the MOSIS service a CMOS process is used to fabricate the test chips (test structures and small memory arrays). When the test chips are received from MOSIS the chalcogenide material is added to the chip as a back-end-of-line process at Boise State University.

Section II of this paper describes the operation of PCM. The device sizes and design constraints are discussed in Sec. III. Section IV describes the PCM Test chip, while Sec. V discusses the reliability issues in PCM NVM. Sec. VI describes the post-processing after the fabrication from MOSIS and in Section VII the progress and future work is discussed.

## II. THEORY OF OPERATION

The PCM consists of chalcogenide materials sandwiched between two electrodes. As shown in Fig. 1 the two chalcogenide layers are a Ge-chalcogenide (the memory layer), and a Sn-chalcogenide (the metal-chalcogenide layer).

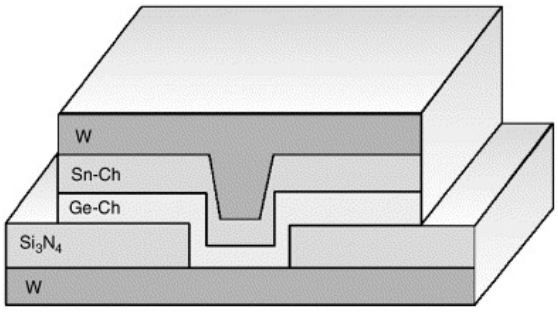


**Figure 1** Cross sectional view of chalcogenide device structure (from [5]).

By employing a stack of two different chalcogenide materials we hope to reduce the voltages, currents, and switching speeds needed for phase-change memory operation without the need for a complicated physical device structure [5-8]. The state of the memory cell is changed by causing a phase change between crystalline and amorphous states. This change is induced by Joule heating of the material through application of an applied current. When the phase is switched, the material changes resistance between low, KΩ values (crystalline) to high 100's KΩ or MΩ values (amorphous) [5].

The multi-state operation is obtained by using pulses with different programming currents, Fig. 2. The change of state from high resistance (amorphous) to low resistance (crystalline) occurs when a voltage higher than a threshold voltage ($V_t$) is applied to the amorphous material causing the resistance to decrease significantly. Due to the decrease in resistance there is an increased current flow in the chalcogenide materials which causes Joule heating of the material above the glass transition temperature. When the temperature rises above the glass transition temperature, but below the melting temperature, the current is removed, allowing the material to cool at a rate that will crystallize it into a low resistance state (write '11' current region, Fig. 2). To get a high resistance state (amorphous), more current is passed through the material to heat it above the melting temperature and then quickly removed to quench the material into an amorphous state (write '10' current region, Fig. 2). Further bits can be stored by passing more current till the resistance again decreases 'showing a snap back in the IV curve' to store '01' and '10' as described above. Hence the number of bits stored in a cell depends on the number of crystalline phases available in the chalcogenide material or, to be precise, the number of stable resistance states of the material.

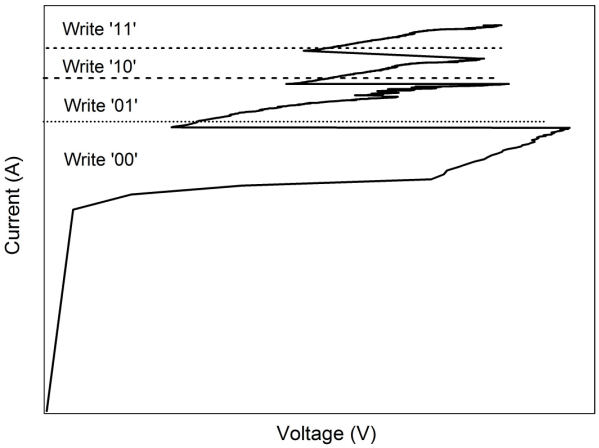


**Figure 2** IV curve of a memory bit with multi state capability.

Fig.3 shows example non-overlapping resistance distributions in a PCM cell. By having four stable resistance states 2 bits of data can be stored on a single cell. The number of stable resistance states determines the number of states we can store on a cell. Note that the chalcogenide material is modeled as a variable resistor where a logic value can be assigned for each resistance state thus realizing multi-state capability.

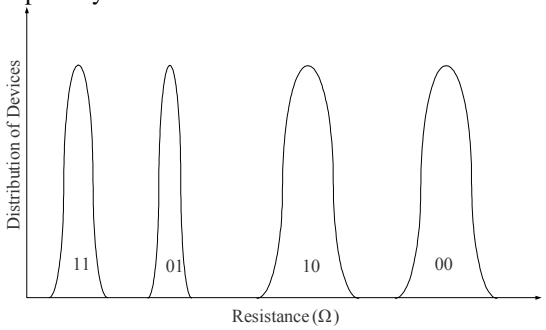


**Figure 3** An example distribution of states based on resistance.

## III. MEMORY BIT ELEMENT

The memory bit consists of an NMOS device as the access transistor and a chalcogenide memory element. The MOS device isolates the memory bits from each other. An NMOS device is preferred over a PMOS device since it has a larger drive current; a requirement for reaching all of the possible resistance states. As seen in Fig. 3, the gate of the MOSFET is used as the wordline, while the drain of the device is connected to the bit line. The PCM bit is connected to the source of the MOSFET. The other end of the PCM is connected to the top electrode of the bit which is common to all memory bits in an array. Note that the definition of the source and drain in Fig. 3 can be swapped depending on the value of the top electrode voltage (current always flows from drain to source). Further note that by connecting the memory bit to the source side of the MOSFET that more drive current can be supplied to the bit (which is important for good heat generation with access transistor size). For programming the cell the gate voltage (wordline) is set high and then a current pulse is passed through drain (bitline) of the access MOSFET which heats the chalcogenide and changes the state accordingly as discussed in Sec. II.

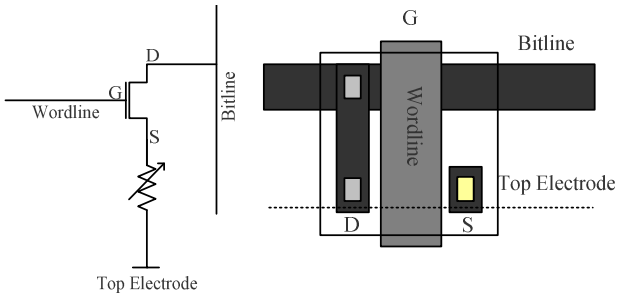


**Figure 4** Schematic and layout view of the memory bit

The NMOS access transistors in this work used a drawn size of 32/2 to ensure that adequate drive current is available to program the memory bits. These devices are laid out, in the test chip using two fingered MOSFETs with drawn widths of 16 each. The size of the NMOS access transistor is chosen to

provide a maximum drive current that is more than what is required to change the material to amorphous state which is estimated as 2 mA in this design. The size of the memory bits laid out in this process is 1.2 µm square.

The cross-sectional view of the memory bit used in our test structures is shown in Fig. 5. The PCM bit is placed between metal3 (MOSIS designation), which act as the bottom electrode, and a tungsten top metal plate. Since the design is done in a three metal process the chalcogenide is deposited on metal3 after the chips are received back from MOSIS. The size of the chalcogenide is thus defined by the area of the exposed metal3.

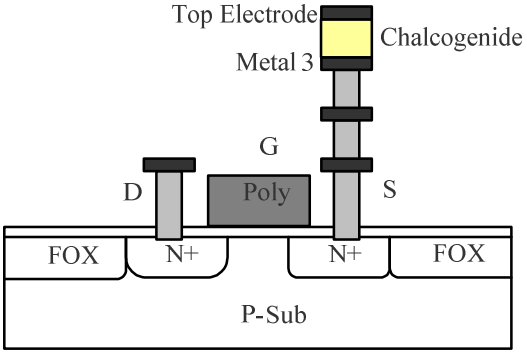


**Figure 5** Cross-sectional view of memory bit showing chalcogenide

## IV. PCM Test Chip

The PCM Test chip shown in Fig. 6 consists of test structures including the various sizes of memory bits (both with and without an access transistor), NMOS devices, and an 8 x 8 matrix of memory bits forming a basic 64-bit memory array. Site1 in Fig. 6 shows the test structures for memory array while Site 2 shows the test structures for individual chalcogenide resistor bits of various sizes.

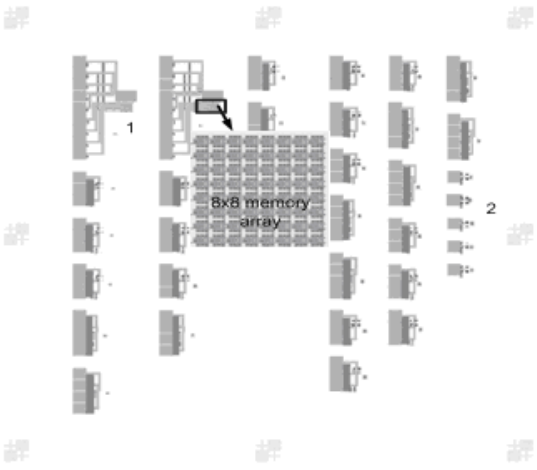


**Figure 6** Layout view of the entire test chip.

Row and column decoders were designed for the 64-bit memory array and sensing is done manually (off chip) to allow for the best characterization of the materials. This test structure array provides basic information concerning the performance of the chalcogenide resistor bit in an array since the read/write and accessing times can be estimated and the multi-state transition behavior in an array can be tested. Test structures of various sizes of NMOS access transistors are included to ensure that the I-V characteristics of the devices can be measured. In addition, test structures for memory bits with various NMOS sizes using minimum-sized chalcogenide bits are included to estimate the programmable currents required by the chalcogenide materials to obtain multi-state switching over a wide range of conditions.

## V. Reliability Issues

The chalcogenide stack as a resistor bit in this design is sandwiched between the metal3 and tungsten which act as bottom and top electrodes, respectively. This layered chalcogenide stack design eliminates the need for an external heater element. By using a material stack of GeTe/SnTe for chalcogenide where SnTe acts as the metal-chalcogenide layer, better adhesion is provided and delaminaton of electrode from chalcogenide memory layer after repeated program/erase cycles is prevented [5]. The devices with chalcogenide stack of GeTe/SnTe have shown at least two 'snap-back' regions similar to the I-V curves shown in Fig. 2 but the stability of the each resistance state is unknown. The switching behavior of the chalcogenide stack when integrated with the MOSFET will be used to determine this stability.

## VI. Fabrication and Post-Processing

The entire design of the PCM test chip is done using the Electric VLSI Design system and is designed for fabrication in AMI's C5 process. Fig. 7 shows the cross-sectional view of the fabrication of a single memory bit with NMOS access transistor and the chalcogenide deposition. Since the AMI's C5 process is a three metal process, the design of the memory up to metal3 is done at AMI. The chip after the MOSIS fabrication undergoes further processing at the Idaho Micro-fabrication Laboratory at Boise State University.

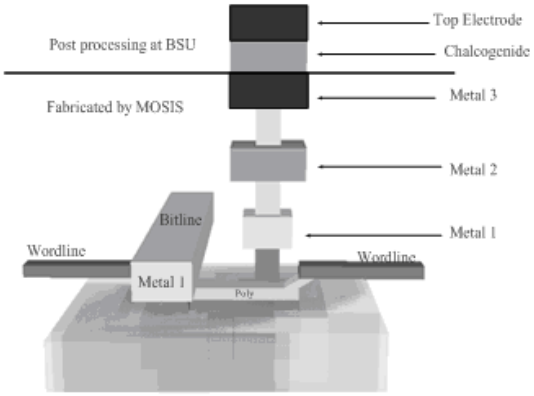


**Figure 7** Cross-sectional view of the memory bit.

The back-end-of-line process steps to complete device fabrication begin with chalcogenide layer deposition using thermal evaporation and/or sputtering on the entire chip

followed by top electrode deposition using sputtered tungsten. Using photolithography, the chalcogenide devices and top electrode bond pads are defined, followed by ion mill etching of the top electrode and chalcogenide stacks. Another photolithography step defines the bottom electrode contacts (which were closed by initial chalcogenide and top electrode deposition). Last, a dry etch is done to open up the bottom electrode contacts.

## VII. Progress and Future Work

The phase change memory (PCM) test chip is currently being fabricated through the MOSIS service and once back-end-of-line processing at BSU is finished, the reliability and radiation tests will be run and parameters such as write current, read/write times, resistance states of each 'snap-back' regions and multi-state transitions will be estimated for individual memory bits and for the 64bit array. Memory arrays up to 1GB are now being designed and efforts on obtaining multi-state transitions in the chalcogenide memory for larger arrays are underway.

## VIII. Conclusion

A new approach for the design, testing, and characterization of nonvolatile multi-state chalcogenide memory has been proposed. The design of individual memory bits is discussed and the test structures included in the PCM test chip are described. Fabrication by MOSIS and post-processing at BSU on the PCM test chip to deposit the chalcogenide and the top electrode is illustrated. After finishing the post-processing the memory chip will be tested for read/write capability and write current requirement for each resistance region of the multi-state memory. Finally, reliability and radiation testing will be done on the PCM test chip.

## ACKNOWLEDGMENTS

This work was supported by a NASA Idaho EPSCoR grant, NASA grant NNX07AT60A.

## References

[1] A.L. Lacaita, "Phase change memories: State-of-the-art, challenges and perspectives" *Solid-State Electron.* **50** (2006), pp. 24-31.

[2] B. Li, A. Bumgarner, D. Peikl, J. Stobie, W. Neiderer, M. Graziano, L. Burcin, T. Storey, B. Orlowsky, K. Hunt, J. Rodgers, J. Maimon, "A 4-Mbit Non-Volatile chalcogenide-random access memory designed for space applications" , *Non-Volatile Memory Technology Symposium*, (2006), pp. 64-70.

[3] M. Wuttig and N. Yamada "Phase-change materials for rewriteable data storage", *Nature Materials*, **6** (2007), pp. 824-832 .

[4] MOSIS "Low-cost prototyping and small-volume production service", http://www.mosis.com/

[5] K.A Campbell and C.M. Anderson, "Phase-Change Memory Devices with Stacked Ge-Chalcogenide/Sn-Chalcogenide Layers", *Microelectronics Journal* **38** (2007), pp. 52-59.

[6] W.Y. Cho, B.-H. Cho, B.-G. Choi, H.-R. Oh, S. Kang, K.-S. Kim, K.-H. Kim, E.-E. Kim, C.-K. Kwak, H.-G. Byun, Y. Hwang, S. Ahn, G.-H. Koh, G. Jeong, H. Jeong and K. Kim, "A 0.18-μm 3.0-V 64-Mb nonvolatile phase-transition random access memory (PRAM)", *IEEE J. Solid-State Circuits* **40** (2005), pp. 293–300.

[7] M.H. Lankhorst, B.W. Ketelaars and R.A. Wolters, "Low-cost and nanoscale non-volatile memory concept for future silicon chips", *Nat. Mater.* **4** (2005), pp. 347–352.

[8] H.F. Hamann, M. O'Boyle, Y.C. Martin, M. Rooks and H.K. Wickramasinghe, "Ultra-high-density phase-change storage and memory", *Nat. Mater.* **5** (2006), pp. 383–387.