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Low-Voltage CMOS Temperature Sensor Design Using Schottky Diode-Based References

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Abstract – **This paper presents the design of a fully differential sigma-delta temperature sensor using Schottky diode-based current references as a replacement for the traditional PN junction diode-based current references. This sensor was designed using the AMI 0.5um process through the MOSIS fabrication organization[1], and the chip performance will be evaluated and compared to the simulated results. The use of the Schottky diode and differential current sensing in the sigma-delta-type sensor allows for lower voltage operation and better noise performance.**

Keywords – CMOS, temperature sensor, CTAT, PTAT, sigma-delta modulation, schottky diode.

I. Introduction

Thermal management circuits have been used for many years in systems such as air conditioners, heating systems, and automotive applications [2]. Today, on-chip temperature sensors are often integrated into microprocessors and memory chips (such as DRAM and Flash) to control the mode or speed of system operation based on the system temperature [3].

In most commonly-used integrated CMOS temperature sensors, one or more bias circuits that utilize a PN junction diode or a diode-connected PNP bipolar transistor are used. This is due to the well-defined I-V temperature characteristics of the semiconductor PN junction. The forward bias voltage of this junction is approximately 0.7 V.

As CMOS device geometries continue to shrink, so do the voltages that supply these circuits [4]. As the supply voltage decreases, this 0.7V drop can be a limiting factor. The need for a device with a similar well-defined temperature characteristic and a lower forward-bias voltage becomes obvious [5]. This paper explores using the Schottky metal-semiconductor (MS) junction diode as a replacement for the tradition PN junction diode in a temperature sensor. It also explores noise problems and other issues that arise with low-voltage temperature sensor design.

II. Circuit Design

A. Schottky Diode Considerations

Most metal-semiconductor junctions (like almost all interconnects in a common integrated circuit) are called *ohmic* contacts, which essentially act as short circuits with a contact resistance added in series with the contact. This type of contact is achieved when a metal is connected to a heavily doped semiconductor. A Schottky contact (which forms the diode junction) is formed by a junction between a metal and a lightly doped semiconductor. The semiconductor may be either n- or p-type, but n-type silicon is generally used. The diode behavior is due to a barrier that is formed at the junction due to a difference in the metal and semiconductor work functions. In general, the height of this barrier is about ½ of the barrier height created by a p-n semiconductor junction[7]. This built-in potential must be overcome in order to allow current to flow through (forward bias) the junction.

The potential required to forward bias this junction is highly dependent on the N-well doping at the junction. Since the doping at this type of junction is not closely monitored in most CMOS processes [6], the design must allow for variation in the voltage characteristics of the Schottky diode. In the design presented here, multiple combinations of parallel Schottky diodes allow for easy adjustments to compensate for the diode variation. Further discussion of Schottky diode characteristics not found in this paper can be found in the referred literature [7].

B. Current References

Figure 1 shows a common example of a current reference designed in a short-channel CMOS process using diode-connected bipolar junction transistors. The bipolar junction transistor can be made from the parasitic substrate bipolar transistor inherent in CMOS processes [6]. The voltage drop across such a device is approximately 0.7V. As CMOS processes scale down to smaller geometries, the supply voltages also scale down and are fast approaching the sub-1V range. As this happens, the PNP-based reference will no longer be practical.

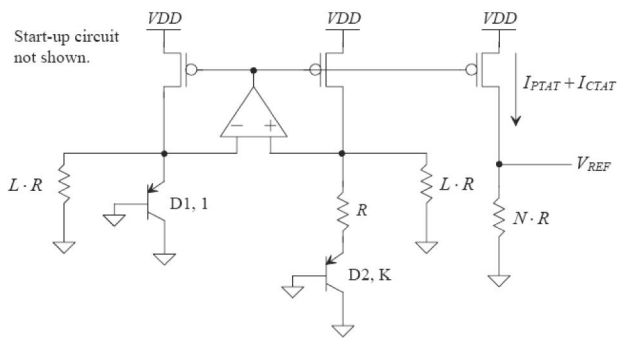

Figure 1. A bandgap reference circuit design [6]

The Schottky diode, discussed in the previous section, offers a viable solution to this problem, as it has a forward-biased voltage drop of approximately 0.3-0.4V. Schottky diodes were used in the design of a low-voltage bandgap reference in [5]. The authors characterized the Schottky diode in the same process used for this temperature sensor design (AMI 0.5um process through the MOSIS organization). As a starting point, the SPICE model parameters for the Schottky diodes derived in that paper were used in the design of this temperature sensor.

In this work, Schottky diodes are used to build current references whose currents vary complementary to absolute temperature (CTAT), and proportional to absolute temperature (PTAT). A schematic of a CTAT current reference is shown in Fig. 2.

This current reference uses the voltage drop across the forward-biased Schottky diode (V_d) to set the current flowing through the resistor in the other leg of the reference circuit. Since the diode voltage (V_d) has a moderately negative temperature coefficient (between -1.5mV and -2.0mV/°C) and the resistor has a positive temperature coefficient (increasing resistance with increasing temperature), the current through the resistor will have a negative temperature coefficient (a CTAT current). The temperature coefficient, as derived in [6], is:

$$TCI_{CTAT} = \frac{1}{V_d}\frac{\partial V_d}{\partial T} - \frac{1}{R}\frac{\partial R}{\partial T} \quad (1)$$

This equation shows that this current is a CTAT since the temperature coefficient is simply the temperature coefficient of the diode voltage (a negative number) minus the temperature coefficient of the resistor (a positive number).

A PTAT current can be produced by adding K parallel-connected diodes in series with the resistor to ground, as shown in Fig. 3.

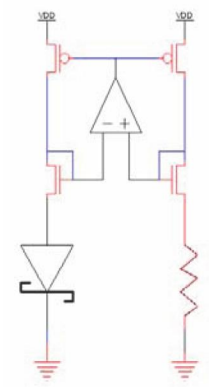

Figure 2. A CTAT current reference using the forward bias voltage of a schottky diode to set the voltage across a reference resistor (a startup circuit is necessary, but not shown).

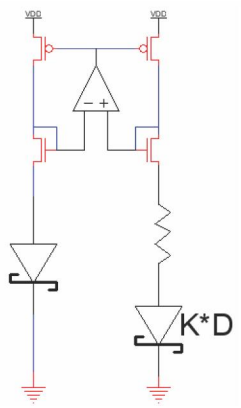

Figure 3. A PTAT current reference using the forward bias voltage of a Schottky diode to set the voltage across a reference resistor and K Schottky diodes in parallel.

The equation for the current in this reference was also derived in [6], and is shown below for reference (*nkT/q* is the diode thermal voltage)

$$I = \frac{nk * \ln K}{qR} * T \quad (2)$$

It is important to note that this current is inherently a PTAT current, based on this equation. Decreasing the resistor size will increase the temperature coefficient, with the tradeoff of increased current (and thus increased power dissipation). In order to use these references in our temperature sensor design, the current was mirrored to produce p-channel and n-channel versions of both currents (PTAT and CTAT). Other diode-based references can be used to produce CTAT and PTAT currents, but these topologies were chosen for simplicity.

C. *Data Converter Design*

A number of different topologies were considered for the temperature sensor data converter. A flash-type data converter is a popular data converter topology due to its simplicity and speed of conversion. The resolution of this converter is limited by the matching of the resistors in the resistor stack and the comparator offset. Also, a 2n-bit resolution converter requires n comparators, which requires a large layout in order to achieve higher resolution.

A sigma-delta ADC was used for this design. Advantages of this topology include eased requirements on comparator accuracy. Increased temperature resolution can also be achieved by averaging a larger number of samples during the temperature sense. A fully-differential sensing design was also chosen because it eases reference voltage requirements and has much better noise performance than a single-ended design. A diagram showing the basic converter topology is shown in Fig. 4.

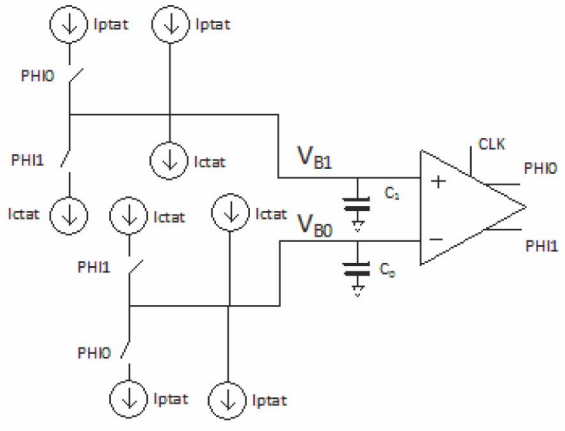

Figure 4. Basic topology of differential sigma-delta temperature sensor (Common-mode feedback circuit excluded from diagram for simplicity).

The topology shown is similar to that shown in [2], with I_{CTAT} replacing I_{be}. This topology has the advantage of extending the dynamic range of the converter at the expense of more current consumption. A ones counter is attached to the PHI0 output of the comparator to produce a digital output code N. The equation for this code is shown below (where M is the total number of samples taken).

$$\frac{N}{M} = \frac{2 * I_{PTAT} - I_{CTAT}}{I_{PTAT} + I_{CTAT}} \tag{3}$$

Bakker and Huijsing [2] show how this topology increases the dynamic range of the converter as compared to a more traditional sensing topology where

$$\frac{N}{M} = \frac{I_{PTAT}}{I_{CTAT}} \tag{4}$$

In this fully-differential topology, it is very important to accurately match all CTAT current sources to each other, as well as matching all of the PTAT sources. In a practical circuit, these currents cannot be exactly matched. This mismatch causes common-mode voltage (V_{CM}) drift, which will affect the accuracy of the sense. V_{CM} is defined as follows:

$$V_{CM} = \frac{V_{B0} + V_{B1}}{2} \tag{5}$$

If this voltage drifts to where the voltage on either line lies outside of the common mode input range of the comparator, it will severely decrease the accuracy of our temperature sense. Adding a common mode feedback amplifier (error amplifier) to the input lines of the comparator will keep the common-mode voltage constant without introducing distortion to the temperature sense. Fig. 5 illustrates the operation of this error amplifier.

It is important to note that even though this re-introduces the need of a reference voltage in the temperature sensor (also required in the single-ended sensor design), it eases the noise

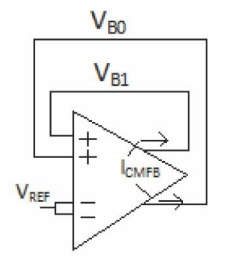

Figure 5. A common-mode feedback amplifier that injects an equal current (I_{CMFB}) onto both B0 and B1 whenever the average of B0 and B1 (V_{CM}) drifts away from V_{REF}.

restrictions on this reference voltage. Any reference noise, including power supply variation, produces a common-mode current on the sense lines which is ideally rejected and does not adversely affect the accuracy of the sense.

With this common-mode feedback added to the circuit, the equation for the digital output (N/M) can be derived to account for the effects of current and capacitor mismatch. With the common-mode feedback circuit, the following condition is satisfied (Note T = clock period).

$$\Delta V_{B0} = -\Delta V_{B1} \tag{6}$$

For PHI1=1, $$\Delta V_{B0} = \frac{2 * I_{CTAT0} - I_{PTAT0} + I_{CMFB}}{C_0} T \tag{7}$$

$$\Delta V_{B1} = \frac{I_{PTAT1} - 2 * I_{CTAT1} + I_{CMFB}}{C_1} T \tag{8}$$

For PHI1=0, $$\Delta V_{B0} = \frac{I_{CTAT0} - 2 * I_{PTAT0} + I_{CMFB}}{C_0} T \tag{9}$$

$$\Delta V_{B1} = \frac{2 * I_{PTAT1} - I_{CTAT1} + I_{CMFB}}{C_1} T \tag{10}$$

If we plug equations 7-10 back into the equation 6, we can solve for I_{CMFB} and get the following equations:

For PHI1=1,

$$I_{CMFB} = \frac{2 * I_{CTAT0} - I_{PTAT0} - (I_{PTAT1} - 2 * I_{CTAT1}) * C_0/C_1}{1 + C_0/C_1} \tag{11}$$

For PHI1=0,

$$I_{CMFB} = \frac{I_{CTAT0} - 2 * I_{PTAT0} - (2 * I_{PTAT1} - I_{CTAT1}) * C_0/C_1}{1 + C_0/C_1} \tag{12}$$

From equations 11 and 12, we can make the following substitutions to write the general transfer function in terms of the currents, capacitors, and the mismatch of the currents.

$$I_{PTAT0} = I_{PTAT}, I_{PTAT1} = I_{PTAT} + \Delta I_{PTAT}$$
$$I_{CTAT0} = I_{CTAT}, I_{CTAT1} = I_{CTAT} + \Delta I_{CTAT} \tag{13}$$

The ΔI_{ptat} and ΔI_{ctat} terms represent the mismatch between the mirrored currents. Using these substitutions, we derive the general transfer function for the data converter:

$$\frac{N}{M}=\frac{\frac{C_0}{C_1}(2I_{PTAT}-I_{CTAT})+(\frac{1}{2}+\frac{3C_0}{2C_1})\Delta I_{PTAT}-(\frac{1}{4}+\frac{3C_0}{4C_1})\Delta I_{CTAT}}{(\frac{2C_0}{C_1}-1)(I_{PTAT}+I_{CTAT})+(\frac{1}{4}+\frac{7C_0}{4C_1})\Delta I_{PTAT}+(\frac{1}{4}-\frac{5C_0}{4C_1})\Delta I_{CTAT}} \quad (14)$$

If we neglect the current mismatch, we can see from this equation that any mismatch in the capacitors will result in a gain (and an effective increase in temperature resolution) as follows:

$$\frac{N}{M}=\frac{2I_{PTAT}-I_{CTAT}}{(2-\frac{C_1}{C_0})(I_{PTAT}+I_{CTAT})} \quad (15)$$

Programming with metal, fuses, or some type of mode register when the sensor is integrated into a given application would be desirable to adjust the gain of the sensor (and thus the temperature resolution).

Finally, if the capacitor gain is set to 1, the transfer function adversely affects the linearity adding a constant term to both the numerator and denominator of the transfer function:

$$\frac{N}{M}=\frac{2I_{PTAT}-I_{CTAT}+2\Delta I_{PTAT}-\Delta I_{CTAT}}{I_{PTAT}+I_{CTAT}+2\Delta I_{PTAT}-\Delta I_{CTAT}} \quad (16)$$

III. Simulation Results

Simulations were run on the temperature sensor with ideal matching conditions and also with current mismatch to create transfer curves for the temperature sensor and evaluate the accuracy of the derived equations. Figures 6 and 7 show these simulation results and the error (differential non-linearity or DNL) introduced by ~2% current mismatch on both I_{CTAT} and I_{PTAT}. Figure 6 illustrates how the temperature sensor is calibrated.

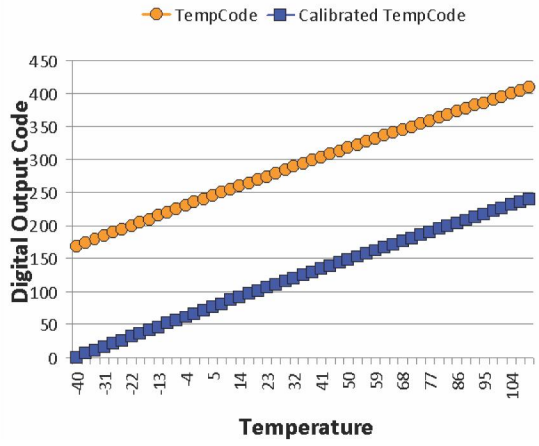

Figure 6. Transfer curve with no mismatch and an example of how calibration works by simply subtracting the count at the -40'C calibration point (setting -40'C equal to a count of zero).

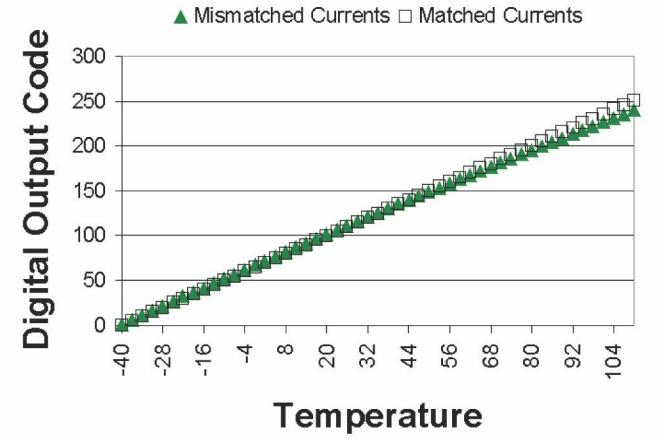

Figure 7. Simulation results with perfectly matched currents and a simulation with a mismatch of ~2% in both I_{CTAT} and I_{PTAT}.

A calibration point is chosen (-40C in this case) and a temperature measurement is taken. We can then subtract an amount based on that measurement to eliminate most or all of the offset error of the sensor.

IV. Conclusion

The design of a fully-differential current-mode sigma-delta temperature sensor using Schottky diode-based references is presented. The design methodology has been presented with special attention given to the advantages of using a fully-differential, noise shaping data converter topology and current references using Schottky diodes (as opposed to diode connected PNP transistors). This sensor was designed using the AMI 0.5um process through a MOSIS fabrication organization [1], and the chip performance will be evaluated and compared to the simulated results.

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