Electrical Characterization of a Second-gate in a Silicon-on-Insulator Transistor

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As an independent double-gate, silicon-on-insulator transistor, the Flexfet™ is suited for a wide range of applications in analog and digital circuitry. This study investigates the ability of the JFET bottom-gate to adjust and control several parameters in the Flexfet™ as well as shield against performance degradation due to substrate biasing. The device parameters under investigation include drive current, leakage current, and threshold voltage. The newly assigned F-factor describes the ability of Flexfet™’s bottom-gate to adjust the threshold voltage. Flexfet™ exhibits nearly a 10x and 3.5x increase in drive current for the nMOS and pMOS devices, respectively, with a 1 V bottom-gate voltage swing. Comparing the nominal devices with the low-power devices, both the nMOS and pMOS unexpectedly demonstrated higher leakage current for the low-power biasing. F-factors of 0.53 V/V and 0.38 V/V were calculated for the nMOS and pMOS devices, respectively. With a 40 V swing on the substrate potential, the nMOS device showed less than 12 pA increase in leakage current and no more than 20 mV of unwanted Vt shift. The pMOS measured less than 2 pA increase in leakage current and 10 mV of Vt shift for the same substrate biases.

Introduction

In the 2006 update, ITRS predicts that the implementation of fully-depleted SOI and multiple-gate MOSFETs will be necessary to manufacture devices at the 32 nm technology node¹. The Flexfet™ developed by American Semiconductor, Inc. incorporates both processes into a single device with a 1450 Å buried-oxide (BOX) and its self-aligned, implanted JFET bottom-gate (BG)²,³ Figure 1. The BG provides dynamic adjustment of several device parameters, including threshold voltage (V_t), drive current (I_on), and leakage current (I_off). This allows for low-power consumption in the stand-by mode and fast device operation when active.

Furthermore, there is a parasitic field-device created by the BOX and substrate in standard SOI devices which affects transistor performance by inadvertently adjusting Vt and increasing Ioff⁴. The Flexfet™ BG negates this parasitic by shielding against substrate potential and radiation-induced trapped-charge in the BOX, making Flexfet™ ideal for circuits where substrate biasing is necessary or in high-radiation environments.

This study investigates the ability of the bottom-gate in adjusting Ioff, Ion, and Vt as well as its ability to protect the transistor performance against substrate potential.

Experimental

The devices under investigation were fabricated at the 0.18 µm node, with gate-oxide and buried-oxide thicknesses of 35 Å and 1450 Å, respectively. The devices were tested with a supply voltage (VDD) of 1.8 V. To perform measurements, an HP 4156A Semiconductor Parameter Analyzer (SPA) was used in conjunction with a Cascade Microtech probe-station and four micromanipulators.

Standard log(ID)-VG tests were conducted, in which the nMOS source voltage (VS) = 0 V, drain voltage (VD) = 1.8 V and top-gate voltage (VTG) was swept from 0.0 V to 1.8 V. The pMOS test was similar with VS = 1.8 V, VD = 0 V and VTG swept from 1.8 V to 0.0 V. To investigate the device behavior with respect to the new BG, the bottom-gate voltages (VBG) were as follows: VBG = -0.5 V, 0 V, 0 V and VBG = 2.3 V, 1.8 V, 1.3 V for the nMOS and pMOS devices, respectively.
Ioff, Ion, and Vt were determined for each VBG. The low-power, nominal, and high-power device characteristics are then compared. A new parameter, F-factor (F) – defined as the change in threshold voltage with respect to the applied bottom-gate voltage – demonstrates the ability of the bottom-gate to control the threshold voltage of the device and is also reported. For each set of tests, the substrate voltage (VSUB) was stepped from -20 V to +20 V, in 5 V steps, to demonstrate the ability of the BG to shield against substrate biases.

![Flexfet™ cross-sectional views illustrating the implanted JFET bottom-gate (BG) and buried-oxide (BOX) layer.](image)

**Results**

Dynamic parameter adjustment

![nMOS Parameter Control for Stepped VBG](image)

**Figure 1.** Flexfet™ cross-sectional views illustrating the implanted JFET bottom-gate (BG) and buried-oxide (BOX) layer.

**Figure 2.** nMOS ID-VG comparison of low-power (VBG = -0.5V), nominal (VBG=0V) and high-power (VBG=0.5V) devices.

Figure 2 shows the ID-VG characteristics for an nMOS device with varying bottom-gate potentials. The drive current ranges from a low of 98.3 µA, low-power device, to a high of 839 µA for the high-power bias. The nominal value for the nMOS Flexfet™ drive current measured 315 µA. Ioff for the
low-power, nominal, and high-power biases measured 167 pA, 159 pA, and 175 pA, respectively. Notice the nominal device unexpectedly has less leakage current than the low-power device. For this nMOS transistor, the F-factor was calculated to be 530 mV/V. That is, a 530 mV Vt shift with a VBG stepped 1 V.

Figure 3 demonstrates the same odd behavior in leakage current for the pMOS device. Again the lowest leakage current, 53.1 pA, is measured when VBG = VS, the nominal biasing condition. The low-power device measured Ioff at 96.5 pA and the high-power device leaked 357 pA of current. For Ion, the currents read 119 µA, 225 µA, and 390 µA for the low- to high-power biases. The F-factor was calculated to be 380 mV/V. Table 1 summarizes the results for the nMOS and pMOS devices.

![pMOS Parameter Control for Stepped VBG](image)

*Figure 3. pMOS ID-VG comparison of low-power (VBG = 2.3 V), nominal (VBG=1.8V) and high-power (VBG=1.3 V) devices.*

Substrate shielding

![Substrate Bias Overlay for nMOS Device](image)

*Figure 4. ID-VG with varying substrates biases for the nMOS Flexfet™.*

Figures 4 and 5 show the ID-VG behavior with VSUB ranging from -20 V to +20 V for the nMOS and pMOS devices, respectively. As seen in the figures, there is little variation in the ID-VG curves across the full 40 V substrate swing; this suggests very little *inadvertent* shift in Vt and minimal increase in leakage current. The nMOS device exhibited only 20 mV change in Vt and an increase in leakage current.
less than 12 pA. The pMOS device behaved better, with only a 10 mV Vt shift and less than 2 pA increase in Ioff.

![Substrate Bias Overlay for pMOS Device](image)

Figure 5 ID-VG with varying substrates biases for the pMOS Flexfet™.

**Discussion**

**Dynamic parameter adjustment**

Table 1 summarizes the dynamic adjustment of Ioff, Ion, and Vt with the bottom-gate voltage stepped by 1 V. For the nMOS transistor, there is nearly a 10x increase in drive current from the low-power to the high-power device, 98.3 µA versus 893 µA. With an increase in drive current from 119 µA to 390 µA, the pMOS transistor showed slightly better than a 3-fold increase from the low-power to the high-power device. In analog and digital circuit design, higher drive currents are desirable to quickly drive capacitive loads. The nMOS device exhibited a significant adjustment in Ion, however, the pMOS device still has room for improvement.

Both the nMOS and pMOS devices show surprising results when the low-power device measured more leakage current than the nominal device. Given the operation of a standard JFET device, reverse biasing the pn-junction created by the channel region and highly-doped BG should result in less leakage current because of the increase in depletion layer width. Furthermore, this phenomenon was not present for the tests performed at supply voltage of 2.5 V. This behavior is still being investigated.

The Flexfet™ bottom-gate was able to adjust Vt 530 mV for the nMOS device and 380 mV for the pMOS device, corresponding to F-factors of 0.53 V/V and 0.38 V/V. While these are not as high as previously measured values, relatively small changes in the processing traveler could improve them. And even though the Vt shifts are not yet perfected, the effect they have on device parameters such as drive current is quite apparent.
Table 1. Summary of device parameter adjustment

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<th>Low-Power</th>
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<th>High-Power</th>
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<tr>
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<td>Ion (µA)</td>
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<td>F-factor (V/V)</td>
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<td><strong>pMOS device</strong></td>
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<tr>
<td>F-factor (V/V)</td>
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Substrate shielding

The Flexfet™ bottom-gate proves to be an effective shield against substrate biasing of ±20 V. The nMOS device showed less than 12 pA of leakage current increase and only 20 mV of unwanted Vt shift. The pMOS outperformed the nMOS with only 1.2 pA of Ioff increase and 10 mV of unintentional Vt shift. Figure 6 illustrates the shielding effect of the bottom-gate with respect to substrate biasing or trapped charge in the BOX. In standard SOI devices, the substrate is coupled to the channel (white region) through the substrate/BOX/channel parasitic MOSFET. So any potential placed on the substrate will attract carriers to the channel-BOX interface, changing the local carrier concentration and effectively adjusting the Vt and possibly creating a leakage path from source to drain. Similar behavior occurs due to radiation-induced trapped charge in the BOX. With the Flexfet™ BG, these effects are negated because there is no longer direct coupling from the substrate to the channel-region and the highly-doped p⁺ BG does not allow for channel inversion at the BOX-channel interface.

![Figure 6. Side-by-side comparison of standard silicon-on-insulator transistor and Flexfet™ device illustrating shielding effect of the bottom-gate.](image)

Similar tests investigating the effects of substrate biasing on standard SOI devices were conducted. Their results exhibit Vt changes of approximately 0.55 V and 0.75 V for their nominal nMOS and pMOS devices, respectively. Figure 7 compares the Vt shift of the Flexfet™ with this recently reported data. It should be noted that the BOX thickness of the standard SOI devices tested was 38% thicker than that of the Flexfet™, 2000 Å vs. 1450 Å. A thinner BOX would imply a stronger coupling effect and would result in larger Vt changes. However, this was not observed in the double-gated device. Demonstrating the effectiveness of the bottom-gate in shielding the transistor from unwanted Vt shifts caused by potential on the substrate.
Figure 7. Threshold voltage shift as a function of substrate potential comparing standard silicon-on-insulator transistor and FlexFet™.

Acknowledgments

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References