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Thermo-Mechanical Characterization of Copper Through-Wafer Interconnects

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Abstract

Copper through wafer interconnects (TWIs) have become a viable solution to providing interconnectivity between stacked die. In a world where minimizing chip real estate while increasing functionality is the goal for further miniaturization of electronics, TWIs hold a key role as new packaging schemes become critical for overall higher density. Little is known, however, about the impacts of mismatched coefficients of thermal expansion (CTEs) inherent to the materials used in their construction. CTE differences, if left unresolved, can pose reliability issues during TWI operation. This research focuses on providing insight into the stress levels experienced by TWI materials through finite element analysis to gain a better understanding of the possible failure mechanisms associated with the CTE differences.

Introduction

The increased demand for smaller portable and wireless electronics has resulted in the development of smaller, higher density integrated circuits (ICs) to be used in next generation micro-electronics [1,2]. Die stacking has surfaced as a viable method in achieving further miniaturization of electronic devices while increasing functionality. As a result, new packaging methods have been developed to accommodate increasing I/O counts. New methods such as system-in-a-package (SiP), chip-scale-packaging (CSP) and vertical die stacking (3-D) are just a few examples of novel packaging schemes used to minimize chip real estate. Other methods explored have included folded packages, chips imbedded in a polymer material and die-side metal contacts [3,4]. Although new methods are being used to shrink die footprints, wire bonding still remains as a common method used to create interconnects between stacked layers. With die stacked configurations, however, the number of I/Os is increased creating problems with reliability due to the complexity of wire bond routing paths. System performance can also be degraded due to increased interference susceptibility and the propensity for increased RC delay.

One alternative solution for creating fewer complex interconnects with 3-D die configurations is through the use of copper TWIs. Copper through-wafer interconnects are small copper filled vias formed through the die which act as the communication pathways between stacked layers. TWIs have been shown to provide dramatic improvements in chip performance including increased speed, decreased propagation delay and lower power requirements [5]. Shown in Figure 1 is just one example of a typical die stack configuration using TWIs.

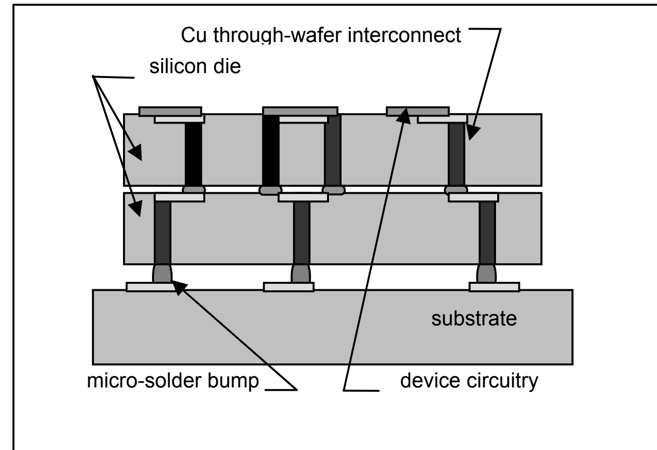

Fig-1: Schematic of a 3D die stack incorporating copper through-wafer interconnects

TWI Fabrication

TWIs have the advantage over wire bonding in that electrical connectivity between stacked layers can be provided without the added complexity of perimeter wire bonds. Micro-solder bumps are then used to join stacked die at the TWI interface allowing for multiple die stack configurations. The process used to create TWI's parallels many of the typical fabrication methods used to fabricate ICs [6].

Holes or vias are first patterned on one side of the wafer by using photolithography. Typical resist thicknesses used in IC fabrication are generally 2µm thick. In TWI fabrication, however, 10µm thick resist is needed to withstand the extended etching time required to form the vias. After patterning, the vias are then etched through the wafer using deep reactive ion (DRIE) plasma known as the Bosch etch method [7]. Via sizes can vary depending on the application. For this particular research, 50µm diameter vias were used in a 500µm thick wafer for a final aspect ratio of 10:1. For electrical isolation, a thin (~1µm) conformal coating of an organic insulator is deposited on the wafer covering both sides of the wafer including via walls. Next, a thin (~600nm) layer of Titanium-Nitride (TiN) is deposited using RF magnetron sputtering. The TiN acts as a diffusion barrier, protecting the silicon from copper contamination as well as providing an adhesion layer for the copper seed. Finally, a Cu seed layer is deposited after which an electroplated copper layer (20µm) is grown on top of the copper seed layer. Chemical-Mechanical Planarization (CMP) is then used to remove the bulk copper leaving copper inside the vias intact. Figure 2 shows a picture of the TWI fabrication process.

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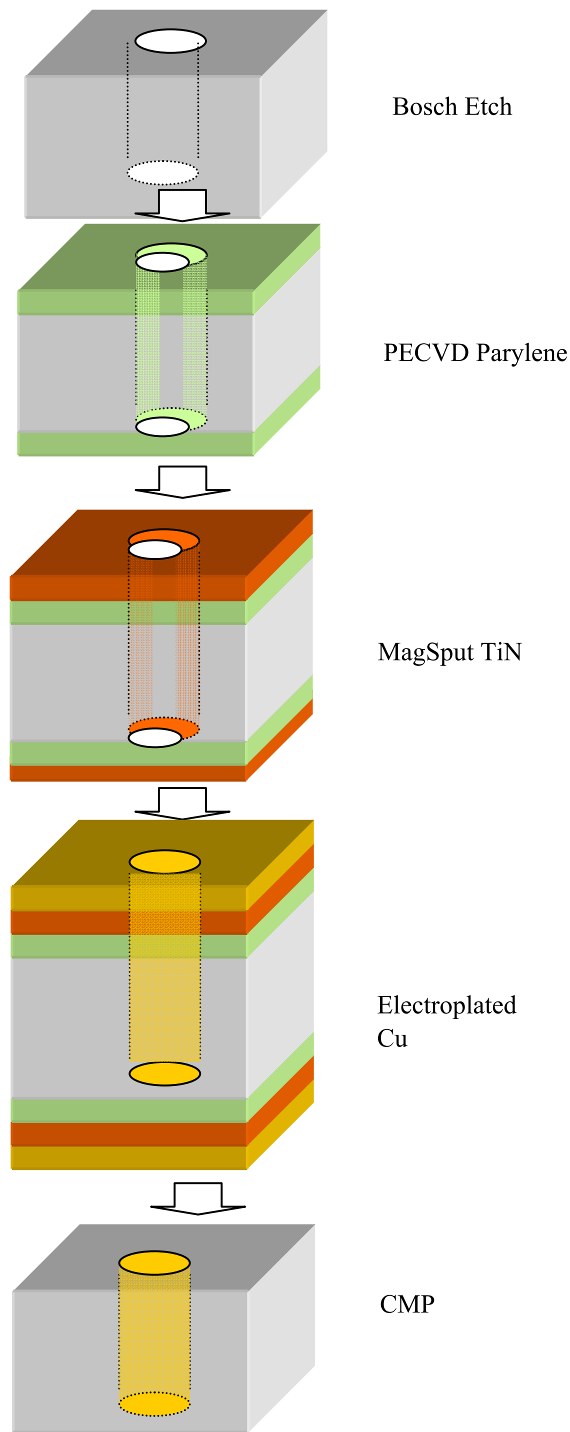

Fig-2: TWI Fabrication process.

TWI Reliability

To date, limited information has been published regarding the reliability of Cu TWIs under normal operating conditions. Recent efforts have focused on modeling the interaction between materials used in TWIs under accelerated life testing routines [8]. In other work, portions of a wafer containing vias were subjected to standard reliability testing which included; A stability bake (200˚C for 24 hrs) and thermal cycling (10X of -65 to 150 ˚C), on a total of four samples (two for each test) following MIL-STD 883E. Pre and post via resistance values were measured (Table 1) between tests to determine if any catastrophic failure had occurred [9].

In a typical IC application TWIs can be expected to carry electrical currents up to 10mA under heavy loading. Joule heating within the TWIs is produced as a result of the resistance of the Cu core thus generating heat. The heat generated must be dissipated outward efficiently to prevent increased thermal stress from manifesting itself by core material heat-up leading to excessive expansion/contraction of TWI materials. Coefficient of thermal expansion (CTE) differences between materials used in TWI construction can produce stress at their interface leading to premature failure. Micro-fractures present at the Si interface can also exacerbate the issue leading to crack propagation and fatigue failure [10]. In this particular research, the materials used in the construction of copper TWIs have a large range in CTE values (Table 2). Other relevant material properties listed in the table also contain a large range in thermal conductivity and yield strength values. The mechanical properties used for copper are representative of thin film characteristics as tested [8].

Table-1: Test results of reliability study.

	Before Testing Sample		**After Testing Sample**	
Stability Bake	1	2	1	2
Average	5.24E-3	5.89E-3	5.08E-3	5.89E-3
St. Deviation	2.74E-4	8.78E-5	1.26E-4	8.78E-5
Thermal Shock				
Average	5.40E-3	4.57E-3	5.33E-3	4.56E-3
St. Deviation	9.79E-5	8.56E-5	1.13E-4	7.40E-5

Table-2: Material properties at 25C.

	CTE (ppm/K)	Thermal Conductivity (W/m-K)	Yield Strength (MPa)
Silicon	3.0	150	Brittle mat'l
Copper	17.0	400	250
TiN	9.4	19.0	200000
Parylene-C	35.0	0.082	55

Thermal Analysis

The stress experienced in the TWI due to material CTE mismatches was explored using the COSMOSWORKS Finite Element Analysis (FEA) extension of SOLIDWORKS. Thermo-mechanical stress analysis under simulated operating conditions was done using the TWI model shown in Figure 3. Depending on the application, the actual layout of TWIs will vary, hence, assumptions were made to enable a fundamental understanding of TWI characteristics under powered

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conditions simplifying the modeling process. Listed below are the assumptions made in the model:

- steady state conditions to resolve fluctuations in power cycling under normal operating conditions.
- TWI power dissipation (~500nW) based on 10mA of current used as a worst case scenario.
- operating die temperature to be isothermal at 50˚C with no convective heat transfer occurring since the slice of the model was assumed to be taken in a central location of the wafer thickness.
- stress in model assumed to be zero at 25°C.

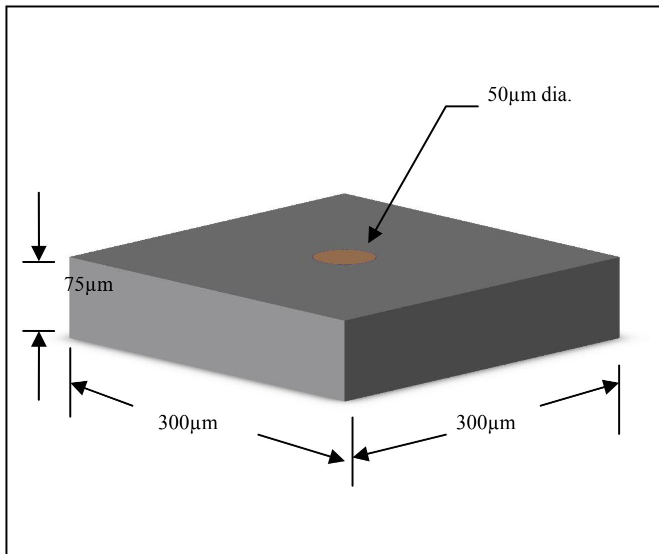

Fig-3: Model used in FEA.

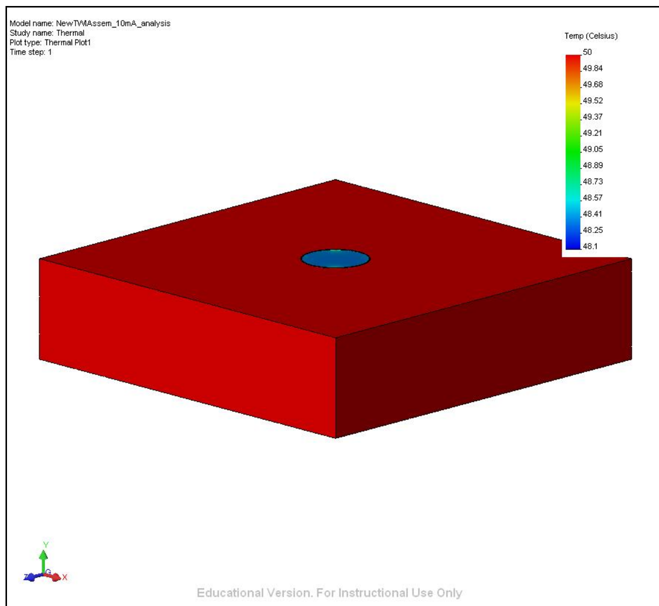

Fig-4: Model FEA results of temperature profile with die temp=50C; TWI power=10mA.

With the assumptions and boundary conditions listed above the results of the temperature profile are shown in Figure 4. As expected, minimal heat generation is produced within the TWI under 10mA of current, however, heat-up of the TWI has occurred as a result of the surrounding die temperature. Poor thermal conductivity of the Parylene layer does impede complete heat-up of the TWI resulting in a small gradient (~2 ˚C) between the die and TWI as shown in Figure 4.

Stress Analysis

Temperatures profiles generated by the thermal FEA were directly imported into the stress analysis algorithm and used to determine the Von Mises or effective stress profile of the TWI under 10mA of power. The copper, TiN and Si were assumed linear elastic in their behavior, with Parylene assumed to be non-linear elastic. With the heat up of the inner core due to the surrounding die temperature, thermal expansion of the copper did occur as shown by Figure 5.

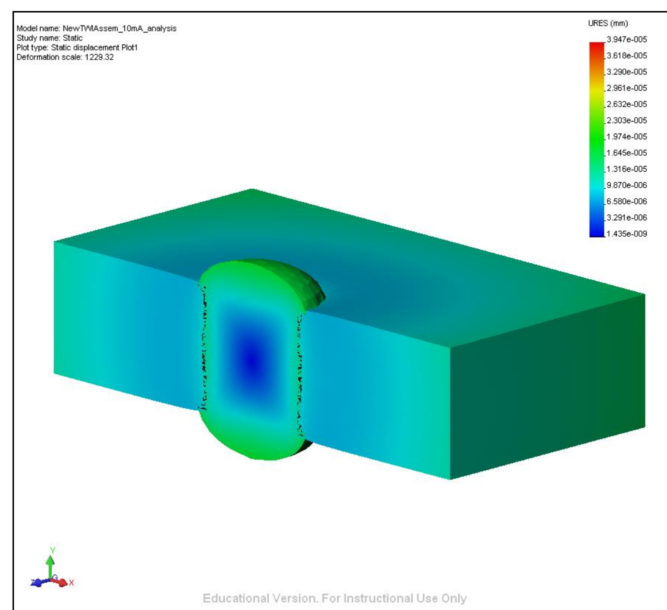

Fig-5: FEA model displacement results of TWI.

An exploded view of the TWI area is shown in Figure 6 revealing top and bottom areas of the copper expanding outward beyond the model surfaces by ~17nm. For reference, the zero-stressed position of the TiN layer is also shown along with the amount of expansion experienced by the TWI (~10nm) or (~40%) displacement.

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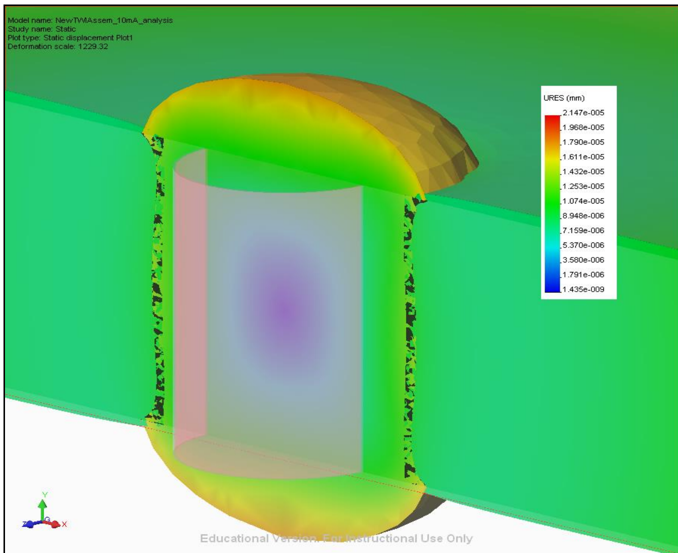

Fig-6: Enhanced view of TWI displacement.

Although minimal expansion was experienced in the copper, stress build up in the areas surrounding the copper/TiN/Si interface can be seen in Figure 7. As a result of the copper core expansion, the TiN layer is subjected to compressive forces from the copper expanding outward and the via compression on the TWI. In viewing the TWI closer, stress is experienced in the copper material with elevated levels of stress peaking at the top and bottom areas of the TWI as shown in Figure 8.

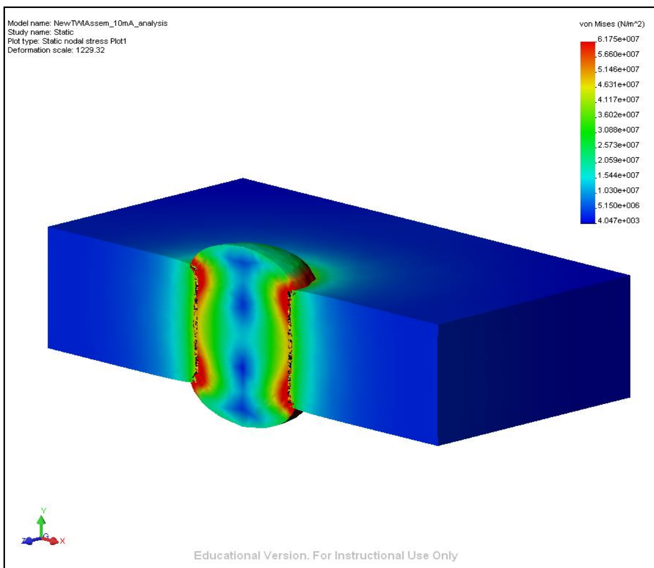

Fig-7: Von Mises stress distribution of TWI using imported temperature profile obtained from thermal analysis.

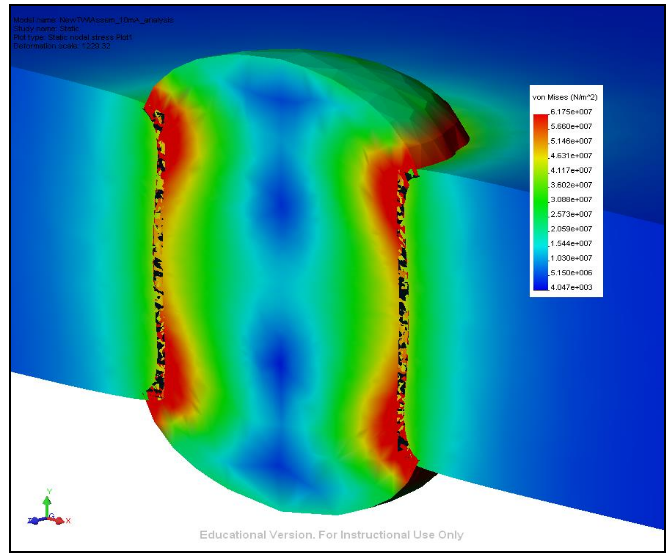

Fig-8: Exploded view of stress concentrations in TWI under assumed loaded conditions.

The stress distribution within the TWI shows a nominal stress of approximately 36MPa experienced at the other edge of the expansion area. This value falls very close to the analytical solution of 40MPa gained from the simple calculation of thermal expansion between two materials taking into account the different CTE values (1):

$$\sigma = (\alpha_1 - \alpha_2)\Delta T E_y \quad (1)$$

where α represent the CTE of the materials, ΛT the change in temperature from its resting point and E_y the modulus of the material. Due to equal and opposite forces acting on the TiN layer from the expansion of the copper core and the expansion of the Si material, the calculation was done using the CTE of copper and Si with the modulus of Cu. Effective stress is also present in the copper core depicted by the blue portion of the FEA plot, however, at much lower levels. The greatest amount of stress (61MPa) can be seen on the ends of the copper core where the greatest displacement occurs. Although the copper core does experience displacement, it is inherently a ductile material and stress levels are not enough to force permanent deformation of the material. Based on the yield strength of the materials used during fabrication of TWI, the stress levels were not high enough to yield failure by using the Von Mises failure criterion (2).

$$\frac{\sigma_e}{\sigma_Y} \geq 1 \quad (2)$$

This criterion postulates that yielding of an isotropic material begins when the strain energy of distortion reaches a limiting value. In this case, the yield strength, σ_Y, of the material. A plot of the model factor of safety (FOS) is shown in Figure 10. Some areas, however, did reveal a level of safety slightly less than one (~0.5) within the copper and TiN material. As shown in Figure 8, an FOS of much greater than

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one can be seen in the Parylene layer which corresponds with its ability to behave as a plastic material. The FOS plot reinforces the stress levels experience in the copper and TiN layers.

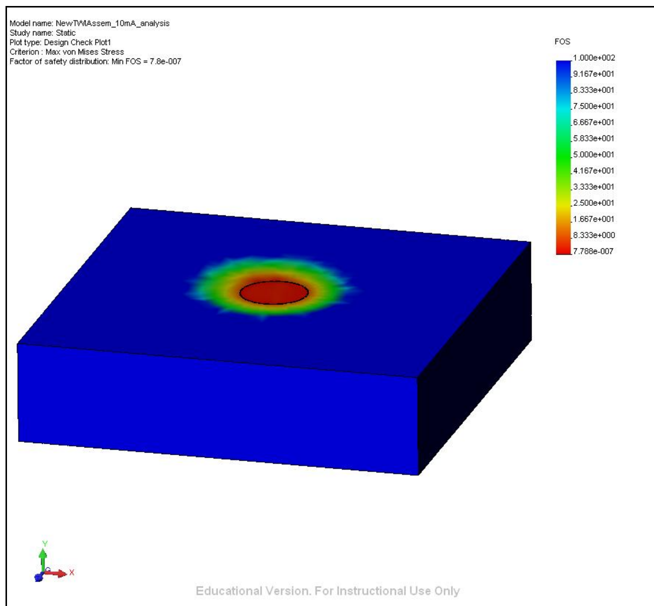

Fig-9: Factor of safety distribution within FEA model.

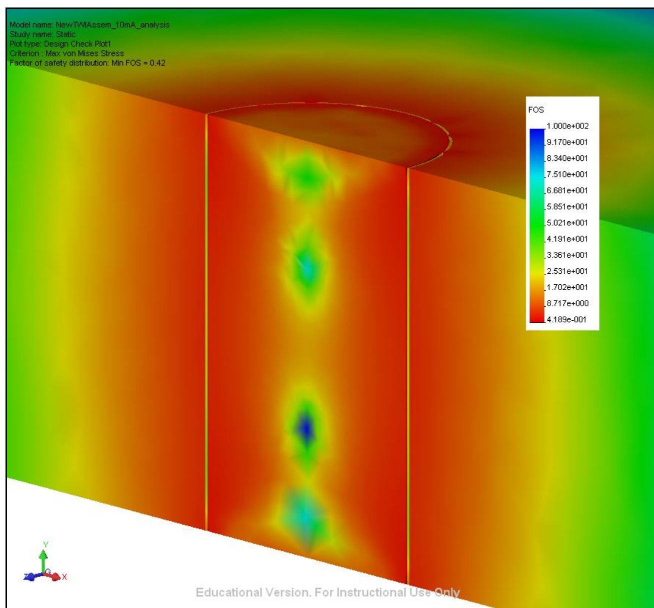

Fig-10: Exploded view of FOS levels within TWI FEA model.

Conclusions

With the next generation ICs, die temperatures will undoubtedly become higher leading to thermal management issues surging to the forefront in packaging design. In this discussion, CTE differences with TWI fabrication materials were found to generate appreciable amounts of stress at their interface under elevated die temperatures and not as a result of Joule heating. Under the given conditions, however, failure of the TWI was not expected. The model shown here merely provides insight into the stress levels and locations under the assumptions outlined earlier. A more in-depth discussion is now possible evaluating the TWI under more realistic conditions including plating anomalies and material layer discontinuities. Moving forward, a model representing an actual application including TWI pattern and chip power density will also be attempted to gain further understanding of reliability issues inherent with this design.

Acknowledgments

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