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Recent Advances in High Density Area Array Interconnect Bonding for 3-D Integration

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ABSTRACT

The demand for more complex and multifunctional microsystems with enhanced performance characteristics for military applications is driving the electronics industry toward the use of best-of-breed materials and device technologies. Three-dimensional (3-D) integration provides a way to build complex microsystems through bonding and interconnection of individually optimized device layers without compromising system performance and fabrication yield. Bonding of device layers can be achieved through polymer bonding or metal-metal interconnect bonding with a number of metal-metal systems. RTI has been investigating and characterizing Cu-Cu and Cu/Sn-Cu processes for high density area array imaging applications, demonstrating high yield bonding between sub-15 μm pads on large area array configurations. This paper will review recent advances in the development of high yield, large area array metal-metal interconnects which enable 3-D integration of heterogeneous materials (e.g. HgCdTe with silicon) and heterogeneous fabrication processes (e.g. infrared emitters or microbolometers with ICs) for imaging and scene projector applications.

Keywords: 3-D integration, IC stacking, high density area arrays, IR emitters, microbolometers, IR detector arrays.

1. INTRODUCTION

3-D integration technologies provide a technology path for miniaturization of systems/platforms, decreasing device weight and power requirements, and increasing data rates between chips for a wide range of military and commercial applications [1]. These technologies enable opportunities for integrating (stacking) dissimilar materials and device technologies into smaller, lighter, lower power, and higher signal processing packages for a variety of applications, including infrared (IR) imaging and scene projector applications. For example, 3-D integration can remove the real-estate limitations of hybridizing IR detector arrays to Si read-out ICs (ROICs) by allowing multiple layers of ICs with different functionalities (e.g., analog and digital ICs) to be stacked with short interconnect paths and large inter-layer signal bandwidth through bonding and interconnection of device layers. Further, the performance of a 3-D integrated detector array would be greatly enhanced through on-chip decision making [2]. The ability to separate different functionalities of Si circuitry into different device layers is significant because it allows ICs based on different processes and design rules to be fabricated as separate components (instead of monolithically). As a result, fabrication processes for the specific functionalities (e.g., sensing, emitting, or signal driving/processing) can be optimized to increase yield and reduce costs without many of the thermal budget, device real estate, and processing limitations inherent in monolithic approaches.

Of the bonding techniques available for creating 3D integrated devices, metal-metal bonding is the most compatible with die-to-die and die-to-wafer configurations for facilitating processing of known-good-die (the preferred route for integrating chips from low-yielding IC processes) and integrating chips of heterogeneous materials [3, 4]. Thermocompression bonding between arrays of Cu pads (Cu-Cu bonding) and solid-liquid diffusion bonding between arrays of Cu and Cu/Sn pads (Cu/Sn-Cu bonding) have been investigated for vertical integration of two or more devices. The rigid nature of these non-collapsible pad structures allows for very fine pitch interconnections to be made with low risk of bridging between neighboring interconnects. In addition, the metal-metal bonds are mechanically stable during subsequent thermal processes, which allows for the stacking of multiple layers of devices without disturbing the interconnections formed in previous bonding cycles.

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The choice of the bonding metallurgy is primarily dictated by the device surface topography and the thermal budget of the devices. Previous work showed that the bonding yield of rigid bump structures is critically dependent on a number of factors, including the intrinsic flatness of the device, the degree of planarity with which the devices can be aligned to one another, and the interconnect pad height uniformity [5]. The use of Cu/Sn pads provides some compliance for the bonding process, compensating for small height variations arising from these factors while maintaining high bonding yields. The compliance afforded by the Cu/Sn-Cu bonding system is due to the wetting action of the Sn on the opposing Cu pad when the Sn is heated above its melting temperature (232°C), leading to bond formation through solid-liquid diffusion [4, 5]. Since the Cu/Sn-Cu bonding process can be executed at temperatures below 300°C, Cu/Sn-Cu bonding consumes less of the thermal budget of ICs and subjects the bonded structures to lower thermal stresses than Cu-Cu thermocompression bonding. Cu-Cu bonding has been investigated because the Cu-Cu bond contains no intermetallic phases and therefore the joining interface is theoretically mechanically stronger than the Cu_6Sn_5 and Cu_3Sn intermetallic phases formed in Cu/Sn-Cu bonding. Cu-Cu bonding may also be preferred for ICs with Cu top metal structures because less back-end-of-line (BEOL) processing is required for the Cu terminated ICs.

Control of the device surface topography is important to achieve a high yielding bonding process for both metal-metal bonding systems. Ideally, devices would be fabricated with the final inorganic passivation layer (typically Si_3N_4 and/or SiO_2) planarized by a chemical-mechanical polish (CMP) process, thus providing a flat surface on which to fabricate the metal interconnect pads. This is not always the case, however, and it is common for devices to have surface topographies that vary by 1-2 microns, which is enough to significantly impact the bonding yield. Therefore, a flexible process that provides a flat surface for formation of the metal interconnect pads and a process that can be extended to most devices is required.

The feasibility of vertically stacking die by Cu-Cu interconnect bonding performed at 300°C and by Cu/Sn-Cu bonding of small arrays at temperatures < 300°C has been demonstrated by various groups [6. 7]. In this paper, we report on the fabrication and bonding of large area array test devices with high yield Cu-Cu and Cu/Sn-Cu bonding processes for interconnect pads ≤ 15 μm in diameter. Bonding was performed without the use of resins or fixing agents. The bond strengths and bond yield, as derived from die shear force measurements, post die shear inspections and electrical measurements, are presented. Cross sections of bonded samples were analyzed to investigate the bond-line formation between interconnect structures. Isothermal aging experiments were also performed to determine the long term stability of the bond interfaces; the aged samples were characterized through electrical measurements and/or die shear testing. Fabrication and bonding techniques for uniform area array bonding and scaling up to higher density arrays are also discussed.

2. EXPERIMENT

The area array test vehicle used in these experiments was built on a 200 mm wafer with two different daisy chain patterns. The pad layout was based on a pixilated readout IC designed by Fermi National Accelerator Laboratory for use in high energy physics detector applications. While the minimum I/O pitch on the device was 50 μm, the interconnect pad structures were designed to ultimately be compatible with 20 μm I/O pitch. In addition, while the original I/O layout was a sparsely populated area array, interconnect pads were added to the test vehicle to create a full area array pattern with uniform 50 μm pitch in the horizontal and vertical directions. The full array was 176 x 128 (22,528 total bumps) with a chip size approximately 8mm x 8 mm. Details regarding test chip fabrication were previously reported [8].

It is important to note that two patterns ('device array' and 'full array') were designed to form daisy chain structures for electrically probing assemblies after bonding. As seen in Figure 1, the device array layout connects every 8th pair of adjacent bumps in a row (channel) to create a daisy chain of 22 interconnects. This pattern replicated the electrical connections that would exist on the functional CMOS device with the non-daisy-chained pads serving as mechanical (electrically passive) support structures only. The full array layout connects all 176 interconnect pads in each row. The SiO2 passivated daisy chains on the device array produced topographical differences between the daisy-chained and non-daisy-chained pads. Prior to the formation of the final pads, the oxide layer was planarized by a chemical-mechanical polish (CMP). Two different plating templates were also designed to provide interconnect pads of different sizes. One plating template formed pads with 7 μm base diameters over the entire test vehicle; the other template

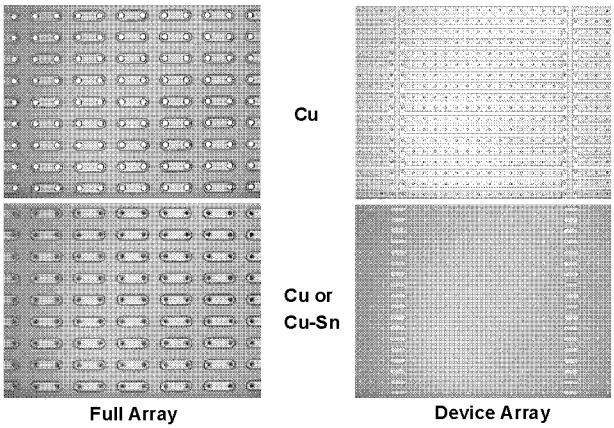

Fig. 1. Optical micrographs of full and device array daisy chain test structure layouts.

contained die with pad arrays of either 11 or 15 μm base diameters. The larger diameter pads provide some misalignment tolerance for the bonding of 7 μm pad arrays to the larger pad arrays.

Once the interconnect pad fabrication process was completed, wafers were diced to singulate the test devices and parts were bonded via thermocompression bonding with the parts held together under heat and pressure in order to form the metal-metal bond. Sample bonding was performed in a Suss Microtech FC150 precision bonder with nitrogen purge. Prior to bonding, the Cu/Sn pad chips were treated with the Plasma Assisted Dry Soldering process (PADS); a process that converts the surface Sn oxides into a brittle oxy-fluoride compound which breaks up under pressure during the bonding process, allowing the sub-surface Sn to flow to the surface and react with the contacted Cu surface [9]. The Cu pad chips were also chemically pre-treated with a weak sulfuric acid solution to remove Cu oxides immediately prior to bonding. Preliminary experiments were performed for both metal-metal systems and the bonding conditions shown in Table 1 were identified as good conditions for generating a high yielding sample set for comparison of the two systems. The bonding pressures shown in Table 1 correspond to applied forces per interconnect of 1.33 g and 0.4 g for Cu-Cu and Cu/Sn-Cu interconnect bonding, respectively.

Table 1: Metal-Metal Bonding Conditions

Metal System	Temperature (°C)	Mechanical Pressure (MPa)	Soak Time (min)
Cu-Cu	300	340	15
Cu/Sn-Cu	275	98	3

The bonded samples were characterized by two-wire probing of electrical connectivity, die shear testing of mechanical strength, and cross-section secondary electron microscopy (SEM). Die shear tests were performed on a Royce instruments Model 550 bond test system containing a maximum 10 kg load cell die shear head; samples were held in a fixture that clamped the bottom die while a shearing force was applied to the upper die. Visual inspections of the failure interfaces were conducted on all die sheared samples to identify the failure modes and any bonds that did not form during the bonding process. Thermal reliability of metal-metal bonded interconnects was determined from die shear tests of isothermally aged samples. Isothermal aging was performed by storing samples for a period of time (500 or 1000 hours) in a SUN Systems oven held at 150°C in ambient atmosphere.

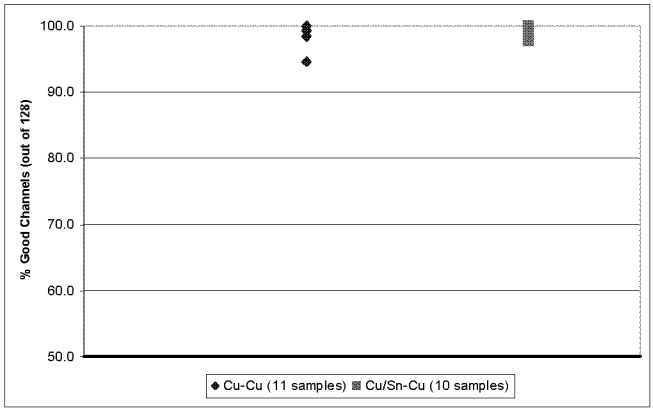

Fig. 2. Electrical connectivity for Cu-Cu and Cu/Sn-Cu bonded samples in terms of % of good channels out of 128 channels in the test vehicle.

3. ELECTRICAL CONNECTIVITY AND INTERCONNECT RESISTANCE

Each bonded sample contained 128 rows of daisy chains for measuring electrical connectivity of either 22 (device layout) or 176 (full layout) interconnects per channel. The electrical connectivity (% of good channels) obtained from two-wire probing of 11 Cu-Cu and 10 Cu/Sn-Cu interconnected samples is shown in Figure 2. The data contains measurements from both device and full layout integrated parts of both metal-metal systems. Regardless of the layout or metal-metal system, the number of open channels was generally very low with an average connectivity of 99.0% and 99.4% for Cu-Cu and Cu/Sn-Cu interconnected parts, respectively. Resistance measurements were also acquired during electrical probing. Taking into account a probe setup line resistance of 1.4 Ω (subtracted from the measurement), the average resistance of full and device arrays per channel for both metal-metal systems was calculated and the results shown in Table 2.

Table 2: Average Resistance (Ω) Per Channel

Metal System	Device Layout (22 interconnects)	Full Layout (176 interconnects)
Cu-Cu	11.9	14.1
Cu/Sn-Cu	11.6	13.2

Using the average channel resistance measurements from the two different layouts (device and full), estimates of the interconnect resistance were made. Assuming the routing lines contribute approximately the same resistance in the two designs, the difference in measured channel resistances for the two designs can be attributed to the difference in the number of electrically interconnected pads ($\Delta = 154$). The average channel resistance values given in Table 2 were then divided by this difference to provide an interconnect resistance estimate of ~ 15 mΩ and 10 mΩ for Cu-Cu and Cu/Sn-Cu interconnects, respectively.

4. MECHANICAL STRENGTH AND BOND YIELD

Die shear testing was performed on a number of bonded samples to determine the mechanical strength and failure modes of the integrated samples. Figure 3 shows the die shear test results in terms of die shear strength. As expected, Cu-Cu bonded samples were mechanically stronger than most Cu/Sn-Cu bonded samples tested and, in fact, none of the 6 Cu-Cu samples sheared at or below the maximum load cell limit of 10 kg. Conversely, the shear strengths of the Cu/Sn-Cu samples ranged from 42 MPa (3.74 kg) to 113 MPa (10 kg) with an average of 79 MPa.

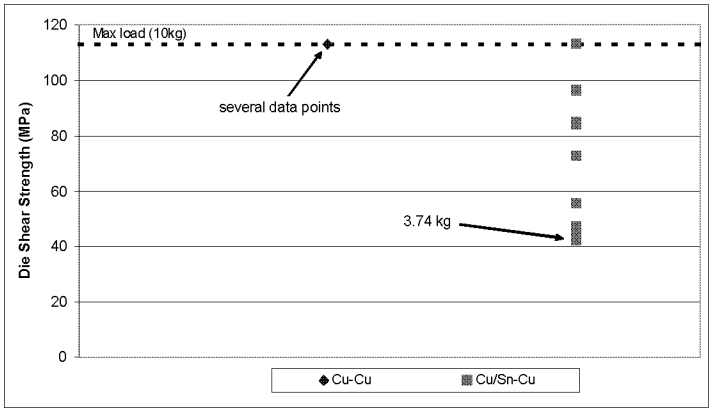

Fig. 3. Die shear strength of Cu-Cu and Cu/Sn-Cu bonded samples. Max. load of tool is 10 kg = 113 MPa.

After die shear testing, the failure interfaces of the bonds were visually inspected in order to identify interconnects that did not form bonds during the bonding process. Since the Cu-Cu samples did not shear during testing, these samples were forced to failure through multiple die shear cycles. For the Cu-Cu integrated parts, the predominant failure interface was at the base of the 7 µm pad, between the adhesion layer and the planarized SiO_2 passivation layer. For the Cu/Sn-Cu integrated parts, the failure interface occurred either in the Cu-Sn IM or at the metal/oxide interface at the base of the pads. Inspection of the sheared samples revealed that the bonding misalignment varied from 0.5 µm to 3 µm in x and/or y between the bonded pads. In general, the amount of misalignment correlated with the spread in die shear data with more misalignment corresponding to lower die shear strength (i.e. lower bonded surface area). The use of larger interconnect pads on one of the bonded die provided enough tolerance to prevent bond yield loss due to misalignment. Bond yield was primarily affected by poorly formed on non-bonded interconnects, observed either as intermittent point defects (particles or pad fabrication defects) in the arrays or small cluster defects located at the corners of the array. Inspections revealed no more than 3 bad bonds per open channel. Coupled with the electrical measurements (1 good channel = 22 or 176 good electrical interconnects, depending on the layout used), the bond yield for Cu-Cu and Cu/Sn-Cu bonded samples were both estimated to be ~ 99.999%.

5. BOND INTERFACE ANALYSIS

After bonding and probing, some samples were cross-sectioned for SEM and energy dispersive spectroscopy (EDS) analysis of the metal-metal bonds. A typical Cu-Cu bond is shown in Figure 4. The alignment between the parts is very good and the bond line formed between the Cu pads shows no voids. Figure 5 illustrates a typical Cu/Sn-Cu bond with good alignment between the pads and the presence of two intermetallic (IM) phases (as determined by EDS) created along the bond line during bonding. The stronger and more stable Cu_3Sn IM phase was created at the center of the bond while the Cu_6Sn_5 IM was formed at the edges of the bond where Sn was squeezed out of the joint due to the bonding pressure. Again, no voids are visible in the Cu/Sn-Cu bond line.

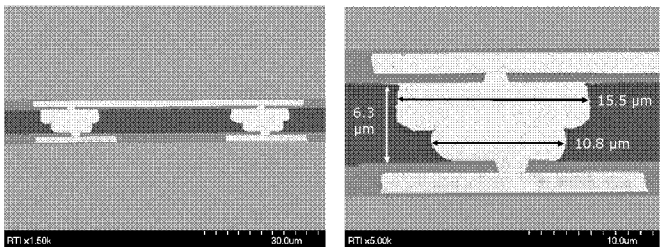

Fig. 4. Cross-section SEM micrographs of Cu-Cu bonds.

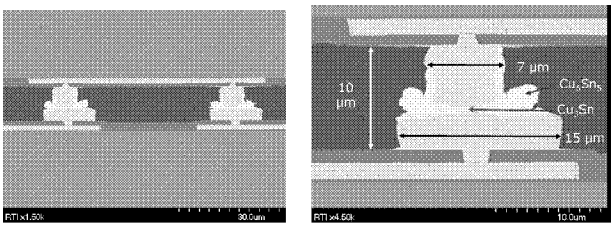

Fig. 5: Cross-section SEM micrographs of Cu/Sn-Cu bonds.

6. THERMAL RELIABILITY

Bonded samples representing both metal-metal systems were subjected to isothermal aging and die shear tested. Samples were subjected to 500 hours or 1000 hours of isothermal aging at 150°C in ambient. After storage, the samples were sheared. Die shear testing of three aged Cu-Cu samples provided mixed results. Two samples remained as mechanically strong as as-bonded assemblies (i.e. did not shear at the maximum tool load). One sample sheared at just above 40 MPa (3.6 kg of force), a substantial decrease in mechanical strength but still above the minimum 2.5 kg die shear strength required by MIL-STD-883G, Method 2019.7 for chips of this size. Visual inspection of the sheared samples revealed signs of Cu oxidation on all three samples, suggesting that oxidative effects at the bonded interface can compromise the mechanical integrity (and electrical properties) of the bonded interconnects. RTI is currently investigating underfill and encapsulation materials to prevent oxidation of Cu interconnects on subsequent test vehicles. The primary failure interface remained the seed layer/oxide interface of the smaller pad.

A larger sampling of bonded Cu/Sn-Cu samples was die shear tested after 0 hours (as-bonded, 8 samples), 500 hours (8 samples), and 1000 hours (14 samples) of isothermal aging with the results shown in Figure 6. The die shear results for the aged Cu/Sn-Cu test samples show that increasing isothermal aging time increases the minimum die shear strength and increases the number of samples that reach the maximum tool load of 10 kg. The improved behavior was attributed to the continued reaction of Cu_6Sn_5 IM into the stronger Cu_3Sn phase and confirmed by cross section SEM/EDS analysis of a 0 hour and 1000 hour aged sample. The analysis showed an increase in Cu_3Sn IM, particularly at the edges of the bond where Cu_6Sn_5 was present prior to isothermal storage. These results are complimentary to the findings of Tanida et al [10] that the evolution of a homogeneous Cu_3Sn phase along the bond-line structure produces higher tensile failure strengths and can be achieved by increasing the bonding temperature and/or soak time.

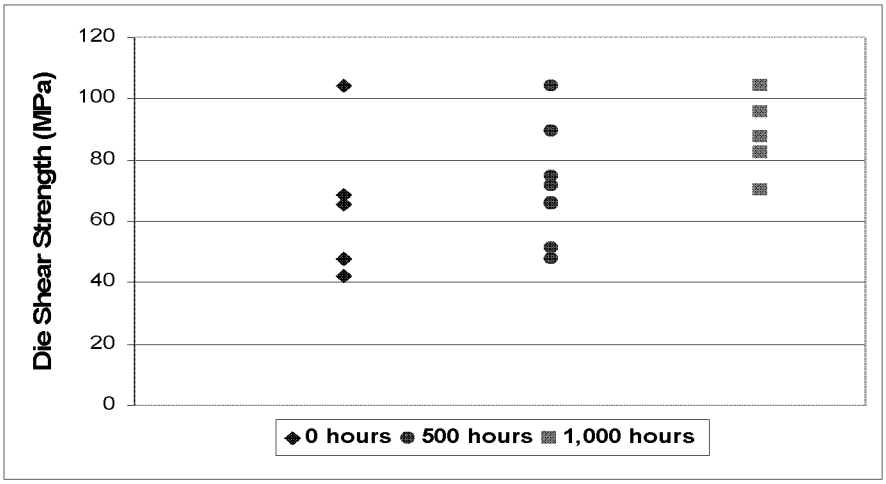

Fig. 6: Die shear test results for Cu/Sn-Cu bonded samples after isothermal storage

8. SUMMARY AND FUTURE APPLICATIONS

The results for Cu-Cu and Cu/Sn-Cu bonding systems compare quite favorably to each other. With the proper bonding conditions, each system produced high interconnect yields (99.999%) with low interconnect resistance (10 - 15 mΩ) and mechanically strong integrated samples that met the MIL-STD-883G standard which requires samples of this size to withstand at least 2.5 kg of shear force. Thermal aging tests revealed the need for passivation or encapsulation of bonded die to improve long term reliability of the bonded interconnects. Both systems are well suited for sub-15 μm diameter interconnects (sub-20 μm pitch) and high density area array bonding (integration) applications for imaging, sensing, and scene projector devices. The results from the test vehicle are now being used to guide designs for the next generation high energy physics particle detector ROIC device. At RTI, these metal-metal systems are also being developed for IR imaging devices using improved interconnect design and fabrication process flows for self-aligned bonding of area array interconnects with pitches down to 10 μm [11]. Future applications could include integration of metalized CMOS chips with MEMS devices (microbolometers or resistive IR emitter arrays) or IR LED arrays. The device designs and required chip integration orientations (face-to-face or back-to-face) will determine whether a combination of through-Si-interconnects and metal-metal bonding is required for a 3D-integrated array.

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