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A Prototyping Hardware Platform for ΔΣ ADCs

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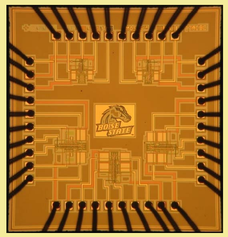

A Prototyping Hardware Platform for ΔΣ ADCs

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1. Introduction

The project involves development of a generic test-bed for prototyping and characterizing Delta-Sigma Analog-to-Digital Converters (ADCs). The ADCs are designed at the Analog Mixed Signal IC (AMS) Laboratory at Boise State. This is a high-speed evaluation board that can be connected into an FPGA board which assists in controlling the ADC chip and assists in capturing blocks of digital data.

2. Why Generic Test Board?

Semiconductor technology keeps advancing at a rapid pace as stated by Moore's law. This leads to faster and smaller transistors which lead to faster chips with more functionality. Delta-Sigma ADC directly benefits from the technology scaling leading to higher bandwidth and better resolution. In a research environment, researchers typically use varying range of technology with MOSFET channel length ranging from 0.5 µm to 45 nm which corresponds to supply voltages from 5, 3, 1.8, 1.2, and 1 and so on. These possess a challenge to the researchers when designing test chip. Thus, it is highly desirable for costumers to have generic hardware in which they can program the supply voltage required. These kinds of boards are used by research groups in many universities.

3. Hardware Architecture

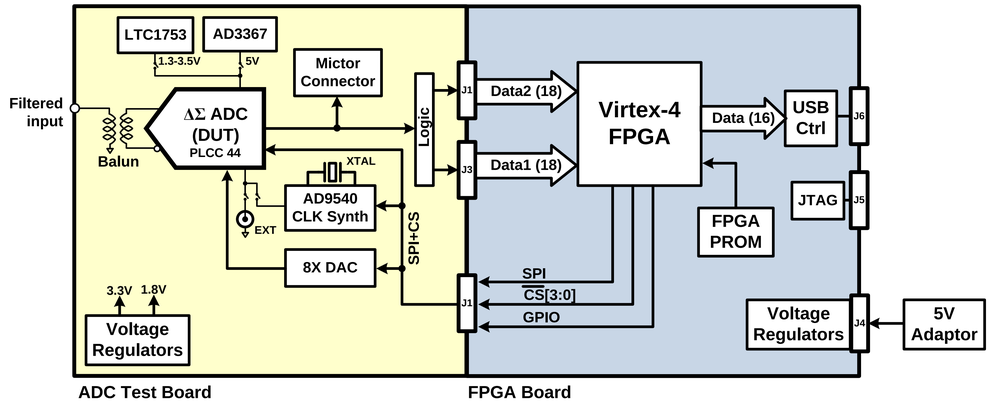

Figure 1: Hardware Architecture Block Diagram

4. Features

- Controlled by FPGA based FIFO board from Analog Devices (HSC-ADC-EVALC using Xilinx Virtex-4 FPGA).
- DC power supplies to the ADC; 5-Bit Digitally Programmable 1.3V to 3.5V Fixed Output Voltage and Low-Drop-Out, 5V Output Voltage.
- On-board programmable clock synthesizer (Up to 655 MHz Low Jitter Clock) and an External Clock Source.
- Programmable Voltage References (DAC) for testing purposes.
- Surface-mount PLCC44 (DUT) socket enables the users to insert the fabricated ADC chips.

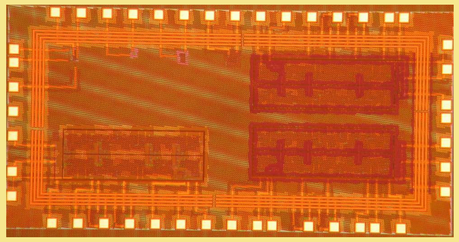

Figure 4: Layout of a Delta-Sigma ADC chip designed at the Analog Mixed Signal IC (AMS) Lab at BSU.

5. FPGA based Controller

Figure 2: Vertex4 FPGA Board Photograph

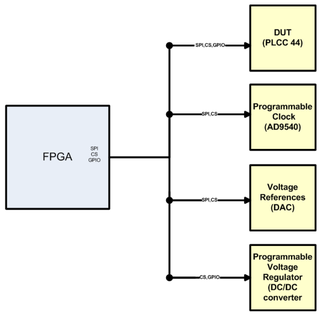

Figure 3: FPGA Control Signals

6. Programmable DC/DC Converter (LTC1753)

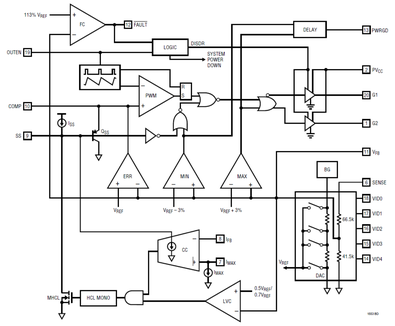

Figure 5: Block diagram for LTC1753*

7. Programmable Clock Synthesizer (AD9540)

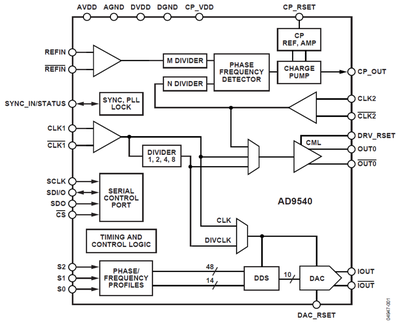

Figure 6: Block diagram for AD9540**